Programmable, Off-Line, PWM Controller

FEATURES
- All Control, Driving, Monitoring, and Protection Functions Included
- Low-Current Off Line Start Circuit
- Voltage Feed Forward or Current Mode Control
- High Current Totem Pole Output
- 50% Absolute Max Duty Cycle
- PWM Latch for Single Pulse Per Period
- Pulse-by-Pulse Current Limiting plus Shutdown for Over-Current Fault
- No Start-Up or Shutdown Transients
- Slow Turn-On Both Initially and After Fault Shutdown
- Shutdown Upon Over or Under Voltage Sensing
- Latch Off or Continuous Retry After Fault
- 1% Reference Accuracy
- 500kHz Operation
- 18 Pin DIL or 20 Pin PLCC Package

DESCRIPTION
The UC1851 family of PWM controllers are optimized for off-line primary side control. These devices include a high current totem pole output stage and a toggle flip-flop for absolute 50% duty cycle limiting. In all other respects this line of controllers is pin for pin compatible with the UC1841 series. Inclusion of all major housekeeping functions in these high performance controllers makes them ideal for use in cost sensitive applications.

Important features of these controllers include low current start-up, linear feed-forward for constant volt-second operation, and compatibility with both voltage or current mode control. In addition, these devices include a programmable start-threshold, as well as programmable over-voltage, under-voltage, and over current fault thresholds. The fault latch on these devices can be configured for automatic restart, or latched off response to a fault.

These devices are packaged in 18-pin plastic or ceramic dual-in-line packages, or for surface mount applications, a 20 Pin PLCC. The UC1851 is characterized for -55°C to +125°C operation while the UC2851 and UC3851 are designed for -40°C to +85°C and 0°C to +70°C, respectively.
**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Supply Voltage, +V IN (Pin 15)
- Voltage Driven ............................................ +32V
- Current Driven, 100mA maximum ......................... Self-limiting

PWM Output Voltage (Pin 12) .................. 40V
PWM Output Current, Steady-State (Pin 12) .......... 400mA
PWM Output Peak Energy Discharge .......... 20mJoules

Driver Bias Current (Pin 14) .................. -200mA
Reference Output Current (Pin 16) ........ -50mA
Slow-Start Sink Current (Pin 8) ........... 20mA
Vin Sense Current (Pin 11) .................. 10mA
Current Limit Inputs (Pins 6 & 7) ........... -0.5 to +5.5V
Stop Input (Pin 4) .................. -0.3 to +5.5V

**Comparator Inputs**
(Pins 1–7, 9–11, 16) .................. Internally clamped at 12V

Power Dissipation at TA = 25°C (Note 3) .............. 1000mW
Power Dissipation at TC = 25°C (Note 3) .............. 2000mW
Operating Junction Temperature .................. -55°C to +150°C
Storage Temperature Range .................. -65°C to +150°C
Lead Temperature (Soldering, 10 sec) .................. +300°C

Note 1: All voltages are with respect to ground, Pin 13.
Currents are positive-into, negative-out of the specified terminal

Note 2: All pin numbers are referenced to DIL-18 package.

Note 3: Consult Packaging Section of Databook for thermal limitations and considerations of package.

**ELECTRICAL CHARACTERISTICS:**

Unless otherwise stated, these specifications apply for TA = -55°C to +125°C for the UC1851, -40°C to +85°C for the UC2851, and 0°C to 70°C for the UC3851; VIN = 20V, RT = 20kΩ, CT = .001 mfd, RR = 10kΩ, CR = .001mfd. Current Limit Threshold = 200mV, TA = TJ.

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**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for $T_A = -55°C$ to $+125°C$ for the UC1851, $-40°C$ to $+85°C$ for the UC2851, and $0°C$ to $70°C$ for the UC3851; $V_{IN} = 20V$, $R_T = 20kΩ$, $C_T = .001$ mfd, $R_R = 10kΩ$, $C_R = .001$ mfd. Current Limit Threshold $= 200mV$, $T_A = T_J$.

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*Note 1: Guaranteed by design. Not 100% tested in production.*
FUNCTIONAL DESCRIPTION

PWM CONTROL

1. Oscillator
   Generates a fixed-frequency internal clock from an external R_T and C_T.
   Frequency = \( \frac{K_C}{R_TC_T} \) where K_C is a first-order correction factor ≈ 0.3 log (C_T x 10^{12}).

2. Ramp Generator:
   Develops a linear ramp with slope defined externally by \( \frac{dV}{dt} = \frac{\text{sense voltage}}{R_RC_R} \).
   C_R is normally selected ≤ C_T and its value will have some effect upon valley duty cycle.
   Limiting the minimum value for I_SENSE into pin 11 will establish a maximum duty cycle clamp.
   C_R terminal can be used as an input port for current mode control.

3. Error Amplifier
   Conventional operational amplifier for closed-loop gain and phase compensation.
   Low output impedance; unity-gain stable.
   The output is held low by the slow start voltage at turn on in order to minimize overshoot.

4. Reference Generator:
   Precision 5.0V for internal and external usage to 50mA.
   Tracking 3.0V reference for internal usage only with nominal accuracy of ±2%.
   40V clamp zener for chip OV protection, 100mA maximum current.

5. PWM Comparator:
   Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.

6. PWM Latch:
   Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse comparator, or the error latch. Resets with each internal clock pulse.

7. PWM Output Switch:
   Totem pole output stage capable of sourcing and sinking 1 amp peak current. The active "on" state is high.

SEQUENCING FUNCTIONS

1. Start/UV Sense:
   With an increasing voltage, this comparator generates a turn-on signal and releases the slow start clamp at a start threshold.
   With a decreasing voltage, it generates a turn-off command at a lower level separated by a 200µA hysteresis current.

2. Drive Switch:
   Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.

3. Driver Bias:
   Supplies drive to external circuitry upon start-up.

4. Slow Start:
   Clamps low to hold PWM OFF. Upon release, rises with rate controlled by R_SC_S for slow increase of output pulse width.
   Can also be used as an alternate maximum duty cycle clamp with an external voltage divider.

PROTECTION FUNCTIONS

1. Error Latch:
   When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset.
   Inputs to Error Latch are:
   a. OV > 3.2V (Typically 3V)
   b. Stop > 2.4V (Typically 1.6V)
   c. Current Sense 400mV over threshold. (Typical).
   Error Latch resets when slow start voltage falls to 0.4V if Reset Pin < 2.8V. With Pin 5 > 3.2V, Error Latch will remain set.

2. Current Limiting:
   Differential input comparator terminates individual output pulses each time sense voltage rises above threshold.
   When sense voltage rises to 400mV (typical) above threshold, a shutdown signal is sent to Error Latch.

3. External Stop:
   A voltage over 2.4 will set the Error Latch and hold the output off.
   A voltage less than 0.8V will defeat the error latch and prevent shutdown.
   A capacitor here will slow the action of the error latch for transient protection by providing a Typical Delay of 13ms/µF.
Start/UV Hysteresis Current

Oscillator Frequency

PWM Output Minimum Pulse Width

Error Amplifier Open-Loop Gain and Phase

Shutdown Timing
High Peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 13 in a single ground point.

Nominal Frequency = \( \frac{1}{RT_{CT}} \approx 50\,\text{kHz} \)

Start Voltage = \( 3 \left( \frac{R_1 + R_2 + R_3}{R_2 + R_3} \right) + 0.2R_1 = 12\,\text{V} \)

UV Fault Voltage = \( 3 \left( \frac{R_1 + R_2 + R_3}{R_2 + R_3} \right) = 8\,\text{V} \)

Current Limit = 200mV

Current Fault Voltage = 600mV

Duty Cycle Clamp = 50%

@Vin = 15V, Duty Cycle = 48%

@Vin = 30V, Duty Cycle = 24%

For further application information see UC1840/UC1841 Data Sheets
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