**DESCRIPTION**

The UC3842 is available in an 8-Pin mini-DIP the necessary features to implement off-line, fixed-frequency current-mode control schemes with a minimal external parts count. This technique results in improved line regulation, enhanced load response characteristics, and a simpler, easier to design control loop. Topological advantages include inherent pulse-by-pulse current limiting.

Protection circuitry includes built-in undervoltage lock-out and current limiting. Other features include fully-latched operation, a 1% trimmed bandgap reference, and start-up current less than 1mA.

These devices feature a totem-pole output designed to source and sink high peak current from a capacitive load, such as the gate of a power MOSFET. Consistent with N-channel power devices, the output is low in the OFF-state.

**FEATURES**

- Low start-up current (≤1mA)
- Automatic feed-forward compensation
- Pulse-by-pulse current limiting
- Enhanced load response characteristics
- Undervoltage lock-out with hysteresis
- Double pulse suppression
- High current totem-pole output
- Internally-trimmed bandgap reference
- 400kHz operation, guaranteed min

**APPLICATIONS**

- Off-line switched mode power supplies
- DC-to-DC converters UC3842

**PIN CONFIGURATIONS**

![Pin Diagram](chart)

**BLOCK DIAGRAM**

![Block Diagram](chart)

**NOTE:**
Pin numbers in parentheses refer to the D package.
## ORDERING INFORMATION

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
<th>ORDER CODE</th>
<th>DWG #</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-Pin Plastic Dual In-Line Package (DIP)</td>
<td>0 to +70°C</td>
<td>UC3842N</td>
<td>0404B</td>
</tr>
<tr>
<td>14-Pin Plastic Small Outline (SO) Package</td>
<td>0 to +70°C</td>
<td>UC3842D</td>
<td>0405B</td>
</tr>
</tbody>
</table>

## ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>RATING</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply voltage (I_{CC}&lt;30mA)</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>VCC</td>
<td>Supply voltage (low impedance source)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IOUT</td>
<td>Output current ±1</td>
<td>±1</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>Output energy (capacitive load)</td>
<td>5</td>
<td>µJ</td>
</tr>
<tr>
<td></td>
<td>Analog inputs (Pin 2, Pin 3)</td>
<td>-0.3 to 6.3</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Error amp output sink current</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>PD</td>
<td>Power dissipation at TA≤70°C (derate 12.5mW/°C for TA&gt;70°C)</td>
<td>1</td>
<td>W</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage temperature range</td>
<td>-65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>TSOLD</td>
<td>Lead temperature (soldering, 10sec max)</td>
<td>300</td>
<td>°C</td>
</tr>
</tbody>
</table>

### NOTES:

1. All voltages are with respect to Pin 5; all currents are positive into the specified terminal.
2. See section in application note on “Power Dissipation Calculation”.
3. This parameter is guaranteed, but not 100% tested in production.
## DC AND AC ELECTRICAL CHARACTERISTICS

0 ≤ TJ ≤ 70°C for UC3842; VCC=15V; RT=10kΩ; CT=3.3nF, unless otherwise specified.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>UC3842</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
</tr>
</tbody>
</table>

### Reference section

- **VOUT**: Output voltage
  - TJ=25°C, IO=1mA
  - Min: 4.90 V, Typ: 5.00 V, Max: 5.10 V

- **Line regulation**: 12 ≤ VIN ≤ 25V
  - Min: 6 mV, Typ: 20 mV, Max: 4 mV

- **Load regulation**: 1 ≤ IO ≤ 20mA
  - Min: 6 mV, Typ: 25 mV, Max: 0.4 mV

- **Temp. stability**
  - Min: 0.2 mV/°C, Typ: 0.4 mV/°C, Max: 0.4 mV/°C

- **Total output variation**
  - Min: 4.82 V, Typ: 5.18 V, Max: 5.18 V

- **TJ**: 25°C

### Oscillator section

- **Initial accuracy**: TJ=25°C
  - Min: 47 kHz, Typ: 52 kHz, Max: 57 kHz

- **Voltage stability**: 12 ≤ VCC ≤ 25V
  - Min: 0.2%, Typ: 1%, Max: 1%

- **Temp. stability**
  - TJ=25°C, 1000 Hrs.
  - Min: 5%, Typ: 5%, Max: 5%

- **Amplitude**: Vpin4 peak-to-peak
  - Min: 1.7 V

### Error amp section

- **Input voltage**: VPin 1=2.5V
  - Min: 2.42 V, Typ: 2.50 V, Max: 2.58 V

- **IBIAS**: Input bias current
  - Min: -0.3 mA, Typ: -2 mA, Max: -2 mA

- **AVOL**: 2 ≤ VOUT ≤ 4V
  - Min: 65 dB, Typ: 90 dB, Max: 90 dB

- **Unity gain bandwidth**
  - TJ=25°C
  - Min: 0.5 MHz, Typ: 1 MHz, Max: 1 MHz

- **PSRR**: Power supply rejection ratio
  - 12 ≤ VCC ≤ 25V
  - Min: 60 MHz, Typ: 70 MHz, Max: 70 MHz

- **ISINK**: Output sink current
  - Min: 2 mA, Typ: 6 mA, Max: 6 mA

- **ISOURCE**: Output source current
  - Min: 0.5 mA, Typ: 0.8 mA, Max: 0.8 mA

- **VOUT High**: VPIN2=2.7V, Rl=15k to ground
  - Min: 5 V, Typ: 6 V, Max: 6 V

- **VOUT Low**: VPIN2=2.7V, RL=15k to Pin 8
  - Min: 0.7 V, Typ: 1.1 V, Max: 1.1 V

### Current sense section

- **Gain 2, 3**: 2.85 V/V
  - Min: 3, Typ: 3.15, Max: 3.15

- **Maximum input signal**
  - Min: 0.9 V, Typ: 1.1 V, Max: 1.1 V

- **PSRR**: Power supply rejection ratio
  - 12 ≤ VCC ≤ 25V
  - Min: 70 dB, Typ: 70 dB, Max: 70 dB

- **IBIAS**: Input bias current
  - Min: -2 µA, Typ: -10 µA, Max: -10 µA

- **Delay to output**
  - Min: 150 ns, Typ: 300 ns, Max: 300 ns
# DC AND AC ELECTRICAL CHARACTERISTICS

$0 \leq T_J \leq 70^\circ\text{C}$ for UC3842; $V_{CC}=15\text{V}$; $R_T=10k\Omega$; $C_T=3.3\text{nF}$, unless otherwise specified.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>UC3842</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
</tr>
<tr>
<td>Output section</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low-Level</td>
<td>$I_{SINK}=20\text{mA}$</td>
<td>0.1</td>
<td>0.4</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output High-Level</td>
<td>$I_{SOURCE}=200\text{mA}$; $I_{SOURCE}=20\text{mA}$</td>
<td>13</td>
<td>13.5</td>
</tr>
<tr>
<td>$t_R$</td>
<td>Rise time</td>
<td>$C_L=1\text{nF}$</td>
<td>50</td>
<td>150</td>
</tr>
<tr>
<td>$t_F$</td>
<td>Fall time</td>
<td>$C_L=1\text{nF}$</td>
<td>50</td>
<td>150</td>
</tr>
<tr>
<td>Undervoltage lockout section</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Start threshold</td>
<td></td>
<td></td>
<td>14.5</td>
<td>16</td>
</tr>
<tr>
<td>Min. operating voltage after turn on</td>
<td></td>
<td></td>
<td>8.5</td>
<td>10</td>
</tr>
<tr>
<td>PWM section</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum duty cycle</td>
<td></td>
<td></td>
<td>93</td>
<td>97</td>
</tr>
<tr>
<td>Minimum duty cycle</td>
<td></td>
<td></td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Total standby current</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Start-up current</td>
<td></td>
<td></td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Operating supply current</td>
<td>$V_{PIN2}=V_{PIN3}=0\text{V}$</td>
<td>11</td>
<td>17</td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>Zener voltage</td>
<td>$I_{CC}=25\text{mA}$</td>
<td>34</td>
<td></td>
</tr>
<tr>
<td>Maximum operating frequency section</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum operating frequency for all functions operating cycle-by-cycle</td>
<td></td>
<td></td>
<td>400</td>
<td></td>
</tr>
</tbody>
</table>

### NOTES:
1. These parameters, although guaranteed, are not 100% tested in production.
2. Parameter measured at trip point of latch with $V_{PIN2}=0$.
3. Gain defined as:
   \[ A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}} ; 0 \leq V_{PIN3} \leq 0.8\text{V} \]

### UNDERVOLTAGE LOCKOUT

- During Undervoltage Lock-Out, the output driver is biased to a high impedance state. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with output leakage current.

### ERROR AMP CONFIGURATION

- Error AMP can source or sink up to 0.5mA.
CURRENT SENSE CIRCUIT

NOTE:
Peak current (I_s) is determined by the formula:

\[ I_{S\,\text{MAX}} = \frac{1.0V}{R_s} \]

A small RC filter may be required to suppress switch transients.

TYPICAL PERFORMANCE CHARACTERISTICS

Output Saturation Characteristics

Error Amplifier Open-Loop Frequency Response
OPEN-LOOP LABORATORY TEST FIXTURE

NOTE:
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to Pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Pin 3.

SHUTDOWN TECHNIQUES

NOTE:
Shutdown of the UC3842 can be accomplished by two methods; either raise Pin 3 above 1V or pull Pin 1 below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to Block Diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at Pins 1 and/or 3 is removed. In the examples shown, an externally-latched shutdown may be accomplished by adding an SCR which will be reset by cycling VCC below the lower UVLO threshold (10V). At this point all internal bias is removed, allowing the SCR to reset.
**OFF-LINE FLYBACK REGULATOR**

![Circuit Diagram]

**SPECIFICATIONS**

- **Input line voltage:** 90VAC to 130VAC
- **Input frequency:** 50 or 60Hz
- **Switching frequency:** 40kHz±10%
- **Output power:** 25W maximum
- **Output voltage:** 5V±5%
- **Output current:** 2 to 5A
- **Line regulation:** 0.01%/V
- **Load regulation:** 8%/A
- **Efficiency @ 25 W, V_N=90VAC:** 70%
- **V_N=130VAC:** 65%
- **Output short-circuit current:** 2.5A average

**NOTE:**

This circuit uses a low-cost feedback scheme in which the DC voltage developed from the primary-side control winding is sensed by the UC3842 error amplifier. Load regulation is therefore dependent on the coupling between secondary and control windings, and on transformer leakage inductance. For applications requiring better load regulation, a UC1901 Isolated Feedback Generator can be used to directly sense the output voltage.
SYNCHRONIZATION AND MAXIMUM DUTY CYCLE CLAMP

NOTES:

\[ I = \frac{1.44}{R_A} \frac{1}{2R_B} C \]

\[ D_{\text{MAX}} = \frac{R_B}{R_A} \frac{1}{2R_B} \]