The TPIC6C595 is a monolithic, medium-voltage, low-current power 8-bit shift register designed for use in systems that require relatively moderate load power such as LEDs. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other low-current or medium-voltage loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift register clock (SRCK) and the register clock (RCK), respectively. The device transfers data out the serial output (SER OUT) port on the rising edge of SRCK. The storage register transfers data to the output buffer when shift register clear (CLR) is high. When CLR is low, the input shift register is cleared. When output enable (G) is held high, all data in the output buffers is held low and all drain outputs are off. When G is held low, data from the storage register is transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs have sink-current capability. The SER OUT allows for cascading of the data from the shift register to additional devices.

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriate logic voltage level, preferably either VCC or ground. Specific guidelines for handling devices of this type are contained in the publication Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies available from Texas Instruments.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
description (continued)

Outputs are low-side, open-drain DMOS transistors with output ratings of 33 V and 100 mA continuous sink-current capability. Each output provides a 250-mA maximum current limit at $T_C = 25^\circ C$. The current limit decreases as the junction temperature increases for additional device protection. The device also provides up to 2500 V of ESD protection when tested using the human-body model and the 200-V machine model.

The TPIC6C595 is characterized for operation over the operating case temperature range of $-40^\circ C$ to $125^\circ C$.

logic diagram (positive logic)
schematic of inputs and outputs

**EQUIVALENT OF EACH INPUT**

- VCC
- Input
- GND
- 25 V
- 12 V

**TYPICAL OF ALL DRAIN OUTPUTS**

- DRAIN
- 33 V
- 20 V
- GND

**Absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)**

- Logic supply voltage, $V_{CC}$ (see Note 1) ........................................ 7 V
- Logic input voltage range, $V_{I}$ ........................................ $-0.3 \text{ V to 7 V}$
- Power DMOS drain-to-source voltage, $V_{DS}$ (see Note 2) ........................................ 33 V
- Continuous source-to-drain diode anode current ........................................ 250 mA
- Pulsed source-to-drain diode anode current (see Note 3) ........................................ 500 mA
- Pulsed drain current, each output, all outputs on, $I_{D}$, $T_C = 25^\circ \text{C}$ (see Note 3) ........................................ 250 mA
- Continuous drain current, each output, all outputs on, $I_{D}$, $T_{C} = 25^\circ \text{C}$ ........................................ 100 mA
- Peak drain current single output, $I_{DM}$, $T_{C} = 25^\circ \text{C}$ (see Note 3) ........................................ 250 mA
- Single-pulse avalanche energy, $E_{AS}$ (see Figure 4) ........................................ 30 mJ
- Avalanche current, $I_{AS}$ (see Note 4) ........................................ 200 mA
- Continuous total dissipation ........................................ See Dissipation Rating Table
- Operating virtual junction temperature range, $T_{J}$ ........................................ $-40^\circ \text{C to 150^\circ C}$
- Operating case temperature range, $T_{C}$ ........................................ $-40^\circ \text{C to 125^\circ C}$
- Storage temperature range, $T_{stg}$ ........................................ $-65^\circ \text{C to 150^\circ C}$
- Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ........................................ $260^\circ \text{C}$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**NOTES:**

1. All voltage values are with respect to GND.
2. Each power DMOS source is internally connected to GND.
3. Pulse duration $\leq 100$ $\mu$s and duty cycle $\leq 2\%$.
4. DRAIN supply voltage = 15 V, starting junction temperature ($T_{JS}$) = 25°C, $L = 1.5$ $H$, $I_{AS} = 200$ mA (see Figure 4).

<table>
<thead>
<tr>
<th>PACKAGE</th>
<th>$T_C \leq 25^\circ \text{C}$ POWER RATING</th>
<th>DERATING FACTOR ABOVE $T_C = 25^\circ \text{C}$</th>
<th>$T_C = 125^\circ \text{C}$ POWER RATING</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>1087 mW</td>
<td>8.7 mW/$^\circ \text{C}$</td>
<td>217 mW</td>
</tr>
<tr>
<td>N</td>
<td>1470 mW</td>
<td>11.7 mW/$^\circ \text{C}$</td>
<td>294 mW</td>
</tr>
<tr>
<td>PW</td>
<td>1372 mW</td>
<td>10.976 mW/$^\circ \text{C}$</td>
<td>274 mW</td>
</tr>
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</table>
### recommended operating conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic supply voltage, $V_{CC}$</td>
<td>4.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>High-level input voltage, $V_{IH}$</td>
<td>0.85 $V_{CC}$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Low-level input voltage, $V_{IL}$</td>
<td>0.15 $V_{CC}$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Pulsed drain output current, $T_C = 25^\circ C$, $V_{CC} = 5 \text{ V}$, all outputs on (see Notes 3 and 5 and Figure 11)</td>
<td>250</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Setup time, SER IN high before SRCK↑, $t_{SU}$ (see Figure 2)</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Hold time, SER IN high after SRCK↑, $t_h$ (see Figure 2)</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Pulse duration, $t_w$ (see Figure 2)</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Operating case temperature, $T_C$</td>
<td>−40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

### electrical characteristics, $V_{CC} = 5 \text{ V}$, $T_C = 25^\circ C$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{(BR)}DSX$</td>
<td>Drain-to-source breakdown voltage</td>
<td>$</td>
<td>I_D</td>
<td>= 1 \text{ mA}$</td>
<td>33</td>
</tr>
<tr>
<td>$V_{SD}$</td>
<td>Source-to-drain diode forward voltage</td>
<td>$</td>
<td>I_F</td>
<td>= 100 \text{ mA}$</td>
<td>0.85</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High-level output voltage, SER OUT</td>
<td>$</td>
<td>I_{OH}</td>
<td>= −20 \mu A$, $V_{CC} = 4.5 \text{ V}$</td>
<td>4.4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$</td>
<td>I_{OH}</td>
<td>= −4 \text{ mA}$, $V_{CC} = 4.5 \text{ V}$</td>
<td>4</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low-level output voltage, SER OUT</td>
<td>$</td>
<td>I_{OL}</td>
<td>= 20 \mu A$, $V_{CC} = 4.5 \text{ V}$</td>
<td>0.005</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$</td>
<td>I_{OL}</td>
<td>= 4 \text{ mA}$, $V_{CC} = 4.5 \text{ V}$</td>
<td>0.3</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>High-level input current</td>
<td>$V_{CC} = 5.5 \text{ V}$, $V_I = V_{CC}$</td>
<td>1</td>
<td></td>
<td>\mu A</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Low-level input current</td>
<td>$V_{CC} = 5.5 \text{ V}$, $V_I = 0$</td>
<td>$−1$</td>
<td></td>
<td>\mu A</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Logic supply current</td>
<td>$V_{CC} = 5.5 \text{ V}$, All outputs off</td>
<td>20</td>
<td>200</td>
<td>\mu A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 5.5 \text{ V}$, All outputs on</td>
<td>150</td>
<td>500</td>
<td>\mu A</td>
</tr>
<tr>
<td>$I_{CC(FRQ)}$</td>
<td>Logic supply current at frequency</td>
<td>$f_{SRCK} = 5 \text{ MHz}$, All outputs off, $C_L = 30 \text{ pF}$, See Figures 2 and 6</td>
<td>1.2</td>
<td>5</td>
<td>mA</td>
</tr>
<tr>
<td>$I_N$</td>
<td>Nominal current</td>
<td>$V_{DS(on)} = 0.5 \text{ V}$, $T_C = 85^\circ C$, $I_N =</td>
<td>I_D</td>
<td>$</td>
<td>See Notes 5, 6, and 7</td>
</tr>
<tr>
<td>$I_{DSX}$</td>
<td>Off-state drain current</td>
<td>$V_{DS} = 30 \text{ V}$, $V_{CC} = 5.5 \text{ V}$</td>
<td>0.1</td>
<td>0.2</td>
<td>\mu A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DS} = 30 \text{ V}$, $T_C = 125^\circ C$, $V_{CC} = 5.5 \text{ V}$</td>
<td>0.15</td>
<td>0.3</td>
<td>\mu A</td>
</tr>
<tr>
<td>$r_{DS(on)}$</td>
<td>Static drain-source on-state resistance</td>
<td>$</td>
<td>I_D</td>
<td>= 50 \text{ mA}$, $V_{CC} = 4.5 \text{ V}$</td>
<td>6.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$</td>
<td>I_D</td>
<td>= 50 \text{ mA}$, $T_C = 125^\circ C$, $V_{CC} = 4.5 \text{ V}$</td>
<td>See Notes 5 and 6 and Figures 7 and 8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$</td>
<td>I_D</td>
<td>= 100 \text{ mA}$, $V_{CC} = 4.5 \text{ V}$</td>
<td>6.8</td>
</tr>
</tbody>
</table>

**NOTES:**
3. Pulse duration ≤ 100 \mu s and duty cycle ≤ 2%.
5. Technique should limit $T_J$ – $T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at $T_C = 85^\circ C$. 
switching characteristics, $V_{CC} = 5V$, $T_C = 25^\circ C$

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLH}$</td>
<td>Propagation delay time, low-to-high-level output from $G$</td>
<td>80</td>
<td>ns</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>Propagation delay time, high-to-low-level output from $G$</td>
<td>20</td>
<td>ns</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{pd}$</td>
<td>Propagation delay time, SRCK to SEROUT</td>
<td>100</td>
<td>ns</td>
<td>80</td>
<td>ns</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Rise time, drain output</td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_f$</td>
<td>Fall time, drain output</td>
<td>120</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{a}$</td>
<td>Reverse-recovery-current rise time</td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{rr}$</td>
<td>Reverse-recovery time</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES: 5. Technique should limit $T_J - T_C$ to $10^\circ C$ maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal resistance

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\theta JA}$</td>
<td>Thermal resistance, junction-to-ambient</td>
<td>115</td>
<td>°C/W</td>
<td>108</td>
</tr>
</tbody>
</table>

NOTES: 5. Technique should limit $T_J - T_C$ to $10^\circ C$ maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50$ Ω.
B. $C_L$ includes probe and jig capacitance.

Figure 1. Resistive-Load Test Circuit and Voltage Waveforms
PARAMETER MEASUREMENT INFORMATION

NOTES: A. The word generator has the following characteristics: $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$, $t_w = 300 \text{ ns}$, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50 \Omega$.
B. $C_L$ includes probe and jig capacitance.

Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

NOTES: A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
B. The $V_{GG}$ amplitude and $R_G$ are adjusted for $\frac{di}{dt} = 10 \text{ A/µs}$. A $V_{GG}$ double-pulse train is used to set $I_F = 0.1 \text{ A}$, where $t_1 = 10 \text{ µs}$, $t_2 = 7 \text{ µs}$, and $t_3 = 3 \text{ µs}$.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode
PARAMETER MEASUREMENT INFORMATION

SINGLE-PULSE AVALANCHE ENERGY TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

NOTES:
A. The word generator has the following characteristics: \( t_r \leq 10 \, \text{ns}, \, t_f \leq 10 \, \text{ns}, \, Z_O = 50 \, \Omega \).

B. Input pulse duration, \( t_w \), is increased until peak current \( I_{AS} = 200 \, \text{mA} \).

Energy test level is defined as \( E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 30 \, \text{mJ} \).

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

Figure 5

Figure 6
TYPICAL CHARACTERISTICS

DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

\[ V_{CC} = 5 \text{ V} \]
Sees Note A

\[ T_C = 125^\circ \text{C} \]
\[ T_C = 25^\circ \text{C} \]
\[ T_C = -40^\circ \text{C} \]

Figure 7

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

\[ T_C = 125^\circ \text{C} \]
\[ T_C = 25^\circ \text{C} \]
\[ T_C = -40^\circ \text{C} \]

Figure 8

SWITCHING TIME vs CASE TEMPERATURE

\[ I_D = 75 \text{ mA} \]
Sees Note A

\[ t_PHL \]
\[ t_PLH \]
\[ t_r \]
\[ t_f \]

Figure 9

NOTE A: Technique should limit \( T_J - T_C \) to 10°C maximum.
THERMAL INFORMATION

MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT

vs

NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

\[ V_{CC} = 5 \, V \]

\[ T_C = 25^\circ C \]

\[ T_C = 100^\circ C \]

\[ T_C = 125^\circ C \]

\[ N \rightarrow \text{Number of Outputs Conducting Simultaneously} \]

\[ I_D \rightarrow \text{Maximum Continuous Drain Current of Each Output - A} \]

\[ d = \frac{t_w}{t_{\text{period}}} \]

\[ d = 10\% \]

\[ d = 20\% \]

\[ d = 50\% \]

\[ d = 80\% \]

Figure 10

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT

vs

NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

\[ V_{CC} = 5 \, V \]

\[ T_C = 25^\circ C \]

\[ d = \frac{t_w}{t_{\text{period}}} = 1 \, \text{ms}/\text{period} \]

\[ d = 10\% \]

\[ d = 20\% \]

\[ d = 50\% \]

\[ d = 80\% \]

Figure 11
THERMAL INFORMATION

D PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE

vs
PULSE DURATION

DC Conditions
- d = 0.5
- d = 0.2
- d = 0.1
- d = 0.05
- d = 0.02
- d = 0.01

Single Pulse
- R\textsubscript{θJA}

NOTES:
- Z\textsubscript{θA(t)} = r(t) R\textsubscript{θJA}
- t\textsubscript{w} = pulse duration
- t\textsubscript{c} = cycle time
- d = duty cycle = t\textsubscript{w}/t\textsubscript{c}

† Device mounted on FR4 printed-circuit board with no heat sink

Figure 12
## Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPIC6C595D</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>40</td>
<td>TBD</td>
<td>CU NIPDAU</td>
<td>Level-1-220C-UNLIM</td>
</tr>
<tr>
<td>TPIC6C595DG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
</tr>
<tr>
<td>TPIC6C595D</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>2500</td>
<td>TBD</td>
<td>CU NIPDAU</td>
<td>Level-1-220C-UNLIM</td>
</tr>
<tr>
<td>TPIC6C595DG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
</tr>
<tr>
<td>TPIC6C595N</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>N</td>
<td>16</td>
<td>25</td>
<td>Pb-Free (RoHS)</td>
<td>CU NIPDAU</td>
<td>N / A for Pkg Type</td>
</tr>
<tr>
<td>TPIC6C595PW</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>90</td>
<td>TBD</td>
<td>CU NIPDAU</td>
<td>Level-1-220C-UNLIM</td>
</tr>
<tr>
<td>TPIC6C595PWG4</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>90</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
</tr>
<tr>
<td>TPIC6C595PWR</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>2000</td>
<td>TBD</td>
<td>CU NIPDAU</td>
<td>Level-1-220C-UNLIM</td>
</tr>
<tr>
<td>TPIC6C595PWRG4</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PW (R-PDSO-G**)

**PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

**NOTES:**

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
D. Falls within JEDEC MO-153

<table>
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<tr>
<th>PINS **</th>
<th>DIM</th>
<th>8</th>
<th>14</th>
<th>16</th>
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<tr>
<td>A MAX</td>
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<td>3.10</td>
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<tr>
<td>A MIN</td>
<td></td>
<td>2.90</td>
<td>4.90</td>
<td>4.90</td>
<td>6.40</td>
<td>7.70</td>
<td>9.60</td>
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</tbody>
</table>
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
   △ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.005 (0.13) per end.
   △ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) per side.
E. Reference JEDEC MS-012 variation AC.
NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
**NOTES:**

A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

⚠️ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

⚠️ The 20 pin end lead shoulder width is a vendor option, either half or full width.
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