TDA8542
2 × 1 W BTL audio amplifier

Product specification
Supersedes data of 1997 Feb 19
File under Integrated Circuits, IC01
FEATURES

• Flexibility in use
• Few external components
• Low saturation voltage of output stage
• Gain can be fixed with external resistors
• Standby mode controlled by CMOS compatible levels
• Low standby current
• No switch-on/switch-off plops
• High supply voltage ripple rejection
• Protected against electrostatic discharge
• Outputs short-circuit safe to ground, \( V_{CC} \) and across the load
• Thermally protected.

APPLICATIONS

• Portable consumer products
• Personal computers
• Motor-driver (servo).

GENERAL DESCRIPTION

The TDA8542(T) is a two channel audio power amplifier for an output power of \( 2 \times 1 \) W with an 8 Ω load at a 5 V supply. The circuit contains two BTL amplifiers with a complementary PNP-NPN output stage and standby/mute logic. The TDA8542T comes in a 16 pin SO package and the TDA8542 in a 16 pin DIP package.

QUICK REFERENCE DATA

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CC} )</td>
<td>supply voltage</td>
<td></td>
<td>2.2</td>
<td>5</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>( I_q )</td>
<td>quiescent current</td>
<td>( V_{CC} = 5 ) V</td>
<td>–</td>
<td>15</td>
<td>22</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{stb} )</td>
<td>standby current</td>
<td>–</td>
<td>–</td>
<td>10</td>
<td>( \mu )A</td>
<td></td>
</tr>
<tr>
<td>( P_o )</td>
<td>output power</td>
<td>( \text{THD} = 10%; R_L = 8 ) Ω; ( V_{CC} = 5 ) V</td>
<td>1</td>
<td>1.2</td>
<td>–</td>
<td>W</td>
</tr>
<tr>
<td>THD</td>
<td>total harmonic distortion</td>
<td>( P_o = 0.5 ) W</td>
<td>–</td>
<td>0.15</td>
<td>–</td>
<td>%</td>
</tr>
<tr>
<td>SVRR</td>
<td>supply voltage ripple rejection</td>
<td></td>
<td>50</td>
<td>–</td>
<td>–</td>
<td>dB</td>
</tr>
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</table>

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>TYPE NUMBER</th>
<th>PACKAGE</th>
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<tbody>
<tr>
<td>TDA8542T</td>
<td>SO16L plastic small outline package; 16 leads; body width 7.5 mm</td>
</tr>
<tr>
<td>TDA8542</td>
<td>DIP16 plastic dual in-line package; 16 leads (300 mil); long body</td>
</tr>
</tbody>
</table>

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2 × 1 W BTL audio amplifier  

TDA8542

BLOCK DIAGRAM

Fig.1 Block diagram.
**PINNING**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PIN</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>LGND</td>
<td>1</td>
<td>ground, left channel</td>
</tr>
<tr>
<td>OUTL+</td>
<td>2</td>
<td>positive loudspeaker terminal, left channel</td>
</tr>
<tr>
<td>MODE</td>
<td>3</td>
<td>operating mode select (standby, mute, operating)</td>
</tr>
<tr>
<td>SVR</td>
<td>4</td>
<td>half supply voltage, decoupling ripple rejection</td>
</tr>
<tr>
<td>BTL/SE</td>
<td>5</td>
<td>BTL loudspeaker or SE headphone operation</td>
</tr>
<tr>
<td>n.c.</td>
<td>6</td>
<td>not connected</td>
</tr>
<tr>
<td>OUTR+</td>
<td>7</td>
<td>positive loudspeaker terminal, right channel</td>
</tr>
<tr>
<td>RGND</td>
<td>8</td>
<td>ground, right channel</td>
</tr>
<tr>
<td>VCCR</td>
<td>9</td>
<td>supply voltage, right channel</td>
</tr>
<tr>
<td>OUTR−</td>
<td>10</td>
<td>negative loudspeaker terminal, right channel</td>
</tr>
<tr>
<td>INR−</td>
<td>11</td>
<td>negative input, right channel</td>
</tr>
<tr>
<td>INR+</td>
<td>12</td>
<td>positive input, right channel</td>
</tr>
<tr>
<td>INL+</td>
<td>13</td>
<td>positive input, left channel</td>
</tr>
<tr>
<td>INL−</td>
<td>14</td>
<td>negative input, left channel</td>
</tr>
<tr>
<td>OUTL−</td>
<td>15</td>
<td>negative loudspeaker terminal, left channel</td>
</tr>
<tr>
<td>VCCl</td>
<td>16</td>
<td>supply voltage, left channel</td>
</tr>
</tbody>
</table>

**FUNCTIONAL DESCRIPTION**

The TDA8542(T) is a 2 × 1 W BTL audio power amplifier capable of delivering 2 × 1 W output power to an 8 Ω load at THD = 10% using a 5 V power supply. Using the MODE pin the device can be switched to standby and mute condition. The device is protected by an internal thermal shutdown protection mechanism. The gain can be set within a range from 6 dB to 30 dB by external feedback resistors.

**Power amplifier**

The power amplifier is a Bridge Tied Load (BTL) amplifier with a complementary PNP-NPN output stage. The voltage loss on the positive supply line is the saturation voltage of a PNP power transistor, on the negative side the saturation voltage of a NPN power transistor. The total voltage loss is <1 V and with a 5 V supply voltage and an 8 Ω loudspeaker an output power of 1 W can be delivered.

**Mode select pin**

The device is in the standby mode (with a very low current consumption) if the voltage at the MODE pin is > (VCC – 0.5 V), or if this pin is floating. At a MODE voltage level of less than 0.5 V the amplifier is fully operational. In the range between 1.5 V and VCC – 1.5 V the amplifier is in mute condition. The mute condition is useful to suppress plop noise at the output caused by charging of the input capacitor.

**Headphone connection**

A headphone can be connected to the amplifier using two coupling capacitors for each channel. The common GND pin of the headphone is connected to the ground of the amplifier (see Fig.13). In this case the BTL/SE pin must be either on a logic HIGH level or not connected at all. The two coupling capacitors can be omitted if it is allowed to connect the common GND pin of the headphone jack not to ground, but to a voltage level of $\frac{1}{2}V_{CC}$ (see Fig.13). In this case the BTL/SE pin must be either on a logic LOW level or connected to ground. If the BTL/SE pin is on a LOW level, the power amplifier for the positive loudspeaker terminal is always in mute condition.

**Fig.2 Pin configuration.**
LIMITING VALUES
In accordance with the Absolute Maximum Rating System (IEC 134).

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{CC}</td>
<td>supply voltage</td>
<td>operating</td>
<td>−0.3</td>
<td>+18</td>
<td>V</td>
</tr>
<tr>
<td>I_{i}</td>
<td>input voltage</td>
<td>−0.3</td>
<td>V_{CC} + 0.3 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{ORM}</td>
<td>repetitive peak output current</td>
<td>−</td>
<td>1</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>T_{stg}</td>
<td>storage temperature</td>
<td>non-operating</td>
<td>−55</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>T_{amb}</td>
<td>operating ambient temperature</td>
<td>−40</td>
<td>+85</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>V_{psc}</td>
<td>AC and DC short-circuit safe voltage</td>
<td>−</td>
<td>10</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>P_{tot}</td>
<td>total power dissipation</td>
<td>SO16L</td>
<td>−</td>
<td>1.2</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>DIP16</td>
<td></td>
<td>−</td>
<td>2.2</td>
<td>W</td>
</tr>
</tbody>
</table>

QUALITY SPECIFICATION
In accordance with “SNW-FO-611-E”. The number of the quality specification can be found in the “Quality Reference Handbook”. The handbook can be ordered using the code 9397 750 00192.

THERMAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{thj-a}</td>
<td>thermal resistance from junction to ambient in free air: TDA8542T (SO16L)</td>
<td>100</td>
<td>K/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>55</td>
<td>K/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
DC CHARACTERISTICS

$V_{CC} = 5\ V; \ T_{amb} = 25\ ^\circ C; \ R_L = 8\ \Omega; \ V_{MODE} = 0\ V$: measured in test circuit Fig.3; unless otherwise specified.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>supply voltage</td>
<td>operating</td>
<td>2.2</td>
<td>5</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>$I_q$</td>
<td>quiescent current</td>
<td>$R_L = \infty$; note 1</td>
<td>–</td>
<td>15</td>
<td>22</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{stb}$</td>
<td>standby current</td>
<td>$V_{MODE} = V_{CC}$</td>
<td>–</td>
<td>–</td>
<td>10</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$V_O$</td>
<td>DC output voltage</td>
<td>note 2</td>
<td>–</td>
<td>2.2</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>$</td>
<td>V_{OUT+} - V_{OUT-}</td>
<td>$</td>
<td>differential output voltage offset</td>
<td>–</td>
<td>–</td>
<td>50</td>
</tr>
<tr>
<td>$I_{IN+}, I_{IN-}$</td>
<td>input bias current</td>
<td>–</td>
<td>–</td>
<td>500</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>$V_{MODE}$</td>
<td>input voltage mode select</td>
<td>operating</td>
<td>0</td>
<td>–</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>mute</td>
<td>1.5</td>
<td>–</td>
<td>$V_{CC} - 1.5$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>standby</td>
<td>$V_{CC} - 0.5$</td>
<td>–</td>
<td>$V_{CC}$</td>
<td>V</td>
</tr>
<tr>
<td>$I_{MODE}$</td>
<td>input current mode select</td>
<td>$0 &lt; V_{MODE} &lt; V_{CC}$</td>
<td>–</td>
<td>–</td>
<td>20</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$V_{BS}$</td>
<td>input voltage BTL/SE pin</td>
<td>single-ended</td>
<td>0</td>
<td>–</td>
<td>0.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>BTL</td>
<td>2</td>
<td>–</td>
<td>$V_{CC}$</td>
<td>V</td>
</tr>
<tr>
<td>$I_{BS}$</td>
<td>input current BTL/SE pin</td>
<td>$V_{BS} = 0$</td>
<td>–</td>
<td>–</td>
<td>100</td>
<td>$\mu$A</td>
</tr>
</tbody>
</table>

Notes

1. With a load connected at the outputs the quiescent current will increase, the maximum of this increase being equal to the DC output offset voltage divided by $R_L$.
2. The DC output voltage with respect to ground is approximately $0.5 \times V_{CC}$.
AC CHARACTERISTICS

$V_{CC} = 5\, \text{V}; \ T_{amb} = 25^\circ\text{C}; \ R_L = 8\, \Omega; \ f = 1\, \text{kHz}; \ V_{MODE} = 0\, \text{V};$ measured in test circuit Fig.3; unless otherwise specified.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_o$</td>
<td>output power</td>
<td>THD = 10%</td>
<td>1</td>
<td>1.2</td>
<td>–</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>THD = 0.5%</td>
<td>0.6</td>
<td>0.9</td>
<td>–</td>
<td>W</td>
</tr>
<tr>
<td>THD</td>
<td>total harmonic distortion</td>
<td>$P_o = 0.5, \text{W}$</td>
<td>–</td>
<td>0.15</td>
<td>0.3</td>
<td>%</td>
</tr>
<tr>
<td>$G_v$</td>
<td>closed loop voltage gain</td>
<td>note 1</td>
<td>6</td>
<td>–</td>
<td>30</td>
<td>dB</td>
</tr>
<tr>
<td>$Z_i$</td>
<td>differential input impedance</td>
<td>–</td>
<td>100</td>
<td>–</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>$V_{no}$</td>
<td>noise output voltage</td>
<td>note 2</td>
<td>–</td>
<td>–</td>
<td>100</td>
<td>μV</td>
</tr>
<tr>
<td>SVRR</td>
<td>supply voltage ripple rejection</td>
<td>note 3</td>
<td>50</td>
<td>–</td>
<td>–</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>note 4</td>
<td>40</td>
<td>–</td>
<td>200</td>
<td>μV</td>
</tr>
<tr>
<td>$V_o$</td>
<td>output voltage in mute condition</td>
<td>note 5</td>
<td>–</td>
<td>–</td>
<td>200</td>
<td>μV</td>
</tr>
<tr>
<td>$\alpha_{cs}$</td>
<td>channel separation</td>
<td>–</td>
<td>40</td>
<td>–</td>
<td>–</td>
<td>dB</td>
</tr>
</tbody>
</table>

Notes

1. Gain of the amplifier is $2 \times R2/R1$ in test circuit of Fig.3.
2. The noise output voltage is measured at the output in a frequency range from 20 Hz to 20 kHz (unweighted), with a source impedance of $R_S = 0\, \Omega$ at the input.
3. Supply voltage ripple rejection is measured at the output, with a source impedance of $R_S = 0\, \Omega$ at the input.
   The ripple voltage is a sine wave with a frequency of 1 kHz and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.
4. Supply voltage ripple rejection is measured at the output, with a source impedance of $R_S = 0\, \Omega$ at the input.
   The ripple voltage is a sine wave with a frequency between 100 Hz and 20 kHz and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.
5. Output voltage in mute position is measured with a 1 V (RMS) input voltage in a bandwidth of 20 kHz, so including noise.
TEST AND APPLICATION INFORMATION

Test conditions

Because the application can be either Bridge-Tied Load (BTL) or Single-Ended (SE), the curves of each application are shown separately.

The thermal resistance = 55 K/W for the DIP16; the maximum sine wave power dissipation for $T_{amb} = 25 ^\circ C$ is:

\[
\frac{150 - 25}{55} = 2.3 \text{ W}
\]

For $T_{amb} = 60 ^\circ C$ the maximum total power dissipation is:

\[
\frac{150 - 60}{55} = 1.7 \text{ W}
\]

BTL application

$T_{amb} = 25 ^\circ C$ if not specially mentioned, $V_{CC} = 5 \text{ V}$, $f = 1 \text{ kHz}$, $R_L = 8 \Omega$, $G_v = 20 \text{ dB}$, audio band-pass 22 Hz to 22 kHz.

The BTL application diagram is illustrated in Fig.3.

The quiescent current has been measured without any load impedance. The total harmonic distortion as a function of frequency was measured with a low-pass filter of 80 kHz. The value of capacitor C3 influences the behaviour of the SVRR at low frequencies, increasing the value of C3 increases the performance of the SVRR.

The figure of the mode select voltage ($V_{ms}$) as a function of the supply voltage shows three areas: operating, mute and standby. It shows, that the DC-switching levels of the mute and standby respectively depends on the supply voltage level.

SE application

$T_{amb} = 25 ^\circ C$ if not specially mentioned, $V_{CC} = 7.5 \text{ V}$, $f = 1 \text{ kHz}$, $R_L = 4 \Omega$, $G_v = 20 \text{ dB}$, audio band-pass 22 Hz to 22 kHz.

The SE application diagram is illustrated in Fig.14.

If the BTL/SE pin (pin 5) is connected to ground, the positive outputs (pins 2 and 7) will be in mute condition with a DC level of $\frac{1}{2}V_{CC}$. When a headphone is used ($R_L \geq 25 \Omega$) the SE headphone application can be used without output coupling capacitors; load between negative output and one of the positive outputs (e.g. pin 2) as common pin.

Increasing the value of electrolytic capacitor C3 will result in a better channel separation. Because the positive output is not designed for high output current ($2 \times I_o$) at low load impedance ($\leq 16 \Omega$), the SE application with output capacitors connected to ground is advised. The capacitor value of C4/C5 in combination with the load impedance determines the low frequency behaviour. The THD as a function of frequency was measured using a low-pass filter of 80 kHz. The value of capacitor C3 influences the behaviour of the SVRR at low frequencies, increasing the value of C3 increases the performance of the SVRR.

General remark

The frequency characteristic can be adapted by connecting a small capacitor across the feedback resistor. To improve the immunity of HF radiation in radio circuit applications, a small capacitor can be connected in parallel with the feedback resistor (56 kΩ); this creates a low-pass filter.
BTL APPLICATION

Gain left = $2 \times \frac{R_2}{R_1}$

Gain right = $2 \times \frac{R_4}{R_3}$

Fig.3 BTL application.

Fig.4 $I_q$ as a function of $V_{CC}$.

Fig.5 THD as a function of $P_o$. 

1. $V_{CC} = 5 \text{ V}, R_L = 8 \Omega$.
2. $V_{CC} = 9 \text{ V}, R_L = 16 \Omega$.

f = 1 kHz, $G_v = 20 \text{ dB}$. 

RI = $\infty$. 

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Fig. 6  THD as a function of frequency.

Fig. 7  Channel separation as a function of frequency.

Fig. 8  SVRR as a function of frequency.

Fig. 9  $P_o$ as a function of $V_{CC}$. 

$P_o = 0.5 \, W$, $G_v = 20 \, dB$.
(1) $V_{CC} = 5 \, V$, $R_L = 8 \, \Omega$.
(2) $V_{CC} = 9 \, V$, $R_L = 16 \, \Omega$.

$V_{CC} = 5 \, V$, $V_o = 2 \, V$, $R_L = 8 \, \Omega$.
(1) $G_v = 30 \, dB$.
(2) $G_v = 20 \, dB$.
(3) $G_v = 6 \, dB$.

$V_{CC} = 5 \, V$, $V_o = 2 \, V$, $R_L = 8 \, \Omega$.
(1) THD = 10%, $R_L = 8 \, \Omega$.
(2) THD = 10%, $R_L = 16 \, \Omega$.
2 × 1 W BTL audio amplifier

Fig. 10 Worst case power dissipation as a function of $V_{CC}$.

(1) $R_L = 8 \, \Omega$.
(2) $R_L = 16 \, \Omega$.

Fig. 11 $P_{dis}$ as a function of $P_o$.

Sine wave of 1 kHz.
(1) $V_{CC} = 9 \, V$, $R_L = 16 \, \Omega$.
(2) $V_{CC} = 5 \, V$, $R_L = 8 \, \Omega$.

Fig. 12 $V_o$ as a function of $V_{ms}$.

Band-pass = 22 Hz to 22 kHz.
(1) $V_{CC} = 3 \, V$.
(2) $V_{CC} = 5 \, V$.
(3) $V_{CC} = 12 \, V$.

Fig. 13 $V_{ms}$ as a function of $V_P$.

standby
mute
operating
SE APPLICATION

Gain left = \( \frac{R_2}{R_1} \)
Gain right = \( \frac{R_4}{R_3} \)

Fig.14 Single-ended application.

\( f = 1 \text{ kHz}, G_v = 20 \text{ dB}. \)
(1) \( V_{CC} = 7.5 \text{ V}, R_L = 4 \Omega \).
(2) \( V_{CC} = 9 \text{ V}, R_L = 8 \Omega \).
(3) \( V_{CC} = 12 \text{ V}, R_L = 16 \Omega \).

Fig.15 THD as a function of \( P_o \).

\( P_o = 0.5 \text{ W}, G_v = 20 \text{ dB}. \)
(1) \( V_{CC} = 7.5 \text{ V}, R_L = 4 \Omega \).
(2) \( V_{CC} = 9 \text{ V}, R_L = 8 \Omega \).
(3) \( V_{CC} = 12 \text{ V}, R_L = 16 \Omega \).

Fig.16 THD as a function of frequency.
Philips Semiconductors

Product specification

$2 \times 1$ W BTL audio amplifier

TDA8542

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**Fig. 17** Channel separation as a function of frequency.

$V_o = 1 \text{ V, } G_v = 20 \text{ dB.}$

1. $V_{CC} = 5 \text{ V, } R_L = 32 \Omega$, to buffer.
2. $V_{CC} = 7.5 \text{ V, } R_L = 4 \Omega$.
3. $V_{CC} = 9 \text{ V, } R_L = 8 \Omega$.
4. $V_{CC} = 12 \text{ V, } R_L = 16 \Omega$.
5. $V_{CC} = 5 \text{ V, } R_L = 32 \Omega$.

---

**Fig. 18** SVRR as a function of frequency.

$V_{CC} = 7.5 \text{ V, } R_L = 4 \Omega, R_s = 0 \Omega, V_r = 100 \text{ mV.}$

1. $G_v = 24 \text{ dB.}$
2. $G_v = 20 \text{ dB.}$
3. $G_v = 0 \text{ dB.}$

---

**Fig. 19** $P_o$ as a function of $V_{CC}$.

THD = 10%.

1. $R_L = 4 \Omega$.
2. $R_L = 8 \Omega$.
3. $R_L = 16 \Omega$.

---

**Fig. 20** Worst case power dissipation as a function of $V_{CC}$.

1. $R_L = 4 \Omega$.
2. $R_L = 8 \Omega$.
3. $R_L = 16 \Omega$. 
Sine wave of 1 kHz.

1. $V_{CC} = 12$ V, $R_L = 16$ Ω.
2. $V_{CC} = 7.5$ V, $R_L = 4$ Ω.
3. $V_{CC} = 9$ V, $R_L = 8$ Ω.

Fig. 21  Power dissipation as a function of $P_o$. 
a. Top view.

b. Component side.

Fig.22 Printed-circuit board layout (BTL and SE).
PACKETAGE OUTLINES
SO16: plastic small outline package; 16 leads; body width 7.5 mm

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT      | A    | A1   | A2   | A3   | bP   | c    | D1   | E1   | e    | HE  | L    | Lp   | Q    | v    | w    | y    | z   |
|-----------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|-----|-----|
| mm        | 2.65 | 0.30 | 2.45 | 0.25 | 0.65 | 0.65 | 7.6  | 10.0 | 1.4  | 0.25 | 0.10 | 0.10 |
| inches    | 0.10 | 0.01 | 0.04 | 0.01 | 0.09 | 0.09 | 0.41 | 0.41 | 0.41 | 0.41 | 0.41 | 0.41 |

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION

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2 × 1 W BTL audio amplifier TDA8542

DIP16: plastic dual in-line package; 16 leads (300 mil); long body SOT38-1

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<th>A2 max.</th>
<th>b</th>
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Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION

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1998 Apr 01
SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our “IC Package Databook” (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature (T_{stg\_max}). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.
2 × 1 W BTL audio amplifier

DEFINITIONS

Data sheet status

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<th>Specification Type</th>
<th>Description</th>
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<td>Objective specification</td>
<td>This data sheet contains target or goal specifications for product development.</td>
</tr>
<tr>
<td>Preliminary specification</td>
<td>This data sheet contains preliminary data; supplementary data may be published later.</td>
</tr>
<tr>
<td>Product specification</td>
<td>This data sheet contains final product specifications.</td>
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</table>

Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.