Overview

The LA4485 is a 5 W, two-channel power amplifier IC that requires a minimum of external parts, making it ideal for radio cassette players and car stereo equipment.

The LA4485 eliminates the need for bootstrap capacitors, negative feedback capacitors, and oscillation prevention CR parts, all of which were necessities for power ICs previously. All of these functions are now on chip, keeping the number of external parts to an absolute minimum. The LA4485 is part of the Power (Stylish Power) Series, and supports two modes: dual and BTL.

Features

- 5 W × 2 output power in dual mode, and 15 W in BTL mode
- Minimum external parts for the Power Series count: 4 or 5 parts in dual mode; 3 or 4 parts in BTL mode
- Protection circuits
  - Overvoltage protection
  - Thermal protection
  - DC output short-circuit protection (to VCC and to GND)
- Circuitry designed to handle +VCC applied to the outputs
- Pop noise reduction
- Standby switch
- Muting function

Specifications

**Maximum Ratings at Ta = 25°C**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum supply voltage</td>
<td>VCC max</td>
<td>No signal</td>
<td>24</td>
<td>V</td>
</tr>
<tr>
<td>Surge supply voltage</td>
<td>VCC surge</td>
<td>Based on the JASO standard</td>
<td>50</td>
<td>V</td>
</tr>
<tr>
<td>Peak output current</td>
<td>I0 peak</td>
<td>Per channel</td>
<td>3.3</td>
<td>A</td>
</tr>
<tr>
<td>Allowable power dissipation</td>
<td>Pd max</td>
<td>With infinite heat sink</td>
<td>15</td>
<td>W</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>Topr</td>
<td></td>
<td>−30 to +80</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>Tstg</td>
<td></td>
<td>−40 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

*: By the π type B check point method.

---

**Notes**

- Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft’s control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.

- SANYO assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO products described or contained herein.
### Operating Conditions at Ta = 25°C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Recommended supply voltage</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td></td>
<td>13.2</td>
<td>V</td>
</tr>
<tr>
<td>Supply voltage range</td>
<td>V&lt;sub&gt;CC op&lt;/sub&gt;</td>
<td>Must not be over package P&lt;sub&gt;d&lt;/sub&gt;</td>
<td>7.5 to 18</td>
<td>V</td>
</tr>
<tr>
<td>Recommended load resistance range</td>
<td>R&lt;sub&gt;L&lt;/sub&gt;</td>
<td>Dual, BTL</td>
<td>2 to 8</td>
<td>Ω</td>
</tr>
</tbody>
</table>

### Operating Characteristics at Ta = 25°C, V<sub>CC</sub> = 13.2 V, R<sub>L</sub> = 4 Ω, R<sub>g</sub> = 600 Ω, f = 1 kHz, Dual

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standby current</td>
<td>I&lt;sub&gt;st&lt;/sub&gt;</td>
<td>Pin 9 to GND, Standby switch OFF</td>
<td>10</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Quiescent supply current</td>
<td>I&lt;sub&gt;CCO&lt;/sub&gt;</td>
<td>R&lt;sub&gt;g&lt;/sub&gt; = 0</td>
<td>40</td>
<td>80</td>
<td>160</td>
<td>mA</td>
</tr>
<tr>
<td>Voltage gain</td>
<td>V&lt;sub&gt;G1&lt;/sub&gt;</td>
<td>Dual: V&lt;sub&gt;O&lt;/sub&gt; = 0 dBm</td>
<td>43</td>
<td>45</td>
<td>47</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;G2&lt;/sub&gt;</td>
<td>BTL: V&lt;sub&gt;O&lt;/sub&gt; = 0 dBm</td>
<td></td>
<td>51</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Output power</td>
<td>P&lt;sub&gt;O1&lt;/sub&gt;</td>
<td>Dual: THD = 10%</td>
<td>4</td>
<td>5</td>
<td></td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>P&lt;sub&gt;O2&lt;/sub&gt;</td>
<td>BTL: THD = 10%</td>
<td>11</td>
<td>15</td>
<td></td>
<td>W</td>
</tr>
<tr>
<td>Total harmonic distortion</td>
<td>THD</td>
<td>P&lt;sub&gt;O&lt;/sub&gt; = 1 W</td>
<td>0.15</td>
<td>0.8</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Channel separation</td>
<td>CH sep</td>
<td>V&lt;sub&gt;O&lt;/sub&gt; = 0 dBm, R&lt;sub&gt;g&lt;/sub&gt; = 0</td>
<td>45</td>
<td>55</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Output noise voltage</td>
<td>V&lt;sub&gt;N0&lt;/sub&gt;</td>
<td>R&lt;sub&gt;g&lt;/sub&gt; = 0, 20 Hz to 20 kHz bandpass filter</td>
<td>0.15</td>
<td>0.5</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Ripple rejection ratio</td>
<td>SVRR</td>
<td>R&lt;sub&gt;g&lt;/sub&gt; = 0, 20 Hz to 20 kHz bandpass filter, f&lt;sub&gt;R&lt;/sub&gt; = 100 Hz, V&lt;sub&gt;R&lt;/sub&gt; = 0 dBm, decoupling capacitor connected</td>
<td>40</td>
<td>50</td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

*: P<sub>O1</sub> = 6 W (typ) when V<sub>CC</sub> = 14.4 V

V<sub>Off</sub> ± 250 mV for BTL-mode

![Graph showing allowable power dissipation, P<sub>d max</sub> vs Ambient temperature, Ta = °C](attachment:image.png)
Equivalent Circuit Block Diagram

Recommended LA4485 External Parts Arrangement (Dual-mode)
IC Usage Notes

Maximum ratings

Care must be taken when operating the LA4485 close to the maximum ratings as small changes in the operating conditions can cause the maximum ratings to be exceeded, thereby breakdown will be caused.

Printed circuit board connections

Care must be taken when designing the circuit of printed board so as not to form feedback loops, particularly with the small-signal and large-signal ground connections.

Notes on LA4485 heatsink mounting

1. Mounting torque must be in the range 39 to 59 N·cm.
2. The spacing of the tapped holes in the heatsink must match the spacing of the holes in the IC tab.
3. Use screws with heads equivalent to truss head machine screws and binding head machine screws stipulated by JIS for the mounting screws. Furthermore, washers must be used to protect the surface of the IC tab.
4. Make sure that there is no foreign matter, such as cutting debris, between the IC tab and the heatsink. If a heat conducting compound is applied between the contact surfaces, make sure that it is spread uniformly over the entire surface.
5. Because the heatsink mounting tab and the heatsink are at the same electric potential as the chip’s GND (large signal GND), care must be taken when mounting the heatsink on more than one device.
6. The heatsink must be mounted before soldering the pins to the PCB.

Comparison of External Parts Required

<table>
<thead>
<tr>
<th>External parts</th>
<th>Existing device</th>
<th>LA4485</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output coupling capacitors</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Input coupling capacitors</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Bootstrap capacitors</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Feedback capacitors</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Filter capacitor</td>
<td>Yes</td>
<td>Optional</td>
</tr>
<tr>
<td>Phase compensating capacitor</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Oscillation-quenching mylar capacitors</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Oscillation-quenching resistors</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Others</td>
<td>No</td>
<td>Optional</td>
</tr>
<tr>
<td>Total (for dual-mode)</td>
<td>15 to 16 parts</td>
<td>4 to 6 parts</td>
</tr>
</tbody>
</table>

Note: Supply capacitors, contained within the power IC, are not counted in both existing and new devices.
### Operating Pin Voltages at $V_{CC} = 13.2$ V

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Function</th>
<th>Pin voltage (Reference value)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CH1 IN</td>
<td>Channel 1 input.</td>
<td>1.4 V (2 $V_{BE}$)</td>
</tr>
<tr>
<td>2</td>
<td>CH2 IN</td>
<td>Channel 2 input.</td>
<td>1.4 V (2 $V_{BE}$)</td>
</tr>
<tr>
<td>3</td>
<td>SS GND</td>
<td>Small-signal ground</td>
<td>0 V</td>
</tr>
<tr>
<td>4</td>
<td>BTL IN</td>
<td>BTL-mode feedback input.</td>
<td>45 mV</td>
</tr>
<tr>
<td>5</td>
<td>BTL OUT</td>
<td>BTL-mode feedback output.</td>
<td>3.1 V ($\approx 1/4 V_{CC}$)</td>
</tr>
<tr>
<td>6</td>
<td>FILTER</td>
<td>Filter capacitor connection.</td>
<td>6.6 V ($\approx 1/2 V_{CC}$)</td>
</tr>
<tr>
<td>7</td>
<td>LS $V_{CC}$</td>
<td>Large-signal supply</td>
<td>13.2 V ($V_{CC}$)</td>
</tr>
<tr>
<td>8</td>
<td>SS $V_{CC}$</td>
<td>Small-signal supply</td>
<td>13.2 V ($V_{CC}$)</td>
</tr>
<tr>
<td>9</td>
<td>STANDBY</td>
<td>Standby control input.</td>
<td>5 V</td>
</tr>
<tr>
<td>10</td>
<td>MUTE</td>
<td>Mute control input.</td>
<td>0 V</td>
</tr>
<tr>
<td>11</td>
<td>CH2 OUT</td>
<td>Channel 2 output.</td>
<td>6.3 V</td>
</tr>
<tr>
<td>12</td>
<td>LS GND</td>
<td>Large-signal ground</td>
<td>0 V</td>
</tr>
<tr>
<td>13</td>
<td>CH1 OUT</td>
<td>Channel 1 output.</td>
<td>6.3 V</td>
</tr>
</tbody>
</table>

Note: Each pin is so arranged lest the IC should be broken even if inserted reversely.

### LA4485 Sample Application Circuit
**Output pin voltage, \( V_{N-V} \)**

- \( V_{CC} = 7.5 \text{ V} \) Cutoff for waveform carrying signal
- Overvoltage cutoff

**Supply voltage, \( V_{CC-V} \)**

- \( V_{CC} = 7.5 \text{ V} \)

**Standby current, \( I_{\text{st}} \)**

- \( V_{CC} = 7.5 \text{ V} \)
- \( C_{VCC} = 0.15 \mu\text{F (mylar)} \)
- \( R_{g} = 0 \) Standby to GND

**Output power, \( P_{O} \)**

- \( V_{CC} = 13.2 \text{ V} \)
- \( R_{L} = 4 \Omega \)
- \( f = 1 \text{ kHz} \)
- \( R_{g} = 600 \Omega \)
- \( P_{0} = 1 \text{ W} \)

**Total harmonic distortion, \( \text{THD} \)**

- \( V_{CC} = 13.2 \text{ V} \)
- \( R_{L} = 4 \Omega \)
- \( R_{g} = 600 \Omega \)
- \( P_{0} = 1 \text{ W} \)

**Response – dB**

- \( C_{0} = 1000 \mu\text{F} \)
- \( f_{H} = 160 \text{ kHz} \)

**Input voltage, \( V_{IN} \)**

- \( V_{CC} = 7.5 \text{ V} \)
- \( R_{L} = 4 \Omega \)
- \( f = 1 \text{ kHz} \)
- \( R_{g} = 600 \Omega \)
- \( V_{0} = 0 \text{ dBm} \)

**Cutoff for waveform carrying signal**

**Muting on**

**Supply voltage, \( V_{CC-V} \)**

- \( V_{CC} = 7.5 \text{ V} \)
- \( C_{VCC} = 0.15 \mu\text{F (mylar)} \)
- \( R_{g} = 0 \) Standby to GND

**Standby current, \( I_{\text{st}} \)**

- \( V_{CC} = 7.5 \text{ V} \)
- \( C_{VCC} = 0.15 \mu\text{F (mylar)} \)
- \( R_{g} = 0 \) Standby to GND

**Output power, \( P_{O} \)**

- \( V_{CC} = 13.2 \text{ V} \)
- \( R_{L} = 4 \Omega \)
- \( f = 1 \text{ kHz} \)
- \( R_{g} = 600 \Omega \)
- \( P_{0} = 1 \text{ W} \)

**Total harmonic distortion, \( \text{THD} \)**

- \( V_{CC} = 13.2 \text{ V} \)
- \( R_{L} = 4 \Omega \)
- \( R_{g} = 600 \Omega \)
- \( P_{0} = 1 \text{ W} \)

**Response – dB**

- \( C_{0} = 1000 \mu\text{F} \)
- \( f_{H} = 160 \text{ kHz} \)

**Supply voltage, \( V_{CC-V} \)**

- \( V_{CC} = 7.5 \text{ V} \)
- \( C_{VCC} = 0.15 \mu\text{F (mylar)} \)
- \( R_{g} = 0 \) Standby to GND

**Standby current, \( I_{\text{st}} \)**

- \( V_{CC} = 7.5 \text{ V} \)
- \( C_{VCC} = 0.15 \mu\text{F (mylar)} \)
- \( R_{g} = 0 \) Standby to GND

**Output power, \( P_{O} \)**

- \( V_{CC} = 13.2 \text{ V} \)
- \( R_{L} = 4 \Omega \)
- \( f = 1 \text{ kHz} \)
- \( R_{g} = 600 \Omega \)
- \( P_{0} = 1 \text{ W} \)

**Total harmonic distortion, \( \text{THD} \)**

- \( V_{CC} = 13.2 \text{ V} \)
- \( R_{L} = 4 \Omega \)
- \( R_{g} = 600 \Omega \)
- \( f = 1 \text{ kHz} \)
- \( P_{0} = 1 \text{ W} \)
**LA4485**

- **Output power, \( P_O \) – W**
- **Supply voltage, \( V_{CC} \) – V**
- **Current drain, \( I_{CC} \) (2CH) – A**
- **Output power, \( P_O \) (1CH) – W**

**Power dissipation, \( P_d \) (2CH) – W**

- Dual \( R_L = 2 \Omega \)
- Dual \( R_L = 3 \Omega \)
- Dual \( R_L = 4 \Omega \)
- Dual \( R_L = 6 \Omega \)
- Dual \( R_L = 8 \Omega \)

**Allowable power dissipation, \( P_{d \ max} \) – W**

- Dual \( R_L = 2 \Omega \)
- Dual \( R_L = 4 \Omega \)
- Dual \( R_L = 6 \Omega \)
- Dual \( R_L = 8 \Omega \)

**Supply voltage, \( V_{CC} \) – V**

- THD = 10%
- \( f = 1 \text{ kHz} \)

- \( P_d \) vs \( P_O \)
- \( V_{CC} = 16V, 15V, 14V, 13.2V, 12V, 10V \)

- \( P_{d \ max} \) vs \( V_{CC} \)
- \( R_L = 2 \Omega, 4 \Omega, 6 \Omega, 8 \Omega \)
- \( Ta = 25°C \)
Leakage from CH2 to CH1
Leakage from CH1 to CH2

Channel separation, CH sep – dB

Frequency, f – Hz

SVRR – V R
Ripple rejection ratio, SVRR – dB
Supplementary ripple voltage, V R – mV

SVRR – V CC
Ripple rejection ratio, SVRR – dB
Supply voltage, V CC – V

SVRR – f R
Ripple rejection ratio, SVRR – dB
Ripple frequency, f R – Hz

ICCO – T a
Quiescent current, ICCO – mA
Ambient temperature, T a – °C

P O – T a
Output power, P O – W
Ambient temperature, T a – °C

V N – T a
Output pin voltage, V N – V
Ambient temperature, T a – °C

V NO – R g
Output noise voltage, V NO – mV
Source resistance, Rg – Ω

Temperature characteristic due to output capacitor
C O = 1000 µF

LA4485
No.3680-8/21
V_{CC} = 13.2 V, standby supply +5 V,
R_L = 4 \, \Omega, \, R_g = 0
Main switch ON/OFF test

V_{CC} = 13.2 V, standby supply +5 V,
R_L = 4 \, \Omega, \, R_g = 0
Standby switch ON/OFF test

\rightarrow \text{Switching noise decreases as } C_{IN} = 0.22 \, \mu F \text{ (Input) is increased. (ex. } 2.2 \, \mu F)\

V_{CC} = 13.2 V,
R_L = 4 \, \Omega,
R_g = 600 \, \Omega,
THD = 10\%,
f = 1 \, kHz,
Output DC waveform
## Dual-mode Operation Notes

- Use the input capacitor $C_{IN}$ in the range of 0.22 µF to 1.0 µF.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$C_{IN} = 0.22$ µF</th>
<th>$C_{IN} = 1.0$ µF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start-up time (ts)</td>
<td>0.15 s</td>
<td>0.25 s</td>
</tr>
<tr>
<td>Attack noise when using the muting function</td>
<td>Somewhat noticeable</td>
<td>Good</td>
</tr>
</tbody>
</table>

Speaker turn-ON transient noise increased significantly when $C_{IN}$ is 2.2 µF or greater.

- The DC (filter) capacitor should be 100 µF or greater.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>100 µF or less</th>
<th>100 µF or more</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ripple rejection ratio (SVRR)</td>
<td>Somewhat worse 40 dB</td>
<td>Good 50 dB</td>
</tr>
<tr>
<td>$V_N$ rise rate when main or standby is turned &quot;on&quot;</td>
<td>Fast</td>
<td>Slow</td>
</tr>
</tbody>
</table>

Note:
*1. Slow as a result of natural discharge.
*2. Approximately 0.3 seconds as a result of forced discharge.

- Use the standby supply capacitor in the range of 0.22 µF to 0.47 µF.
  The $V_N$ trace for standby OFF changes and speaker turn-ON transient noise is increased significantly when the capacitor is 1 µF or greater. If the standby function is not used, this capacitor must be removed and pin 9 must be pulled up to the power supply.

- The output capacitor’s recommended value for $C_O$ is 1,000 µF.
  Smaller capacitance will worsen the roll-off frequency $f_L$ and $P_O$ in a low range.

- The recommended power supply capacitor is approximately 2,200 µF, but other capacitors than 2,200 µF can be used according to the application’s design.
  Using a capacitor with this value, the load on the supply can be as high as 56 Ω while still providing good supply stability during momentary supply glitches. Note that using a 0.15 µF capacitor can cause oscillations if the supply impedance increases. (Example: Mild oscillation results if the power supply capacitor is open.)

- **STANDBY** pin 9 IC internal circuit

- **MUTE** pin 10 IC internal circuit

---

No.3680-10/21
• Input pin 1/2 IC internal circuit

• Output pin 11/13 IC internal circuit

• The minimum configuration for dual-mode operation
* Insert capacitors of 1000 pF between each input and ground to prevent external noise.

* When the load (R_L) or the supply voltage (V_{CC}) is increased, turning the standby switch or the main switch on under strong input conditions will activate the IC’s internal pseudo ASO protection circuit for the upper power transistor (V_{CE} \times I_{CP}). This causes output oscillations or intermittent operation (The reference area is shown in Figure 1 below). However, strong input tests after the bias has stabilized have no problems. They also protect the upper power transistors close to the limits of ASO when all signal switches are on. Therefore, when using this IC under these conditions, the circuit design should obey the following condition:
  
  \[ \text{Signal generation time} > \text{Start-up time of the power amplifier IC} \]

or some other method of attaining the zero-volume condition should be adopted.

* An undervoltage protection circuit operates when the voltage is 7.5 V or lower.

---

**Figure 1**

This figure shows the pseudo ASO protection area when strong signal is input, and switch is ON: the upper power transistors have an area where V_{CE} \times I_{CP} load is caused.

Strong signal input after switch-ON is OK.

In BTL-mode operation, the load is R_L \times 2

Input voltage, V_{IN} - mV rms

Supply voltage, V_{CC} - V
i) The operating conditions for the PHOTO-1 series in dual mode are $V_{CC} = 13.2$ V, $R_L = 2$ Ω, $f = 1$ kHz, $V_{IN} = 50$ mV and standby switch ON.

"X-Y path observed within the normal area": checking each channel

```
Output waveforms
```

```
Current and voltage waveforms
```

```
Transition
```

```
Stabilization
```

```
Power transistor
```

```
Plot each point on the power transistor ASO curve. Refer to Figure 2.
```

```
Upper power transistor
```
The load line becomes more closely aligned with the vertical axis because of the load.

Figure 2
ii) The operating conditions for the PHOTO-2 in dual mode are $V_{CC} = 15\, \text{V}$, $R_L = 3\, \Omega$, $f = 1\, \text{kHz}$, $V_{IN} = 100\, \text{mV}$ and standby switch ON.

“X-Y path observed within the normal area”

Output waveforms

Transition

Stabilization

Current and voltage waveforms

Power transistor CE voltage – $V$

* Plot each point on the power transistor ASO curve. Refer to Figure 3.

Figure 3
LA4485, BTL Sample Application Circuit

![Circuit Diagram](image)

**Graphs:**
- **PO - VIN**: Output power (PO - W) vs. Input voltage (VIN - mV)
  - BTL: VCC=13.2V, RL=4Ω, f=1kHz, Rg=600Ω
- **THD - PO**: Total harmonic distortion (THD - %) vs. Output power (PO - W)
  - BTL: VCC=13.2V, RL=4Ω, f=1kHz

---

No.3680-15/21
LA4485

V_{CC} = 13.2 V, standby +5 V, 
R_{L} = 4 \Omega, R_{g} = 0
Main switch ON/OFF test

V_{CC} = 13.2 V, standby +5 V, 
R_{L} = 4 \Omega, R_{g} = 0
Standby switch ON/OFF test

Note: Switching noise decreases as 
C_{IN} = 0.22 \mu F (input) is increased. (ex. 2.2 \mu F)

V_{CC} = 13.2 V, 
R_{L} = 4 \Omega, 
R_{g} = 0
Mute ON/OFF

Output DC waveform
BTL-mode Operation Notes

In BTL mode, channel 1 should be non-inverted and channel 2 should be inverted.

- Use the input capacitor \( C_{IN} \) in the range 0.22 \( \mu \)F to 2.2 \( \mu \)F.
- Use the standby supply capacitor in the range 0.22 \( \mu \)F to 1.0 \( \mu \)F.

When the capacitor is 2.2 \( \mu \)F or more, the \( V_N \) trace for standby-off changes, and the switching noise increases significantly.

- The recommended DC (filter) capacitor is 100 \( \mu \)F or greater.
- The BTL-mode coupling capacitor should be 2.2 \( \mu \)F.

When this capacitor is decreased, the output power is decreased. However, when this capacitor is increased, speaker turn-ON transient noise is increased significantly.

- In BTL mode, the ripple rejection ratio (SVRR) is approximately 40 dB.

This is because the output ripple portion of the noninverted side penetrates the BTL coupling end, so that ripple on the inverted side is large. The following method is described as one external measure:

![Circuit Diagram](Image)

This measure yields an SVRR of approximately 50 dB. Note that the Rx loss voltage is approximately 1 V, and the \( P_O \) loss is about 1.0 to 1.5 W (to the 15 W level).

- Example of minimum parts for BTL operation

![Circuit Diagram](Image)

Dual-mode short-circuit test circuit

![Circuit Diagram](Image)

1. Load short-circuit (to ground)
2. Output-to-supply short-circuit
3. Output-to-ground short-circuit
Taking BTL coupling into consideration, the output-to-supply/output-to-ground protector is two-sided in order to protect both the IC and the speaker.

When using this method (simultaneously shorting the outputs to supply and to ground), in BTL mode, the IC protection function works even in noninverted output → output-to-supply mode, inverted output → output-to-ground mode. (The reverse is also OK.)

**Reference Value**

(a) Short-circuit test for dual-mode operation after the main and standby switches are turned ON.

Conditions:
1. \( V_{CC} = 10 \text{ to } 16 \text{ V}, R_L = 4 \Omega \) and \( P_O = 1 \text{ to } 5 \text{ W} \) (variable) for load short-circuit
2. \( V_{CC} = 10 \text{ to } 16 \text{ V}, R_L = 4 \Omega, R_g = 0 \) (no signal) for output-to-supply short-circuit
3. \( V_{CC} = 10 \text{ to } 16 \text{ V}, R_L = 4 \Omega, R_g = 0 \) (no signal) for output-to-ground short-circuit.

Z: impedance  ○: no device breakdown

<table>
<thead>
<tr>
<th>① Load short-circuit</th>
<th>② Output-to-supply short-circuit</th>
<th>③ Output-to-ground short-circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>One-time test</td>
<td>Repeated switching test</td>
<td>One-time test</td>
</tr>
<tr>
<td>Z = 0</td>
<td>Z = 0.5 Ω</td>
<td>Z = 0</td>
</tr>
<tr>
<td>○</td>
<td>○</td>
<td>○</td>
</tr>
<tr>
<td>Z = 0</td>
<td>Z = 0.5 Ω</td>
<td>Z = 0.5 Ω</td>
</tr>
<tr>
<td>○</td>
<td>○</td>
<td>○</td>
</tr>
<tr>
<td>Z = 0</td>
<td>Z = 0.5 Ω</td>
<td>Z = 0</td>
</tr>
<tr>
<td>○</td>
<td>○</td>
<td>○</td>
</tr>
<tr>
<td>Z = 0.5 Ω</td>
<td>Z = 0</td>
<td>Z = 0.5 Ω</td>
</tr>
<tr>
<td>○</td>
<td>○</td>
<td>○</td>
</tr>
</tbody>
</table>

(b) Short-circuit test for dual-mode operation (opposite flow of (a)) after the main and standby switches are turned ON.

Conditions: same as (a)  ○: No device breakdown

<table>
<thead>
<tr>
<th>① Load short-circuit</th>
<th>② Output-to-supply short-circuit</th>
<th>③ Output-to-ground short-circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>One-time test</td>
<td>Repeated switching test</td>
<td>One-time test</td>
</tr>
<tr>
<td>Z = 0</td>
<td>Z = 0.5 Ω</td>
<td>Z = 0</td>
</tr>
<tr>
<td>○</td>
<td>○</td>
<td>○</td>
</tr>
<tr>
<td>Z = 0</td>
<td>Z = 0.5 Ω</td>
<td>Z = 0.5 Ω</td>
</tr>
<tr>
<td>○</td>
<td>○</td>
<td>○</td>
</tr>
<tr>
<td>Z = 0</td>
<td>Z = 0.5 Ω</td>
<td>Z = 0</td>
</tr>
<tr>
<td>○</td>
<td>○</td>
<td>○</td>
</tr>
<tr>
<td>Z = 0.5 Ω</td>
<td>Z = 0</td>
<td>Z = 0.5 Ω</td>
</tr>
<tr>
<td>○</td>
<td>○</td>
<td>○</td>
</tr>
</tbody>
</table>

(Note) Shorting the outputs to ground when muting is active can result in device breakdown.

**BTL-mode short-circuit test circuit**
Reference Value

(a) Short-circuit test for BTL-mode operation after the main and standby switches are turned ON.

Conditions:
1. \( V_{CC} = 10 \text{ to } 16 \text{ V}, R_L = 4 \ \Omega \text{ and } P_O = 1 \text{ to } 15 \text{ W (variable) for load short-circuit} \)
2. \( V_{CC} = 10 \text{ to } 16 \text{ V}, R_L = 4 \ \Omega, R_g = 0 \text{ (no signal) for output-to-supply short-circuit} \)
3. \( V_{CC} = 10 \text{ to } 16 \text{ V}, R_L = 4 \ \Omega, R_g = 0 \text{ (no signal) for output-to-ground short-circuit} \).

Z: impedance  ○: no device breakdown

<table>
<thead>
<tr>
<th>Load short-circuit</th>
<th>Output-to-supply short-circuit</th>
<th>Output-to-ground short-circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>One-time test</td>
<td>Repeated switching test</td>
<td>One-time test</td>
</tr>
<tr>
<td>( Z = 0 )</td>
<td>( Z = 0 )</td>
<td>( Z = 0 )</td>
</tr>
<tr>
<td>( Z = 0.5 \ \Omega )</td>
<td>( Z = 0.5 \ \Omega )</td>
<td>( Z = 0.5 \ \Omega )</td>
</tr>
</tbody>
</table>

(b) Short-circuit test for BTL-mode operation (opposite flow of (a)) after the main and standby switches are turned ON.

Conditions: same as (a)  ○: No device breakdown

<table>
<thead>
<tr>
<th>Load short-circuit</th>
<th>Output-to-supply short-circuit</th>
<th>Output-to-ground short-circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>One-time test</td>
<td>Repeated switching test</td>
<td>One-time test</td>
</tr>
<tr>
<td>( Z = 0 )</td>
<td>( Z = 0 )</td>
<td>( Z = 0 )</td>
</tr>
<tr>
<td>( Z = 0.5 \ \Omega )</td>
<td>( Z = 0.5 \ \Omega )</td>
<td>( Z = 0.5 \ \Omega )</td>
</tr>
</tbody>
</table>

(Note) Shorting the outputs to ground when muting is active can result in device breakdown.

* Power supply positive surge

The power supply line positive surge breakdown margin has been increased by using the built-in overvoltage protection circuits \( (V_{CCX} = 28 \text{ V}) \) to cut off all bias circuits/change the base-emitter reverse of the output stage. In other words, the breakdown margin is being raised by changing output stage groups that operate as the \( V_{CEO} (V_{CER}) \) type to the \( V_{CES} (V_{CBO}) \) type.
Test of application of $+V_{CC}$ to output pins

If the power supply pin is floating under the power supply capacitor insertion conditions, and $+V_{CC}$ comes into contact with output lines (a) and (b) as shown in the diagram above, the IC’s internal upper power transistor will generally be damaged. The LA4485 has a protective bypass circuit on chip. However, it is dangerous if the power supply capacitor is greater than 2200 µF.

Specifications of any and all SANYO products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer’s products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer’s products or equipment.

SANYO Electric Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.

In the event that any or all SANYO products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.

No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Electric Co., Ltd.

Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the “Delivery Specification” for the SANYO product that you intend to use.

Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of July, 1996. Specifications and information herein are subject to change without notice.