CMOS Voltage Converters

The Intersil ICL7660 and ICL7660A are monolithic CMOS power supply circuits which offer unique performance advantages over previously available devices. The ICL7660 performs supply voltage conversions from positive to negative for an input range of +1.5V to +10.0V resulting in complementary output voltages of -1.5V to -10.0V and the ICL7660A does the same conversions with an input range of +1.5V to +12.0V resulting in complementary output voltages of -1.5V to -12.0V. Only 2 noncritical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7660 and ICL7660A can also be connected to function as voltage doublers and will generate output voltages up to +18.6V with a +10V input.

Contained on the chip are a series DC supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. A unique logic element senses the most negative voltage in the device and ensures that the output N-Channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0V. This frequency can be lowered by the addition of an external capacitor to the “OSC” terminal, or the oscillator may be overdriven by an external clock.

The “LV” terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5V to +10.0V for the ICL7660 and +3.5V to +12.0V for the ICL7660A), the LV pin is left floating to prevent device latchup.

Ordering Information

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>TEMP. RANGE (°C)</th>
<th>PACKAGE</th>
<th>PKG. NO.</th>
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<td>ICL7660CBA</td>
<td>0 to 70</td>
<td>8 Ld SOIC (N)</td>
<td>M8.15</td>
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<tr>
<td>ICL7660CBA-T</td>
<td>0 to 70</td>
<td>8 Ld SOIC (N) Tape and Reel</td>
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<tr>
<td>ICL7660CPA</td>
<td>0 to 70</td>
<td>8 Ld PDIP</td>
<td>E8.3</td>
</tr>
<tr>
<td>ICL7660MTV†</td>
<td>0 to 70</td>
<td>8 Pin Metal Can</td>
<td>T8.C</td>
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<td>ICL7660ACBA</td>
<td>0 to 70</td>
<td>8 Ld SOIC (N)</td>
<td>M8.15</td>
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<td>0 to 70</td>
<td>8 Ld SOIC (N) Tape and Reel</td>
<td>M8.15</td>
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<td>ICL7660ACPA</td>
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<tr>
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<td>-40 to 85</td>
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<td>ICL7660AIPA</td>
<td>-40 to 85</td>
<td>8 Ld PDIP</td>
<td>E8.3</td>
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</tbody>
</table>

† Add /883B to part number if 883B processing is required.

Features

- Simple Conversion of +5V Logic Supply to ±5V Supplies
- Simple Voltage Multiplication (V_{OUT} = \pm nV_{IN})
- Typical Open Circuit Voltage Conversion Efficiency 99.9%
- Typical Power Efficiency 98%
- Wide Operating Voltage Range
  - ICL7660 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 1.5V to 10.0V
  - ICL7660A . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 1.5V to 12.0V
- ICL7660A 100% Tested at 3V
- Easy to Use - Requires Only 2 External Non-Critical Passive Components
- No External Diode Over Full Temp. and Voltage Range

Applications

- On Board Negative Supply for Dynamic RAMs
- Localized μProcessor (8080 Type) Negative Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems

Pinouts

ICL7660, ICL7660A (PDIP, SOIC) TOP VIEW

ICL7660 (METAL CAN) TOP VIEW

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

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Absolute Maximum Ratings

Supply Voltage
- ICL7660: +10.5V
- ICL7660A: +13.0V
LV and OSC Input Voltage (Note 2):
- 0.3V to (V+ - 0.3V) for V+ < 5.5V
- 0V to (V+ - 5.5V) for V+ > 5.5V
Current into LV (Note 2): 20µA for V+ > 3.5V
Output Short Duration (V$_{SUPPLY}$ ≤ 5.5V): Continuous

Operating Conditions

Temperature Range
- ICL7660M: -55°C to 125°C
- ICL7660C, ICL7660AC: 0°C to 70°C
- ICL7660AI: -40°C to 85°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
1. θ$_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

ICL7660 and ICL7660A, V+ = 5V, TA = 25°C, C$_{OSC}$ = 0, Test Circuit Figure 11

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>ICL7660</th>
<th>ICL7660A</th>
<th>UNITS</th>
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<tbody>
<tr>
<td>Supply Current</td>
<td>I+</td>
<td>RL = ∞</td>
<td>MIN</td>
<td>170</td>
<td>500</td>
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<tr>
<td>Supply Voltage Range - Lo</td>
<td>V$_L+$</td>
<td>MIN ≤ TA ≤ MAX, RL = 10kΩ, LV to GND</td>
<td>1.5</td>
<td>-</td>
<td>3.5</td>
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<tr>
<td>Supply Voltage Range - Hi</td>
<td>V$_H+$</td>
<td>MIN ≤ TA ≤ MAX, RL = 10kΩ, LV to Open</td>
<td>3.0</td>
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<td>10.0</td>
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<td>Output Source Resistance</td>
<td>R$_{OUT}$</td>
<td>I$_{OUT}$ = 20mA, TA = 25°C</td>
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<td>55</td>
<td>100</td>
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<td></td>
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<td>I$_{OUT}$ = 20mA, 0°C ≤ TA ≤ 70°C</td>
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<td>I$_{OUT}$ = 20mA, -55°C ≤ TA ≤ 125°C</td>
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<td>I$_{OUT}$ = 20mA, -40°C ≤ TA ≤ 85°C</td>
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<td>-</td>
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<td></td>
<td></td>
<td>V+ = 2V, I$_{OUT}$ = 3mA, LV to GND, 0°C ≤ TA ≤ 70°C</td>
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<td>-</td>
<td>300</td>
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<td>V+ = 2V, I$_{OUT}$ = 3mA, LV to GND, -55°C ≤ TA ≤ 125°C</td>
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<td>Oscillator Frequency</td>
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<td>-</td>
<td>10</td>
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<tr>
<td>Power Efficiency</td>
<td>P$_{EF}$</td>
<td>RL = 5kΩ</td>
<td>95</td>
<td>98</td>
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<td>Voltage Conversion Efficiency</td>
<td>V$_{OUT EF}$</td>
<td>RL = ∞</td>
<td>97</td>
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<td>Oscillator Impedance</td>
<td>Z$_{OSC}$</td>
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<td></td>
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<td>V = 5V</td>
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ICL7660A, V+ = 3V, TA = 25°C, OSC = Free running, Test Circuit Figure 11, Unless Otherwise Specified

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
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<th>UNITS</th>
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<tr>
<td>Supply Current (Note 3)</td>
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<td>V+ = 3V, RL = ∞, 25°C</td>
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<td></td>
<td></td>
<td>0°C &lt; TA &lt; 70°C</td>
<td>-</td>
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<td>-40°C &lt; TA &lt; 85°C</td>
<td>-</td>
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<tr>
<td>Output Source Resistance</td>
<td>R$_{OUT}$</td>
<td>V+ = 3V, I$_{OUT}$ = 10mA</td>
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<td>-</td>
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<td>0°C &lt; TA &lt; 70°C</td>
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<tr>
<td>Oscillator Frequency (Note 3)</td>
<td>f$_{OSC}$</td>
<td>V+ = 3V (same as 5V conditions)</td>
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<td></td>
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<td>-40°C &lt; TA &lt; 85°C</td>
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ICL7660, ICL7660A

Electrical Specifications ICL7660 and ICL7660A, $V_+ = 5V$, $T_A = 25^\circ C$, $C_{OSC} = 0$, Test Circuit Figure 11

Unless Otherwise Specified (Continued)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>ICL7660</th>
<th>ICL7660A</th>
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<tr>
<td>Voltage Conversion Efficiency</td>
<td>$V_{OUT \text{E}F F}$</td>
<td>$V_+ = 3V$, $R_L = \infty$</td>
<td>- - -</td>
<td>99 - - %</td>
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<tr>
<td></td>
<td></td>
<td>$T_{MIN} &lt; T_A &lt; T_{MAX}$</td>
<td>- - -</td>
<td>99 - - %</td>
</tr>
<tr>
<td>Power Efficiency</td>
<td>$P_{\text{E}F F}$</td>
<td>$V_+ = 3V$, $R_L = 5k\Omega$</td>
<td>- - -</td>
<td>96 - - %</td>
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<tr>
<td></td>
<td></td>
<td>$T_{MIN} &lt; T_A &lt; T_{MAX}$</td>
<td>- - -</td>
<td>95 - - %</td>
</tr>
</tbody>
</table>

NOTES:
2. Connecting any input terminal to voltages greater than $V_+$ or less than GND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to “power up” of the ICL7660, ICL7660A.
3. Derate linearly above 50°C by 5.5mW/°C.
4. In the test circuit, there is no external capacitor applied to pin 7. However, when the device is plugged into a test socket, there is usually a very small but finite stray capacitance present, of the order of 5pF.
5. The Intersil ICL7660A can operate without an external diode over the full temperature and voltage range. This device will function in existing designs which incorporate an external diode with no degradation in overall circuit performance.

Functional Block Diagram

Typical Performance Curves (Test Circuit of Figure 11)

![Typical Performance Curves](image-url)
Typical Performance Curves (Test Circuit of Figure 11) (Continued)

**Figure 3.** Output Source Resistance as a Function of Temperature

**Figure 4.** Power Conversion Efficiency as a Function of Osc. Frequency

**Figure 5.** Frequency of Oscillation as a Function of External Osc. Capacitance

**Figure 6.** Unloaded Oscillator Frequency as a Function of Temperature

**Figure 7.** Output Voltage as a Function of Output Current

**Figure 8.** Supply Current and Power Conversion Efficiency as a Function of Load Current
**Detailed Description**

The ICL7660 and ICL7660A contain all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10\(\mu\)F polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 12, which shows an idealized negative voltage converter. Capacitor \(C_1\) is charged to a voltage, \(V^+\), for the half cycle when switches \(S_1\) and \(S_3\) are closed. (Note: Switches \(S_2\) and \(S_4\) are open during this half cycle.) During the second half cycle of operation, switches \(S_2\) and \(S_4\) are closed, with \(S_1\) and \(S_3\) open, thereby shifting capacitor \(C_1\) negatively by \(V^+\) volts. Charge is then transferred from \(C_1\) to \(C_2\) such that the voltage on \(C_2\) is exactly \(V^+\), assuming ideal switches and no load on \(C_2\). The ICL7660 approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7660 and ICL7660A, the 4 switches of Figure 12 are MOS power switches; \(S_1\) is a P-Channel device and \(S_2, S_3\) and \(S_4\) are N-Channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of \(S_3\) and \(S_4\) must always remain reverse biased with respect to their sources, but not so much as to degrade their “ON” resistances. In addition, at circuit start-up, and under output short circuit conditions (\(V_{OUT} = V^+\)), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7660 and ICL7660A by a logic network which senses the output voltage (\(V_{OUT}\)) together with the level translators, and switches the substrates of \(S_3\) and \(S_4\) to the correct level to maintain necessary reverse bias.

**Note:**

6. These curves include in the supply current that current fed directly into the load \(R_L\) from the \(V^+\) (See Figure 11). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7660/ICL7660A, to the negative side of the load. Ideally, \(V_{OUT} \approx 2V_{IN}\), \(I_S \approx 2I_L\), so \(V_{IN} \times I_S \approx V_{OUT} \times I_L\).
The voltage regulator portion of the ICL7660 and ICL7660A is an integral part of the anti-latchup circuitry; however, its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the “LV” pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5V the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

### Theoretical Power Efficiency Considerations

In theory, a voltage converter can approach 100% efficiency if certain conditions are met.

1. The driver circuitry consumes minimal power.
2. The output switches have extremely low ON resistance and virtually no offset.
3. The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660 and ICL7660A approach these conditions for negative voltage conversion if large values of $C_1$ and $C_2$ are used.

![Figure 12. Idealized Negative Voltage Converter](image)

**ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

$$ E = \frac{1}{2} C_1 (V_1^2 - V_2^2) $$

where $V_1$ and $V_2$ are the voltages on $C_1$ during the pump and transfer cycles. If the impedances of $C_1$ and $C_2$ are relatively high at the pump frequency (refer to Figure 12) compared to the value of $R_L$, there will be a substantial difference in the voltages $V_1$ and $V_2$. Therefore it is not only desirable to make $C_2$ as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for $C_1$ in order to achieve maximum efficiency of operation.

**Do’s And Don’ts**

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 3.5V.
3. Do not short circuit the output to V+ supply for supply voltages above 5.5V for extended periods, however, transient conditions including start-up are okay.
4. When using polarized capacitors, the + terminal of $C_1$ must be connected to pin 2 of the ICL7660 and ICL7660A and the + terminal of $C_2$ must be connected to GROUND.
5. If the voltage supply driving the ICL7660 and ICL7660A has a large source impedance (25Ω - 30Ω), then a 2.2µF capacitor from pin 8 to ground may be required to limit rate of rise of input voltage to less than 2V/µs.
6. User should insure that the output (pin 5) does not go more positive than GND (pin 3). Device latch up will occur under these conditions. A 1N914 or similar diode placed in parallel with $C_2$ will prevent the device from latching up under these conditions. (Anode pin 5, Cathode pin 3).

![Figure 13A. Configuration](image)

![Figure 13B. Thevenin Equivalent](image)

**FIGURE 13. SIMPLE NEGATIVE CONVERTER**
**Typical Applications**

**Simple Negative Voltage Converter**

The majority of applications will undoubtedly utilize the ICL7660 and ICL7660A for generation of negative supply voltages. Figure 13 shows typical connections to provide a negative supply negative (GND) for supply voltages below 3.5V.

The output characteristics of the circuit in Figure 13A can be approximated by an ideal voltage source in series with a resistance as shown in Figure 13B. The voltage source has a value of \(-V^+\). The output impedance \(R_O\) is a function of the ON resistance of the internal MOS switches (shown in Figure 12), the switching frequency, the value of \(C_1\) and \(C_2\), and the ESR (equivalent series resistance) of \(C_1\) and \(C_2\). A good first order approximation for \(R_O\) is:

\[
R_O \approx 2(R_{SW1} + R_{SW3} + ESR_{C1}) + \\
2(R_{SW2} + R_{SW4} + ESR_{C1}) + \\
1 + ESR_{C2}(f_{PUMP}) \left(\frac{1}{C_1}\right)
\]

Combining the four \(R_{SWX}\) terms as \(R_{SW}\), we see that:

\[
R_O \approx 2(R_{SW}) + \\
\frac{1}{(f_{PUMP} \cdot (C_1))} + 4(ESR_{C1}) + ESR_{C2}
\]

\(R_{SW}\), the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs), typically 23Ω at 25°C and 5V. Careful selection of \(C_1\) and \(C_2\) will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the \(1/(f_{PUMP} \cdot C_1)\) component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the \(1/(f_{PUMP} \cdot C_1)\) term, but may have the side effect of a net increase in output impedance when \(C_1 > 10\mu F\) and there is no longer enough time to fully charge the capacitors.
every cycle. In a typical application where \( f_{\text{OSC}} = 10\,\text{kHz} \) and \( C = C_1 = C_2 = 10\,\mu\text{F} \):

\[
R_O \approx 2 \frac{(23)}{5 \times 10^3} + 4 \frac{(\text{ESR}_{C1})}{10^{-5}} + 4 \frac{(\text{ESR}_{C2})}{5 \times 10^{-3}} (10^{-5})
\]

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low \( 1/(f_{\text{PUMP}} \times C_1) \) term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as 10\( \Omega \).

\[
R_O \approx 2 \frac{(23)}{5 \times 10^3} + 4 \frac{(\text{ESR}_{C1})}{10^{-5}} + 4 \frac{(\text{ESR}_{C2})}{5 \times 10^{-3}} (10^{-5})
\]

Cascading Devices

The ICL7660 and ICL7660A may be cascaded as shown to produced larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

\[
V_{\text{OUT}} = -n \times (V_{\text{IN}})
\]

where \( n \) is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660 and ICL7660A \( R_O \) values.

Changing the ICL7660/ICL7660A Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 17. In order to prevent possible device latchup, a 1k\( \Omega \) resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10k\( \Omega \) pullup resistor to V+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be \( 1/2 \) of the clock frequency. Output transitions occur on the positive-going edge of the clock.

It is also possible to increase the conversion efficiency of the ICL7660 and ICL7660A at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 18. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump \( (C_1) \) and reservoir \( (C_2) \) capacitors; this is overcome by increasing the values of \( C_1 \) and \( C_2 \) by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (OSC) and V+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of \( C_1 \) and \( C_2 \) (from 10\( \mu \text{F} \) to 100\( \mu \text{F} \)).
Positive Voltage Doubling

The ICL7660 and ICL7660A may be employed to achieve positive voltage doubling using the circuit shown in Figure 19. In this application, the pump inverter switches of the ICL7660 and ICL7660A are used to charge C1 to a voltage level of V+ - V_F (where V+ is the supply voltage and V_F is the forward voltage drop of diode D1). On the transfer cycle, the voltage on C1 plus the supply voltage (V+) is applied through diode D2 to capacitor C2. The voltage thus created on C2 becomes (2V+) - (2V_F) or twice the supply voltage minus the combined forward voltage drops of diodes D1 and D2.

The source impedance of the output (V_OUT) will depend on the output current, but for V+ = 5V and an output current of 10mA it will be approximately 60Ω.

Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 20 combines the functions shown in Figures 13 and Figure 19 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9V and -5V from an existing +5V supply. In this instance capacitors C1 and C3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C2 and C4 are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 21. The combined load will be evenly shared between the two sides. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 16, +15V can be converted (via +7.5, and -7.5) to a nominal -15V, although with rather high series output resistance (~250Ω).

Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7660 and ICL7660A can be a problem, particularly if the load current varies substantially. The circuit of Figure 22 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7660s and ICL7660As output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the ICL7660 and ICL7660A, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.
**Other Applications**

Further information on the operation and use of the ICL7660 and ICL7660A may be found in AN051 “Principals and Applications of the ICL7660 and ICL7660A CMOS Voltage Converter”.

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**FIGURE 22. REGULATING THE OUTPUT VOLTAGE**

**FIGURE 23. RS232 LEVELS FROM A SINGLE 5V SUPPLY**

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**Sales Office Headquarters**

**NORTH AMERICA**
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

**EUROPE**
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

**ASIA**
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029