MOTOROLA

Microprocessors and Memory
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MC68302

Integrated Multiprotocol Processor
User's Manual

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PREFACE

The complete documentation package for the MC68302 consists of the M68000PM/AD, *MC68000 Family Programmer's Reference Manual,* MC68302UM/AD, *MC68302 Integrated Multiprotocol Processor User's Manual,* and the MC68302/D, *MC68302 Integrated Multiprotocol Processor Product Brief*.

The *MC68302 Integrated Multiprotocol Processor User's Manual* describes the programming, capabilities, registers, and operation of the MC68302; the *MC68000 Family Programmer's Reference Manual* provides instruction details for the MC68302; and the *MC68302 Low Power Integrated Multiprotocol Processor Product Brief* provides a brief description of the MC68302 capabilities.

This user's manual is organized as follows:

Section 1	General Description
Section 2	MC68000/MC68008 Core
Section 3	System Integration Block (SIB)
Section 4	Communications Processor (CP)
Section 5	Signal Description
Section 6	Electrical Characteristics
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Appendix E	SCC Programming Reference
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SECTION 1
GENERAL DESCRIPTION

The MC68302 integrated multiprotocol processor (IMP) is a very large-scale integration (VLSI) device incorporating the main building blocks needed for the design of a wide variety of controllers. The device is especially suitable to applications in the communications industry. The IMP is the first device to offer the benefits of a closely coupled, industry-standard M68000 microprocessor core and a flexible communications architecture. The IMP may be configured to support a number of popular industry interfaces, including those for the Integrated Services Digital Network (ISDN) basic rate and terminal adaptor applications. Concurrent operation of different protocols is easily achieved through a combination of architectural and programmable features. Data concentrators, line cards, modems, bridges, and gateways are examples of suitable applications for this device.

The IMP is a high-density complementary metal-oxide semiconductor (HCMOS) device consisting of an M68000 microprocessor core, a system integration block (SIB), and a communications processor (CP).

1.1 BLOCK DIAGRAM

The block diagram is shown in Figure 1-1.

By integrating the microprocessor core with the serial ports (in the CP) and the system peripherals (in the SIB), the IMP is capable of handling complex tasks such as all ISDN basic rate (2B + D) access tasks. For example, the IMP architecture and the serial communications controller (SCC) ports can support the interface of an S/T transceiver chip and the lower part (bit handling) ISO/OSI layer-2 functions. Other layer-2 functions and the higher protocol layers would then be implemented by software executed by the M68000 core.

Using the flexible memory-based buffer structure of the IMP, terminal adaptor applications also can be supported by transforming and sharing data buffer information between the three SCC ports and the serial communications port (SCP). Each SCC channel is available for HDLC/SDLC[1], UART, BISYNC, DDCMP[2], V.110, or transparent operation. The IMP provides a number of choices for various rate adaptive techniques and can be used for functions such as a terminal controller, multiplexer, or concentrator.

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1. SDLC is a trademark of International Business Machines.

2. DDCMP is a trademark of Digital Equipment Corporation.

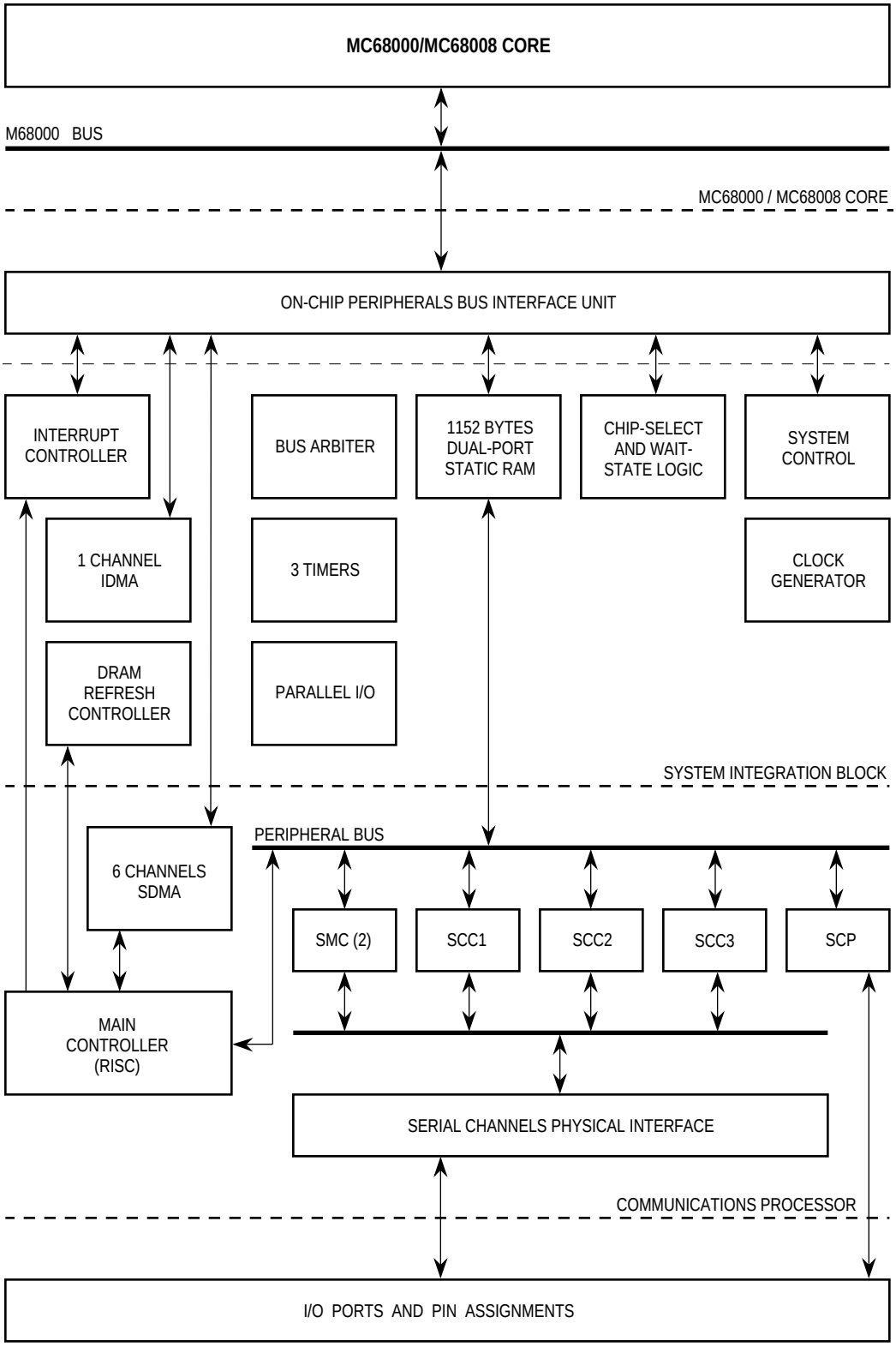


Figure 1-1. MC68302 Block Diagram

The MC68302 can also be used in applications such as board-level industrial controllers performing real-time control applications with a local control bus and an X.25 packet network connection. Such a system provides the real-time response to a demanding peripheral while permitting remote monitoring and communication through an X.25 packet network.

1.2 FEATURES

The features of the IMP are as follows:

- On-Chip HCMOS MC68000/MC68008 Core Supporting a 16- or 8-Bit M68000 Family-System
- IB Including:
  - —Independent Direct Memory Access (IDMA) Controller with Three Handshake Signals: $\overline{\text{DREQ}}$, $\overline{\text{DACK}}$, and $\overline{\text{DONE}}$.
  - —Interrupt Controller with Two Modes of Operation
  - —Parallel Input/Output (I/O) Ports, Some with Interrupt Capability
  - —On-Chip 1152-Byte Dual-Port RAM
  - —Three Timers Including a Watchdog Timer
  - —Four Programmable Chip-Select Lines with Wait-State Generator Logic
  - —Programmable Address Mapping of the Dual-Port RAM and IMP Registers
  - —On-Chip Clock Generator with Output Signal
  - —System Control:
    - Bus Arbitration Logic with Low-Interrupt Latency Support
    - System Status and Control Logic
    - Disable CPU Logic (M68000)
    - Hardware Watchdog
    - Low-Power (Standby) Modes
    - Freeze Control for Debugging
    - DRAM Refresh Controller
- CP Including:
  - —Main Controller (RISC Processor)
  - —Three Independent Full-Duplex Serial Communications Controllers (SCCs)
  - —Supporting Various Protocols:
    - High-Level/Synchronous Data Link Control (HDLC/SDLC)
    - Universal Asynchronous Receiver Transmitter (UART)
    - Binary Synchronous Communication (BISYNC)
    - Synchronous/Asynchronous Digital Data Communications Message Protocol (DDCMP)
    - Transparent Modes
    - V.110 Rate Adaption
  - —Six Serial DMA Channels for the Three SCCs
  - —Flexible Physical Interface Accessible by SCCs Including:
    - Motorola Interchip Digital Link (IDL)
    - General Circuit Interface (GCI, also known as IOM[3]-2)
    - Pulse Code Modulation (PCM) Highway Interface

3. IOM is a trademark of Siemens AG

Nonmultiplexed Serial Interface (NMSI) Implementing Standard Modem Signals
—SCP for Synchronous Communication
—Two Serial Management Controllers (SMCs) To Support IDL and GCI Auxiliary Channels

1.3 MC68302 SYSTEM ARCHITECTURE

Most general-purpose microprocessor-based systems use an architecture that interfaces all peripheral devices directly onto a single microprocessor bus (see Figure 1-2).

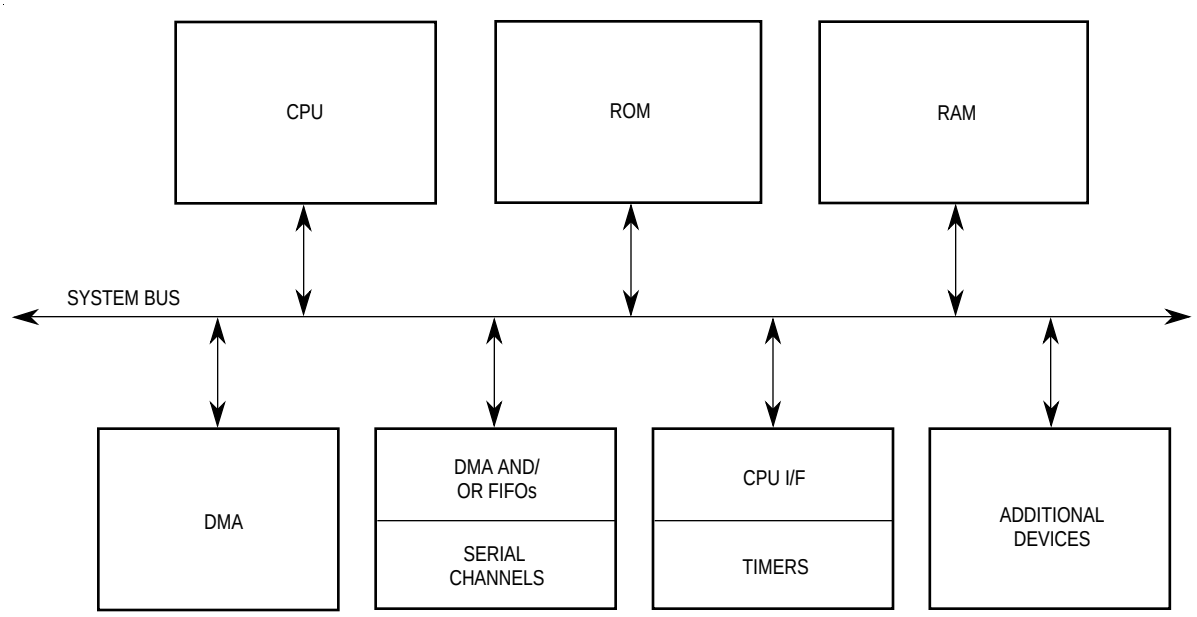


Figure 1-2. General-Purpose Microprocessor System Design

The MC68302 microprocessor architecture is shown in Figure 1-3. In this architecture, the peripheral devices are isolated from the system bus through a dual-port memory. Various parameters and counters and all memory buffer descriptor tables reside in the dual-port RAM. The receive and transmit data buffers may be located in the on-chip RAM or in the off-chip system RAM. Six DMA channels are dedicated to the six serial ports (receive and transmit for each of the three SCC channels). If data for an SCC channel is programmed to be located in the external RAM, the CP will program the corresponding DMA channel for the required accesses, bypassing the dual-port RAM. If data resides in the dual-port RAM, then the CP accesses the RAM with one clock cycle and no arbitration delays.

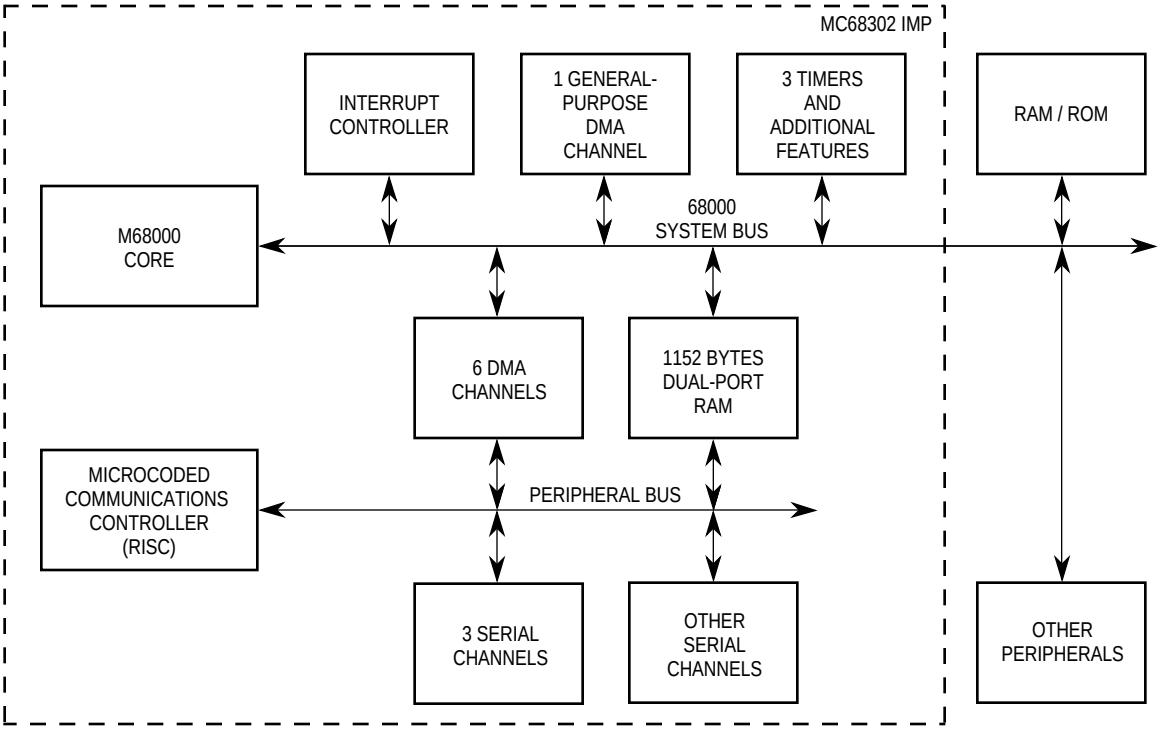


Figure 1-3. MC68302 System Design

The use of a unique arbitration scheme and synchronous transfers between the microprocessor and dual-port RAM gives zero wait-state operation to the M68000 microprocessor core. The dual-port RAM can be accessed by the CP main controller (RISC) once every clock cycle for either read or write operations. When the M68000 core accesses the dual-port RAM, each access is pipelined along with the CP accesses so that data is read or written without conflict. The net effect is the loss of a single memory access by the CP main controller per M68000 core access.

The buffer memory structure of the MC68302 can be configured to closely match I/O channel requirements by careful selection of buffer size and buffer linking. The interrupt structure is also programmable so that the on-chip M68000 processor can be off-loaded from the peripheral bit-handling functions to perform higher layer application software or protocol processing.

1.4 NMSI COMMUNICATIONS-ORIENTED ENVIRONMENT

When the interface to equipment or proprietary networks requires the use of standard control and data signals, the MC68302 can be programmed into the nonmultiplexed serial interface (NMSI) mode. This mode, which is available for one, two, or all three SCC ports, can be selected while the other ports use one of the multiplexed interface modes (IDL, GCI, or PCM highway).

In the example shown in Figure 1-4, one SCC channel connects through the NMSI mode to a commercial packet data network. This connection might be used for remote status monitoring or for maintenance functions for a system. Another SCC is used to connect to a local asynchronous terminal. The other SCC channel is used as a local synchronous channel, which could connect to another computer or subsystem. The SCP channel could then be used for local interconnection of interface chips or peripherals to the MC68302-based system.

1.5 BASIC RATE ISDN OR DIGITAL VOICE/DATA TERMINAL

A basic rate ISDN (2B + D) or digital voice/data terminal can be made from a chip set based on the MC68302. Refer to Figure 1-5 for an example of a basic rate ISDN voice/data terminal. In this terminal, the CP can directly support the 2B + D channels and perform either V.110 or V.120 rate adaption. The physical layer serial interface is connected to the local interconnection bus (IDL in Figure 1-5, but the GCI and PCM buses can also be supported). The system then supports one of the B channels for voice (connected directly to the physical bus). The D channel consists of one SCC port; the other B channel is used for data transfer through a second SCC port. The data can be routed to a terminal (RS-232 type) via the third SCC port in the NMSI mode. The SCP functions as a control channel for the IDL bus in this case.

Some ISDN physical layer devices support the signaling and framing functions of the D channel. In these cases, the D channel can connect through the microprocessor interface to the physical layer device, and the extra SCC port can then be used for a second B channel to transfer data.

The benefit of a local interconnection bus (see Figure 1-5) versus a microprocessor bus is a lower pin count. It is also easy to maintain this low pin-count interface between several different interface chips, such as the MC145554 PCM codec/filter monocircuit and the MC145474 S/T transceiver.

The MC68302 combines the M68000 architecture with a number of peripherals for integrated applications in communications control. The M68000 core manages the CP through the on-chip, dual-port RAM and internal registers. The base address of the dual-port RAM and internal registers is selected through the base address register. Other peripherals are also accessed and controlled through internal registers: the IDMA controller, the three timers, I/O ports, and the interrupt controller.

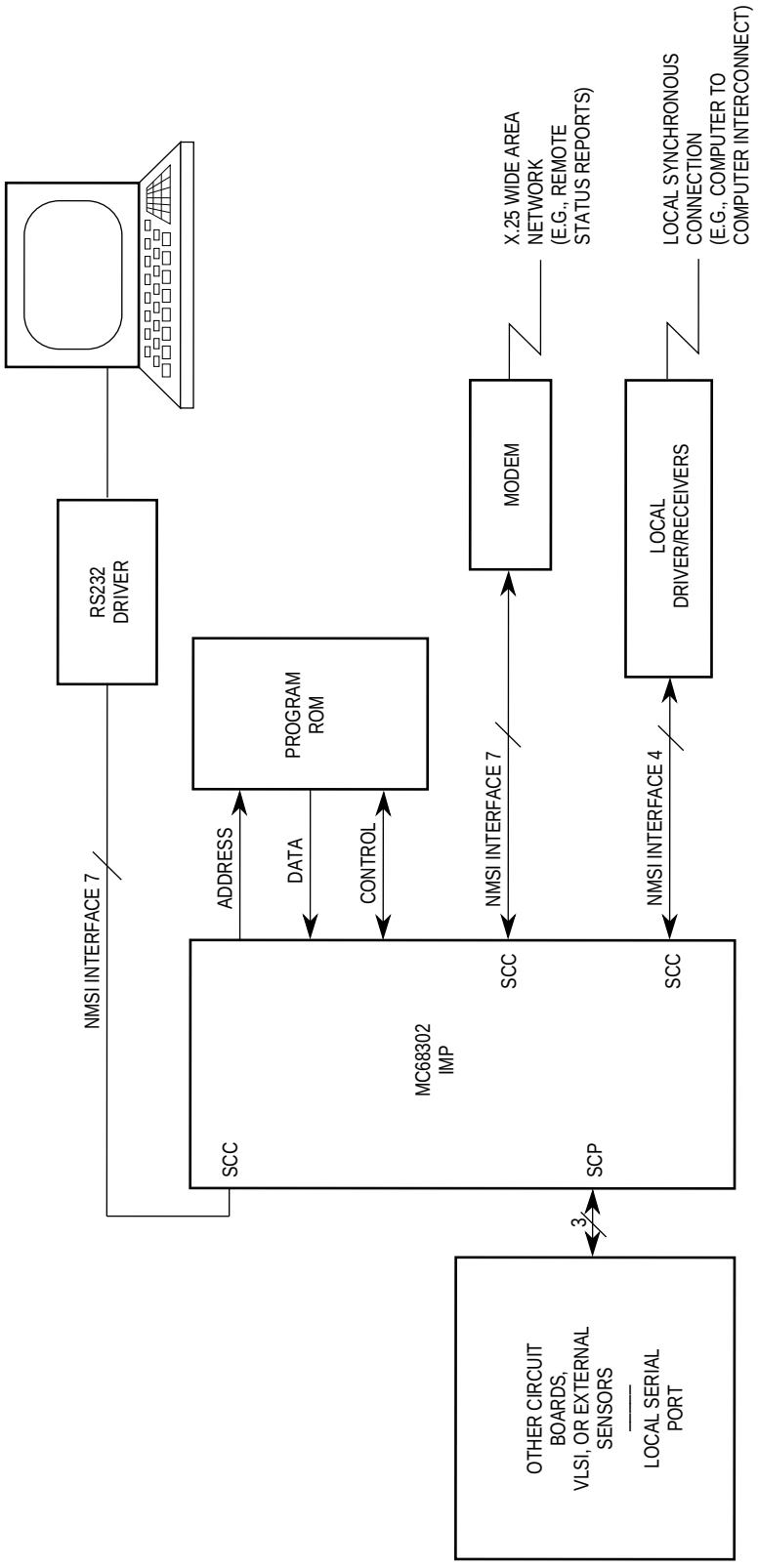


Figure 1-4. NMSI Communications-Oriented Board Design

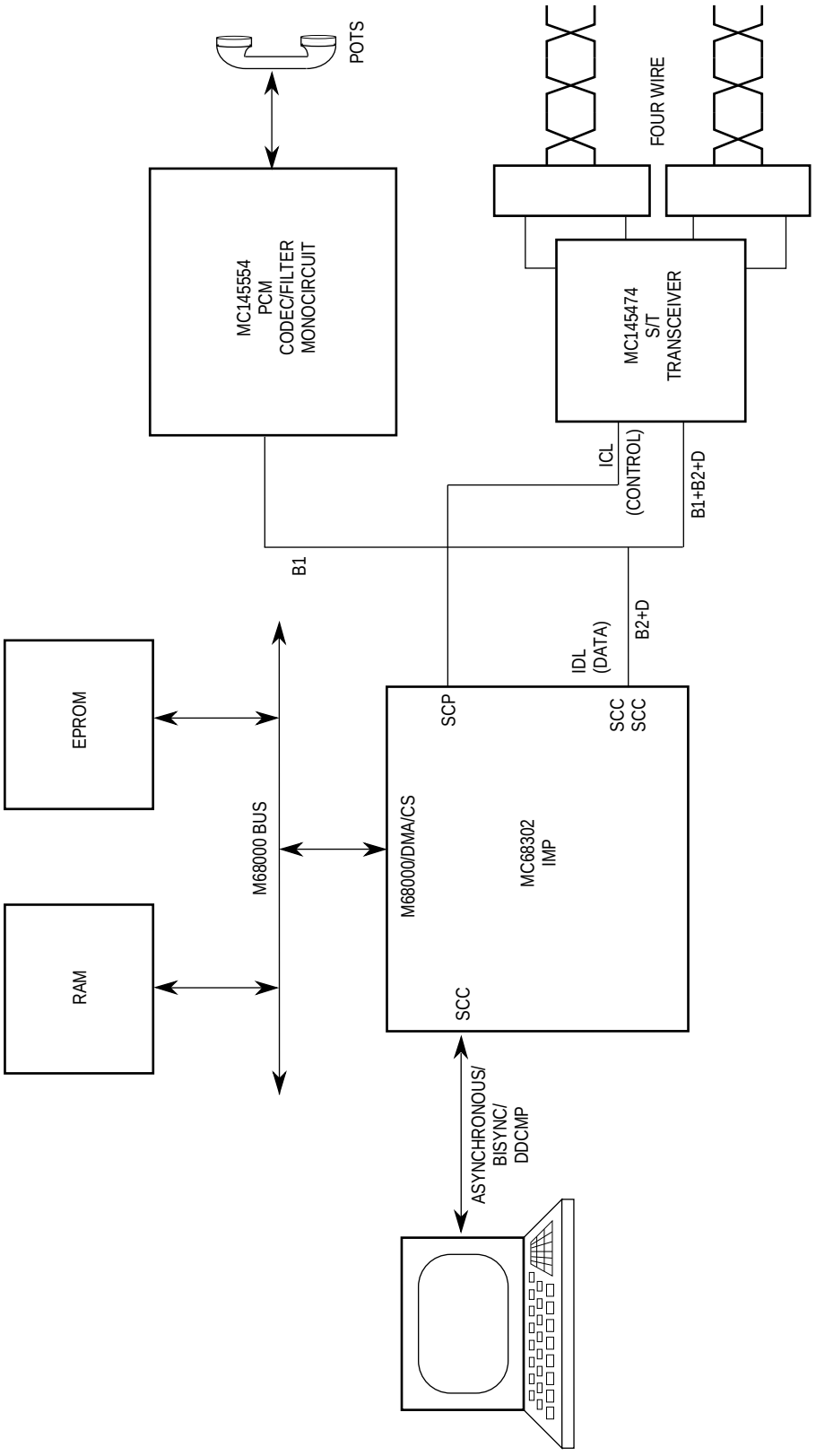


Figure 1-5. Basic Rate IDL Voice/Data Terminal in ISDN

SECTION 2
MC68000/MC68008 CORE

The MC68302 integrates a high-speed M68000 processor with multiple communications peripherals. The provision of direct memory access (DMA) control and link layer management with the serial ports allows high throughput of data for communications-intensive applications, such as basic rate Integrated Services Digital Network (ISDN).

The MC68302 can operate either in the full MC68000 mode with a 16-bit data bus or in the MC68008 mode with an 8-bit data bus by tying the bus width (BUSW) pin low. $\overline{\text{UDS}}$/A0 functions as A0 and $\overline{\text{LDS}}$/$\overline{\text{DS}}$ functions as $\overline{\text{DS}}$ in the MC68008 mode.

NOTE

The BUSW pin is static and is not intended to be used for dynamic bus sizing. If the state of BUSW is changed during operation of the MC68302, erratic operation may occur.

Refer to the MC68000UM/AD, *M68000 8-/16-/32-Bit Microprocessors User's Manual*, for complete details of the on-chip microprocessor. Throughout this manual, references may use the notation M68000, meaning all devices belonging to this family of microprocessors, or the notation MC68000, MC68008, meaning the specific microprocessor products.

2.1 PROGRAMMING MODEL

The M68000 microprocessor executes instructions in one of two modes: user or supervisor. The user mode provides the execution environment for most of the application programs. The supervisor mode, which allows some additional instructions and privileges, is intended for use by the operating system and other system software.

Shown in Figure 2-1, the M68000 core programming model offers 16, 32-bit, general-purpose registers (D7–D0, A7–A0), a 32-bit program counter (PC), and an 8-bit condition code register (CCR) when running in user space. The first eight registers (D7–D0) are used as data registers for byte (8-bit), word (16-bit), and long-word (32-bit) operations. The second set of seven registers (A6–A0) and the stack pointer (USP in user space) may be used as software stack pointers and base address registers. In addition, the address registers may be used for word and long-word operations. All 16 registers may be used as index registers.

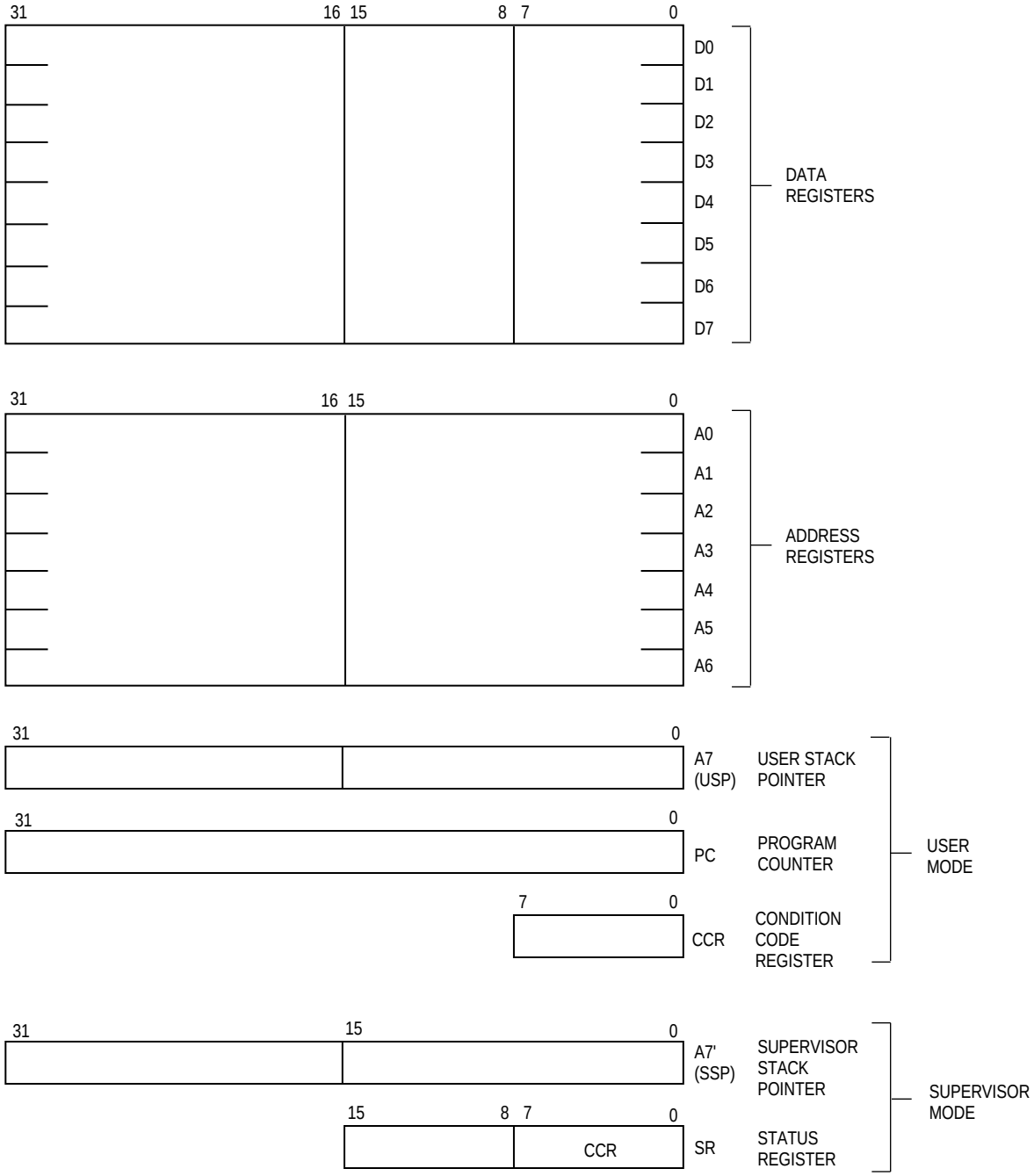


Figure 2-1. M68000 Programming Model

The supervisor's programming model includes supplementary registers, including the supervisor stack pointer (SSP) and the status register (SR) as shown in Figure 2-2. The SR contains the interrupt mask (eight levels available) as well as the following condition codes: overflow (V), zero (Z), negative (N), carry (C), and extend (X). Additional status bits indicate that the processor is in trace (T) mode and/or in a supervisor (S) state.

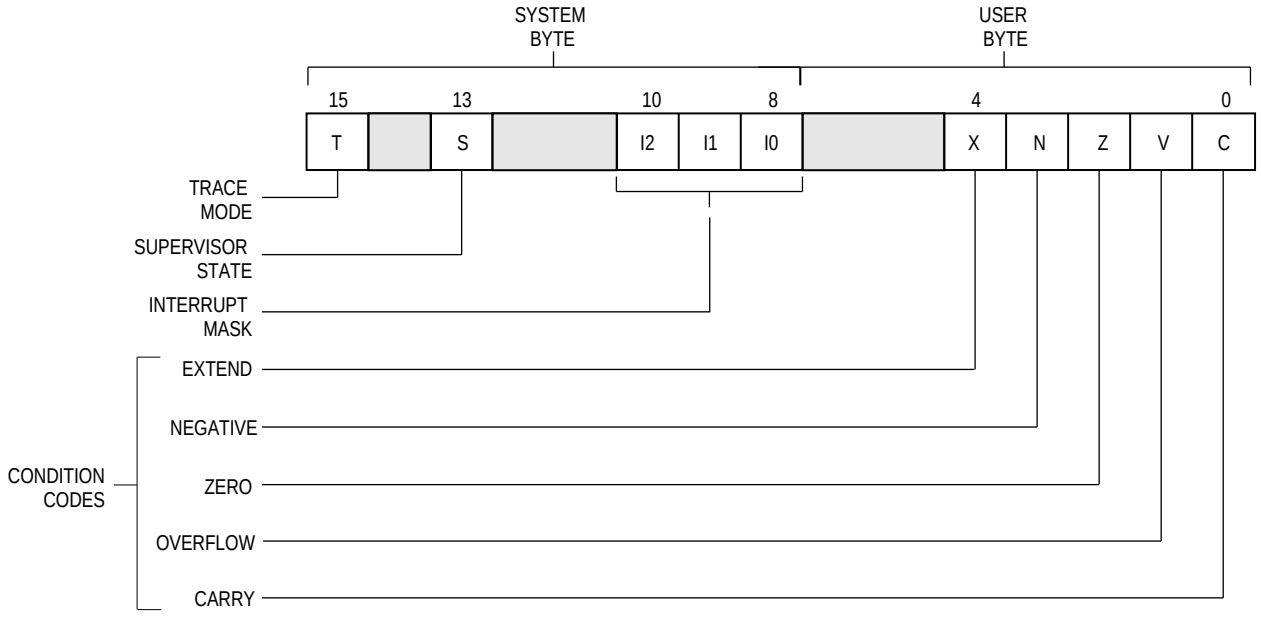


Figure 2-2. M68000 Status Register

2.2 INSTRUCTION SET SUMMARY

The five data types supported by the M68000 on the MC68302 are bits, binary-coded decimal (BCD) digits (4 bits), bytes (8 bits), words (16 bits), and long words (32 bits).

In addition, operations on other data types, such as memory addresses, status word data, etc., are provided for in the instruction set. Shown in Table 2-1, the 14 flexible addressing modes include six basic types:

- Register Direct
- Register Indirect
- Absolute
- Immediate
- Program Counter Relative
- Implied

The capability to perform postincrementing, predecrementing, offsetting, and indexing is included in the register indirect addressing modes. Program counter relative modes can also be modified via indexing and offsetting.

The M68000 instruction set is shown in Table 2-2.

Some basic instructions also have variations as shown in Table 2-3.

Special emphasis has been placed on the instruction set to simplify programming and to support structured high-level languages. With a few exceptions, each instruction operates

on bytes, words, or long words, and most instructions can use any of the 14 addressing modes.

Combining instruction types, data types, and addressing modes provides over 1000 useful instructions. These instructions include signed and unsigned multiply and divide, quick arithmetic operations, BCD arithmetic, and expanded operations (through traps).

Table 2-1. M68000 Data Addressing Modes

Mode	Generation
Register Direct Addressing	
Data Register Direct	EA = Dn
Address Register Direct	EA = An
Absolute Data Addressing	
Absolute Short	EA = (Next Word)
Absolute Long	EA = (Next Two Words)
Program Counter Relative Addressing	
Relative with Offset	EA = (PC) + d_{16}
Relative with Index and Offset	EA = (PC) + Xn + d8
Register Indirect Addressing	
Register Indirect	EA = (An)
Postincrement Register Indirect	EA = (An), An ⇐ An + N
Predecrement Register Indirect	EA = ← An - N, EA = (An)
Register Indirect with Offset	EA = (An) + d_{16}
Indexed Register Indirect with Offset	EA = (An) + (Xn) + d_8
Immediate Data Addressing	
Immediate	DATA = Next Word(s)
Quick Immediate	Inherent Data
Implied Addressing	
Implied Register	EA = SR, USP, SSP, PC

NOTES:

EA	=	Effective Address
An	=	Address Register
Dn	=	Data Register
Xn	=	Address or Data Register Used as an Index Register
SR	=	Status Register
PC	=	Program Counter
( )	=	Contents of
d_8	=	8-Bit Offset (Displacement)
d16	=	16-Bit Offset (Displacement)
N	=	1 for byte, 2 for word, and 4 for long word. If An is the stack pointer and the operand size is byte, N = 2 to keep the stack pointer on a word boundary.
←	=	Replaces

Table 2-2. M68000 Instruction Set Summary

Mnemonic	Description
ABCD	Add Decimal with Extend
ADD	Add
AND	Logical AND
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
Bcc	Branch Conditionally
BCHG	Bit Test and Change
BCLR	Bit Test and Clear
BRA	Branch Always
BSET	Bit Test and Set
BSR	Branch to Subroutine
BTST	Bit Test
CHK	Check Register Against Bounds
CLR	Clear Operand
CMP	Compare
DBcc	Decrement and Branch Conditionally
DIVS	Signed Divide
DIVU	Unsigned Divide
EOR	Exclusive OR
EXG	Exchange Registers
EXT	Sign Extend
JMP	Jump
JSR	Jump to Subroutine
LEA	Load Effective Address
LINK	Link Stack
LSL	Logical Shift Left
LSR	Logical Shift Right
MOVE	Move Source to Destination
MULS	Signed Multiply
MULU	Unsigned Multiply
NBCD	Negate Decimal with Extend
NEG	Negate
NOP	No Operation
NOT	Ones Complement
OR	Logical OR
PEA	Push Effective Address
RESET	Reset External Devices
ROL	Rotate Left without Extend
ROR	Rotate Right without Extend
ROXL	Rotate Left with Extend
ROXR	Rotate Right with Extend
RTE	Return from Exception
RTR	Return and Restore
RTS	Return from Subroutine
SBCD	Subtract Decimal with Extend
Scc	Set Conditionally
STOP	Stop
SUB	Subtract
SWAP	Swap Data Register Halves
TAS	Test and Set Operand
TRAP	Trap
TRAPV	Trap on Overflow
TST	Test
UNLK	Unlink

Table 2-3. M68000 Instruction Type Variations

Instruction Type	Variation	Description
ADD	ADD ADDA ADDQ ADDI ADDX	Add Add Address Add Quick Add Immediate Add with Extend
AND	AND ANDI ANDI to CCR ANDI to SR	Logical AND And Immediate And Immediate to Condition Codes And Immediate to Status Registers
CMP	CMP CMPA CMPM CMPI	Compare Compare Addresses Compare Memory Compare Immediate
EOR	EOR EORI EORI to CCR EORI to SR	Exclusive OR Exclusive OR Immediate Exclusive OR Immediate to Condition Codes Exclusive OR Immediate to Status Register
MOVE	MOVE MOVEA MOVEM MOVEP MOVEQ MOVE from SR MOVE to SR MOVE to CCR MOVE USP	Move Source to Destination Move Address Move Multiple Register Move Peripheral Data Move Quick Move from Status Register Move to Status Register Move to Condition Codes Move User Stack Pointer
NEG	NEG NEGX	Negate Negate with Extend
OR	OR ORI ORI to CCR ORI to SR	Logical OR OR Immediate OR Immediate to Condition Codes OR Immediate to Status Register
SUB	SUB SUBA SUBI SUBQ SUBX	Subtract Subtract Address Subtract Immediate Subtract Quick Subtract with Extend

2.3 ADDRESS SPACES

The M68000 microprocessor operates in one of two privilege states: user or supervisor. The privilege state determines which operations are legal, which operations are used by the external memory management device to control and translate accesses, and which operations are used to choose between the SSP and the USP in instruction references. The M68000 address spaces are shown in Table 2-4.

In the M68000 Family, the address spaces are indicated by function code pins. On the M68000, three function code pins are output from the device on every bus cycle of every executed instruction. This provides the purpose of each bus cycle to external logic.

Other bus masters besides the M68000 may also output function codes during their bus cycles. On the MC68302, this capability is provided for each potential internal bus master (i.e., the IDMA, SDMA, and DRAM refresh units). Also on the MC68302, provision is made for the decoding of function codes that are output from external bus masters (e.g., in the chip-select generation logic).

In computer design, function code information can be used to protect certain portions of the address map from unauthorized access or even to extend the addressable range beyond the M68000 16-Mbyte address limit. However, in controller applications, function codes are used most often as a debugging aid. Furthermore, in many controller applications, the M68000 stays continuously in the supervisor state.

Table 2-4. M68000 Address Spaces

Function Code Output			
FC2	**FC1**	**FC0**	**Reference Class**
1	0	0	(Unassigned)
0	0	1	User Data
0	1	0	User Program
0	1	1	(Unassigned)
1	0	0	(Unassigned)
1	0	1	Supervisor Data
1	1	0	Supervisor Program
1	1	1	CPU Space*

* This is the function code output for the M68000 interrupt acknowledge cycle.

All exception processing occurs in the supervisor state, regardless of the state of the S bit when the exception occurs. The bus cycles generated during exception processing are classified as supervisor references. All stacking operations during exception processing use the SSP.

The user state is the lower state of privilege. For instruction execution, the user state is determined by the S bit of the SR; if the S bit is negated (low), the processor is executing instructions in the user state. Most instructions execute identically in either user state or supervisor state. However, instructions having important system effects are privileged. User programs are not permitted to execute the STOP instruction or the RESET instruction. To ensure that a user program cannot enter the supervisor state except in a controlled manner, the instructions which modify the entire SR are privileged. To aid in debugging programs to be used in operating systems, the move-to-user-stack-pointer (MOVE to USP) and move-from-user-stack-pointer (MOVE from USP) instructions are also privileged.

The supervisor state is the highest state of privilege. For instruction execution, the supervisor state is determined by the S bit of the SR; if the S bit is asserted (high), the processor is in the supervisor state. The bus cycles generated by instructions executed in the supervisor state are classified as supervisor references. While the processor is in the supervisor privilege state, those instructions using either the system stack pointer implicitly or address register seven explicitly access the SSP.

Once the processor is in the user state and executing instructions, only exception processing can change the privilege state. During exception processing, the current state of the S bit in the SR is saved and the S bit is asserted, putting the processor in the supervisor state. Therefore, when instruction execution resumes at the address specified to process the exception, the processor is in the supervisor privilege state. The transition from the supervisor to user state can be accomplished by any of four instructions: return from exception (RTE), move to status register (MOVE to SR), AND immediate to status register (ANDI to SR), and exclusive OR immediate to status register (EORI to SR).

2.4 EXCEPTION PROCESSING

The processing of an exception occurs in four steps, with variations for different exception causes. During the first step, a temporary copy of the SR is made, and the SR is set for exception processing. During the second step, the exception vector is determined; during the third step, the current processor context is saved. During the fourth step, a new context is obtained, and the processor switches to instruction processing.

2.4.1 Exception Vectors

Exception vectors are memory locations from which the processor fetches the address of a routine to handle that exception. All exception vectors are two words long except for the reset vector, which is four words. All exception vectors lie in the supervisor data space except for the reset vector, which is in the supervisor program space. A vector number is an 8-bit number which, when multiplied by four, gives the offset of the exception vector. Vector numbers are generated internally or externally, depending on the cause of the exception. In the case of interrupts, during the interrupt acknowledge bus cycle, a peripheral may provide an 8-bit vector number to the processor on data bus lines D7–D0. Alternatively, the peripheral may assert autovector ($\overline{\text{AVEC}}$) instead of data transfer acknowledge ($\overline{\text{DTACK}}$) to request an autovector for that priority level of interrupt. The exception vector assignments for the M68000 processor are shown in Table 2-5.

Table 2-5. M68000 Exception Vector Assignment

Vector Number	Decimal	Address Hex	Space	Assignment
0	0	000	SP	Reset: Initial SSP[2]
1	4	004	SP	Reset: Initial PC[2]
2	8	008	SD	Bus Error
3	12	00C	SD	Address Error
4	16	010	SD	Illegal Instruction
5	20	014	SD	Zero Divide
6	24	018	SD	CHK Instruction
7	28	01C	SD	TRAPV Instruction
8	32	020	SD	Privilege Violation
9	36	024	SD	Trace
10	40	028	SD	Line 1010 Emulator

Table 2-5. M68000 Exception Vector Assignment

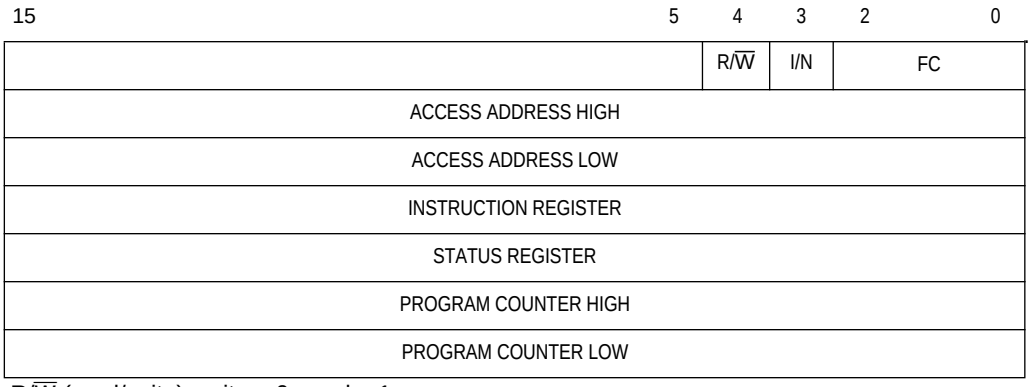
11	44	02C	SD	Line 1111 Emulator
12[1]	48	030	SD	(Unassigned, Reserved)
13[1]	52	034	SD	(Unassigned, Reserved)
14[1]	56	038	SD	(Unassigned, Reserved)
15	60	03C	SD	Uninitialized Interrupt Vector
16–23[1]	64	040	SD	(Unassigned, Reserved)
	92	05C	SD	
24	96	060	SD	Spurious Interrupt[3]
25	100	064	SD	Level 1 Interrupt Autovector
26	104	068	SD	Level 2 Interrupt Autovector
27	108	06C	SD	Level 3 Interrupt Autovector
28	112	070	SD	Level 4 Interrupt Autovector
29	116	074	SD	Level 5 Interrupt Autovector
30	120	078	SD	Level 6 Interrupt Autovector
31	124	07C	SD	Level 7 Interrupt Autovector
32–47	128	080	SD	TRAP Instruction Vectors[4]
	188	0BC	SD	
48–63[1]	192	0C0	SD	(Unassigned, Reserved)
	255	0FC	SD	
64–255	256	100	SD	User Interrupt Vectors
	1020	3FC	SD	

NOTES:

1. Vector numbers 12–14, 16–23, and 48–63 are reserved for future enhancements by Motorola (with vectors 60–63 being used by the M68302 (see 2.7 MC68302 IMP Configuration and Control)). No user peripheral devices should be assigned these numbers.
2. Unlike the other vectors which only require two words, reset vector (0) requires four words and is located in the supervisor program space.
3. The spurious interrupt vector is taken when there is a bus error indication during interrupt processing.
4. TRAP # n uses vector number 32 + n.

2.4.2 Exception Stacking Order

Exception processing saves the most volatile portion of the current processor context on top of the supervisor stack. This context is organized in a format called the exception stack frame. The amount and type of information saved on the stack is determined by the type of exception. The reset exception causes the M68000 to halt current execution and to read a new SSP and PC as shown in Table 2-5. A bus error or address error causes the M68000 to store the information shown in Figure 2-3. The interrupts, traps, illegal instructions, and trace stack frames are shown in Figure 2-4.



R/$\overline{W}$ (read/write): write = 0, read = 1
I/N (instruction not): instruction = 0, not =1
FC: Function Code

Figure 2-3. M68000 Bus/Address Error Exception Stack Frame

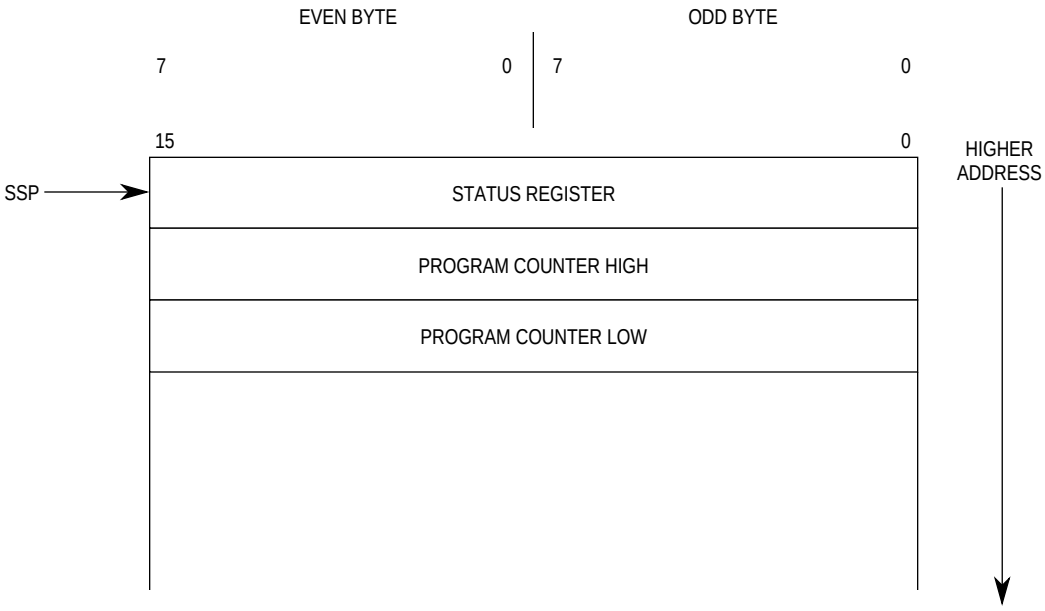


Figure 2-4. M68000 Short-Form Exception Stack Frame

NOTE

The MC68302 uses the exact same exception stack frames as the MC68000.

For exception processing times and instruction execution times, refer to MC68000UM/AD, *8-/16-/32-Bit Microprocessor User's Manual*.

2.5 INTERRUPT PROCESSING

Seven interrupt levels are provided by the M68000 core. If the IMP's interrupt controller is placed in the normal mode, six levels are available to the user. If the interrupt controller is in the dedicated mode, three levels are available to the user. In either mode, level 4 is reserved for the on-chip peripherals. Devices may be chained externally within one of the available priority levels, allowing an unlimited number of external peripheral devices to interrupt the processor. The SR contains a 3-bit mask indicating the current processor priority level. Interrupts are inhibited for all priority levels less than or equal to the current processor priority (see Figure 2-2).

An interrupt request is made to the processor by encoding the request on the interrupt request lines (normal mode) or by asserting the appropriate request line (dedicated mode). Rather than forcing immediate exception processing, interrupt requests arriving at the processor are made pending to be detected between instruction executions.

If the priority of the pending interrupt is lower than or equal to the current processor priority, execution continues with the next instruction, and the interrupt exception processing is postponed.

If the priority of the pending interrupt is greater than the current processor priority, the exception processing sequence is started. A copy of the SR is saved, the privilege state is set to supervisor state, tracing is suppressed, and the processor priority level is set to the level of the interrupt being acknowledged. The processor fetches the vector number from the interrupting device, classifying the reference as an interrupt acknowledge on the address bus. If external logic requests automatic vectoring (via the $\overline{\text{AVEC}}$ pin), the processor internally generates a vector number determined by the interrupt level number. If external logic indicates a bus error, the interrupt is considered spurious, and the generated vector number references the spurious interrupt vector number.

2.6 M68000 SIGNAL DIFFERENCES

The MC68302 core supports one additional signal not visible on the standard M68000: $\overline{\text{RMC}}$. Asserted externally on read-modify-write cycles, the $\overline{\text{RMC}}$ signal is typically used as a bus lock to ensure integrity of instructions using the locked read-modify-write operation of the test and set (TAS) instruction. The $\overline{\text{RMC}}$ signal from the M68000 core is applied to the MC68302 arbiter and can be programmed to prevent the arbiter from issuing bus grants until the completion of an MC68000-core-initiated read-modify-write cycle.

The MC68302 can be programmed to use the $\overline{\text{RMC}}$ signal to negate address strobe ($\overline{\text{AS}}$) at the end of the read portion of the cycle and assert $\overline{\text{AS}}$ at the beginning of the write portion of the cycle (See 3.8.3 System Control Bits).

Two M6800 signals are omitted from the MC68302: valid memory address ($\overline{\text{VMA}}$) and enable (E). The valid peripheral address ($\overline{\text{VPA}}$) signal is retained, but is only used on the MC68302 as $\overline{\text{AVEC}}$ to direct the core to use an autovector during interrupt acknowledge cycles.

2.7 MC68302 IMP CONFIGURATION CONTROL

Four reserved entries in the external M68000 exception vector table (see Table 2-5) are used as addresses for internal system configuration registers. These entries are at locations $0F0, $0F4, $0F8, and $0FC. The first entry is the on-chip peripheral base address register (BAR) entry; the second is the on-chip system control register (SCR) entry; the least significant word of the third entry is the clock control register (CKCR), and fourth entry is reserved for future use.

The BAR entry contains the BAR described in this section. The SCR entry contains the SCR described in 3.8.1 System Control Register (SCR). The CKCR entry contains the CKCR register described in 3.9 Clock Control Register.

Figure 2-5 shows all the MC68302 IMP on-chip addressable locations and how they are mapped into system memory.

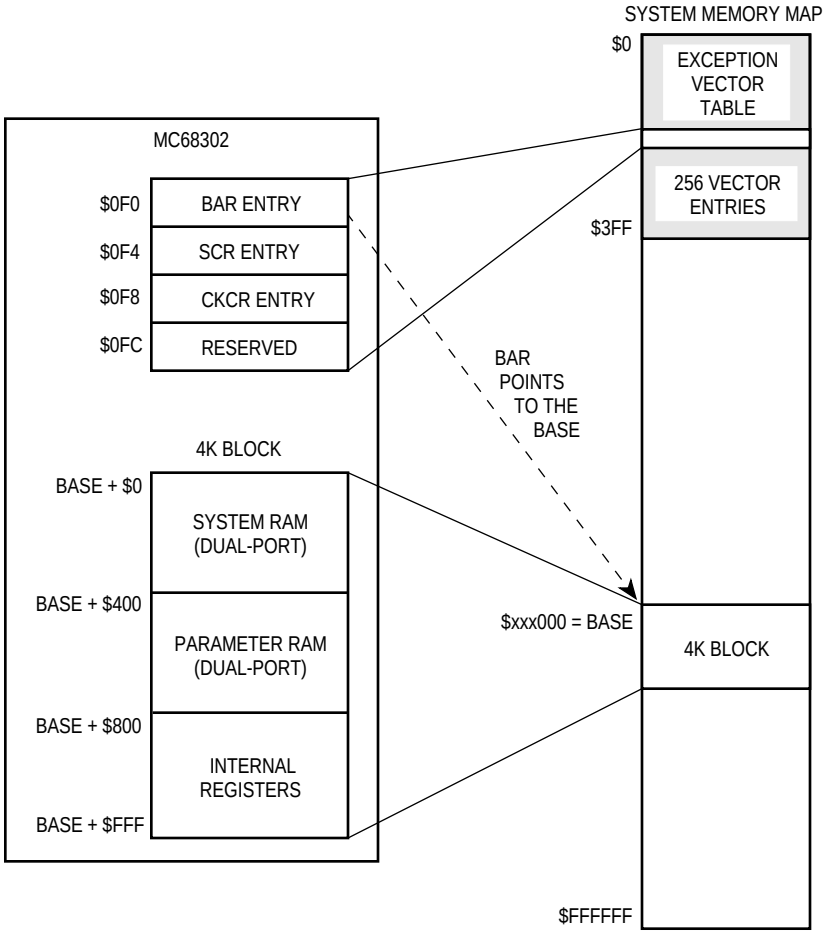


Figure 2-5. MC68302 IMP Configuration Control

The on-chip peripherals, including those peripherals in both the CP and SIB, require a 4K-byte block of address space. This 4K-byte block location is determined by writing the intended base address to the BAR in supervisor data space (FC = 5). The address of the BAR en-

try is $0F0; however, the actual BAR is a 16-bit value within the BAR entry and is located at $0F2.

After a total system reset, the on-chip peripheral base address is undefined, and it is not possible to access the on-chip peripherals at any address until BAR is written. The BAR and the SCR can always be accessed at their fixed addresses.

NOTE

The BAR, SCR and CKCR registers are internally reset only when a total system reset occurs by the simultaneous assertion of RESET and HALT. The chip-select (CS) lines are not asserted on accesses to these locations. Thus, it is very helpful to use CS lines to select external ROM/RAM that overlaps the BAR and SCR register locations, since this prevents potential bus contention. (The internal access (IAC) signal may also be used to prevent bus contention.)

NOTE

In 8-bit system bus operation, IMP accesses are not possible until the low byte of the BAR is written. Since the MOVE.W instruction writes the high byte followed by the low byte, this instruction guarantees the entire word is written.

Do not assign other devices on the system bus an address that falls within the address range of the peripherals defined by the BAR. If this happens, $\overline{\text{BERR}}$ is generated (if the address decode conflict enable (ADCE) bit is set) and the address decode conflict (ADC) bit in the SCR is set.

The BAR is a 16-bit, memory-mapped, read-write register consisting of the high address bits, the compare function code bit, and the function code bits. Upon a total system reset, its value may be read as $BFFF, but its value is not valid until written by the user. The address of this register is fixed at $0F2 in supervisor data space. BAR cannot be accessed in user data space.

15 13	12	11											0
FC2–FC0	CFC	BASE ADDRESS											
		23	22	21	20	19	18	17	16	15	14	13	12

Bits 15–13—FC2–FC0

The FC2–FC0 field is contained in bits 15–13 of the BAR. These bits are used to set the address space of 4K-byte block of on-chip peripherals. The address compare logic uses these bits, dependent upon the CFC bit, to cause an address match within its address space.

NOTE

Do not assign this field to the M68000 core interrupt acknowledge space (FC2–FC0 = 7).

CFC—Compare Function Code

0 = The FC bits in the BAR are ignored. Accesses to the IMP 4K-byte block occur without comparing the FC bits.
1 = The FC bits in the BAR are compared. The address space compare logic uses the FC bits to detect address matches.

Bits 11–0—Base Address

The high address field is contained in bit 11–0 of the BAR. These bits are used to set the starting address of the dual-port RAM. The address compare logic uses only the most significant bits to cause an address match within its block size.

2.8 MC68302 MEMORY MAP

The following tables show the additional registers added to the M68000 to make up the MC68302. All of the registers are memory-mapped. Four entries in the M68000 exception vectors table (located in low RAM) are reserved for addresses of system configuration registers (see Table 2-6) that reside on-chip. These registers have fixed addresses of $0F0–$0FF. All other on-chip peripherals occupy a 4K-byte relocatable address space. When an on-chip register or peripheral is accessed, the internal access (IAC) pin is asserted.

Table 2-6. System Configuration Register

Address	Name	Width	Description	Reset Value
$0F0	RES	16	Reserved	
$0F2*	BAR	16	Base Address Register	BFFF
$0F4*	SCR	32	System Control Register	0000 0F00
$0F8	RES	16	Reserved	
$0FA	CKCR	16	Clock Control Register	0000
$0FC	RES	32	Reserved	

*Reset only upon a total system reset.

The internal 1176-byte dual-port RAM has 576 bytes of system RAM (see Table 2-7) and 576 bytes of parameter RAM (see Table 2-8).

Table 2-7. System RAM

Address	Width	Block	Description
Base + 000 • • • Base + 23F	576 Bytes	RAM	User Data Memory
Base +240 • • • Base + 3FF			Reserved (Not Implemented)

The parameter RAM contains the buffer descriptors for each of the three SCC channels, the SCP, and the two SMC channels. The memory structures of the three SCC channels are

identical. When any SCC, SCP, or SMC channel buffer descriptors or parameters are not used, their parameter RAM area can be used for additional memory. For detailed information about the use of the buffer descriptors and protocol parameters in a specific protocol, see 4.5 Serial Communication Controllers (SCCs). Base + 67E contains the MC68302 revision number. Revision A parts (mask 1B14M) correspond to the value $0001. Revision B parts (mask 2B14M and 3B14M which are described in this manual) correspond to the value $0002. Revision C and D parts have revision number $0003.

Table 2-8. Parameter RAM

Address	Width	Block	Description
Base + 400	4 Word	SCC1	Rx BD 0
Base + 408	4 Word	SCC1	Rx BD 1
Base + 410	4 Word	SCC1	Rx BD 2
Base + 418	4 Word	SCC1	Rx BD 3
Base + 420	4 Word	SCC1	Rx BD 4
Base + 428	4 Word	SCC1	Rx BD 5
Base + 430	4 Word	SCC1	Rx BD 6
Base + 438	4 Word	SCC1	Rx BD 7
Base + 440	4 Word	SCC1	Tx BD 0
Base + 448	4 Word	SCC1	Tx BD 1
Base + 450	4 Word	SCC1	Tx BD 2
Base + 458	4 Word	SCC1	Tx BD 3
Base + 460	4 Word	SCC1	Tx BD 4
Base + 468	4 Word	SCC1	Tx BD 5
Base + 470	4 Word	SCC1	Tx BD 6
Base + 478	4 Word	SCC1	Tx BD 7
Base + 480 • • • Base + 4BF		SCC1 SCC1	Specific Protocol Parameters
Base + 4C0 • • • Base + 4FF			Reserved (Not Implemented)
Base + 500	4 Word	SCC2	Rx BD 0
Base + 508	4 Word	SCC2	Rx BD 1
Base + 510	4 Word	SCC2	Rx BD 2
Base + 518	4 Word	SCC2	Rx BD 3
Base + 520	4 Word	SCC2	Rx BD 4
Base + 528	4 Word	SCC2	Rx BD 5
Base + 530	4 Word	SCC2	Rx BD 6
Base + 538	4 Word	SCC2	Rx BD 7
Base + 540	4 Word	SCC2	Tx BD 0
Base + 548	4 Word	SCC2	Tx BD 1
Base + 550	4 Word	SCC2	Tx BD 2
Base + 558	4 Word	SCC2	Tx BD 3
Base + 560	4 Word	SCC2	Tx BD 4
Base + 568	4 Word	SCC2	Tx BD 5
Base + 570	4 Word	SCC2	Tx BD 6/DRAM Refresh
Base + 578	4 Word	SCC2	Tx BD 7/DRAM Refresh

Table 2-8. Parameter RAM

Base + 580 • • • Base + 5BF		SCC2 SCC2	Specific Protocol Parameters
Base + 5C0 • • • Base + 5FF			Reserved (Not Implemented)
Base + 600 Base + 608 Base + 610 Base + 618 Base + 620 Base + 628 Base + 630 Base + 638 Base + 640 Base + 648 Base + 650 Base + 658 Base + 660 Base + 666 Base + 668 Base + 66A Base + 66C Base + 66E # Base +67A Base +67C Base +67E #	4 Word 4 Word 4 Word 4 Word 4 Word 4 Word 4 Word 4 Word 4 Word 4 Word 4 Word 4 Word 3 Word Word Word Word Word 6 Word Word Word Word	SCC3 SCC3 SCC3 SCC3 SCC3 SCC3 SCC3 SCC3 SCC3 SCC3 SCC3 SCC3 SMC SCC1 SCC1 SCC2 SCC2 SMC1–SMC2 SCP SCC1–SCC3 CP	RxBD0 RxBD1 RxBD2 RxBD3 RxBD4 RxBD5 RxBD6 RxBD7 TxBD0 TxBD1 TxBD2 TxBD3 ## Reserved RxBD TxBD RxBD TxBD Internal Use Rx/TxBD BERR Channel Number MC68302 Revision Number
Base + 680 • • • Base + 6BF		SCC3 SCC3	Specific Protocol Parameters
Base + 6C0 • • • Base + 7FF			Reserved (Not Implemented)

Modified by the CP after a CP or system reset.

Tx BD 4, 5, 6, and 7 are not initially available to SCC3. (See 4.5.5 Buffer Descriptors Table for information on how they may be regained.)

In addition to the internal dual-port RAM, a number of internal registers support the functions of the various M68000 core peripherals. The internal registers (see Table 2-9) are memory-mapped registers offset from the BAR point1616er and are located on the internal M68000 bus.

NOTE

All undefined and reserved bits within registers and parameter RAM values written by the user in a given application should be written with zero to allow for future enhancements to the device.

Table 2-9. Internal Registers

Address	Name	Width	Block	Description	Reset Value
Base + 800	RES	16	IDMA	Reserved	
Base + 802	CMR	16	IDMA	Channel Mode Register	0000
Base + 804	SAPR	32	IDMA	Source Address Pointer	XXXX XXXX
Base + 808	DAPR	32	IDMA	Destination Address Pointer	XXXX XXXX
Base + 80C	BCR	16	IDMA	Byte Count Register	XXXX
! Base + 80E	CSR	8	IDMA	Channel Status Register	00
Base + 80F	RES	8	IDMA	Reserved	
Base + 810	FCR	8	IDMA	Function Code Register	XX
Base + 811	RES	8	IDMA	Reserved	
Base + 812 #	GIMR	16	Int Cont	Global Interrupt Mode Register	0000
! Base + 814	IPR	16	Int Cont	Interrupt Pending Register	0000
Base + 816	IMR	16	Int Cont	Interrupt Mask Register	0000
! Base + 818	ISR	16	Int Cont	In-Service Register	0000
Base + 81A	RES	16	Int Cont	Reserved	
Base + 81C	RES	16	Int Cont	Reserved	
Base + 81E #	PACNT	16	PIO	Port A Control Register	0000
Base + 820 #	PADDR	16	PIO	Port A Data Direction Register	0000
Base + 822 #	PADAT	16	PIO	Port A Data Register	XXXX ##
Base + 824 #	PBCNT	16	PIO	Port B Control Register	0080
Base + 826 #	PBDDR	16	PIO	Port B Data Direction Register	0000
Base + 828 #	PBDAT	16	PIO	Port B Data Register Reserved	XXXX ##
Base + 82A	RES	16	PIO		
Base + 82C	RES	16	CS	Reserved	
Base + 82E	RES	16	CS	Reserved	
Base + 830 #	BR0	16	CS0	Base Register 0	C001
Base + 832 #	OR0	16	CS0	Option Register 0	DFFD
Base + 834 #	BR1	16	CS1	Base Register 1	C000
Base + 836 #	OR1	16	CS1	Option Register 1	DFFD
Base + 838 #	BR2	16	CS2	Base Register 2	C000
Base + 83A #	OR2	16	CS2	Option Register 2	DFFD
Base + 83C #	BR3	16	CS3	Base Register 3	C000
Base + 83E #	OR3	16	CS3	Option Register 3	DFFD

Table 2-9. Internal Registers

Base + 840	TMR1	16	Timer	Timer Unit 1 Mode Register	0000
Base + 842	TRR1	16	Timer	Timer Unit 1 Reference Register	FFFF
Base + 844	TCR1	16	Timer	Timer Unit 1 Capture Register	0000
Base + 846	TCN1	16	Timer	Timer Unit 1 Counter	0000
Base + 848	RES	8	Timer	Reserved	
! Base + 849	TER1	8	Timer	Timer Unit 1 Event Register	00
Base + 84A	WRR	16	WD	Watchdog Reference Register	FFFF
Base + 84C	WCN	16	WD	Watchdog Counter	0000
Base + 84E	RES	16	Timer	Reserved	
Base + 850	TMR2	16	Timer	Timer Unit 2 Mode Register	0000
Base + 852	TRR2	16	Timer	Timer Unit 2 Reference Register	FFFF
Base + 854	TCR2	16	Timer	Timer Unit 2 Capture Register	0000
Base + 856	TCN2	16	Timer	Timer Unit 2 Counter	0000
Base + 858	RES	8	Timer	Reserved	
! Base + 859	TER2	8	Timer	Timer Unit 2 Event Register	00
Base + 85A	RES	16	Timer	Reserved	
Base + 85C	RES	16	Timer	Reserved	
Base + 85E	RES	16	Timer	Reserved	
Base + 860	CR	8	CP	Command Register	00
Base + 861 • • • Base + 87F				Reserved (Not Implemented)	
Base + 880	RES	16	SCC1	Reserved	
Base + 882	SCON1	16	SCC1	SCC1 Configuration Register	0004
Base + 884	SCM1	16	SCC1	SCC1 Mode Register	0000
Base + 886	DSR1	16	SCC1	SCC1 Data Sync. Register	7E7E
! Base + 888	SCCE1	8	SCC1	SCC1 Event Register	00
Base + 889	RES	8	SCC1	Reserved	
Base + 88A	SCCM1	8	SCC1	SCC1 Mask Register	00
Base + 88B	RES	8	SCC1	Reserved	
Base + 88C	SCCS1	8	SCC1	SCC1 Status Register	00
Base + 88D	RES	8	SCC1	Reserved	
Base + 88E	RES	16	SCC1	Reserved	
Base + 890	RES	16	SCC2	Reserved	
Base + 892	SCON2	16	SCC2	SCC2 Configuration Register	0004
Base + 894	SCM2	16	SCC2	SCC2 Mode Register	0000
Base + 896	DSR2	16	SCC2	SCC2 Data Sync. Register	7E7E
! Base + 898	SCCE2	8	SCC2	SCC2 Event Register	00
Base + 899	RES	8	SCC2	Reserved	
Base + 89A	SCCM2	8	SCC2	SCC2 Mask Register	00
Base + 89B	RES	8	SCC2	Reserved	
Base + 89C	SCCS2	8	SCC2	SCC2 Status Register	00
Base + 89D	RES	8	SCC2	Reserved	
Base + 89E	RES	16	SCC2		

Table 2-9. Internal Registers

Base + 8A0	RES	16	SCC3	Reserved	
Base + 8A2	SCON3	16	SCC3	SCC3 Configuration Register	0004
Base + 8A4	SCM3	16	SCC3	SCC3 Mode Register	0000
Base + 8A6	DSR3	16	SCC3	SCC3 Data Sync. Register	7E7E
! Base + 8A8	SCCE3	8	SCC3	SCC3 Event Register	00
Base + 8A9	RES	8	SCC3	Reserved	
Base + 8AA	SCCM3	8	SCC3	SCC3 Mask Register	00
Base + 8AB	RES	8	SCC3	Reserved	
Base + 8AC	SCCS3	8	SCC3	SCC3 Status Register	00
Base + 8AD	RES	8	SCC3	Reserved	
Base + 8AE	RES	16	SCC3	Reserved	
Base + 8B0	SPMODE	16	SCM	SCP, SMC Mode and Clock Control Register	0000
Base + 8B2 #	SIMASK	16	SI	Serial Interface Mask Register	FFFF
Base + 8B4 #	SIMODE	16	SI	Serial Interface Mode Register	0000
Base + 8B6 • • • Base + FFF				Reserved (Not Implemented)	

\# Reset only upon a total system reset ($\overline{\text{RESET}}$ and $\overline{\text{HALT}}$ assert together), but not on the execution of an M68000 RESET instruction. See the RESET pin description for details.

The output latches are undefined at total system reset.

! Event register with special properties (see 2.9 Event Registers).

2.9 EVENT REGISTERS

The IMP contains a few special registers designed to report events to the user. They are the channel status register (CSR) in the independent DMA, the interrupt pending register (IPR) and interrupt in-service register (ISR) in the interrupt controller, the timer event register 1 (TER1) in timer 1, the TER2 in timer 2, serial communication controller event register 1 (SCCE1) in SCC1, SCCE2 in SCC2, and SCCE3 in SCC3. Events in these register are always reported by a bit being set.

During the normal course of operation, the user software will clear these events after recognizing them. To clear a bit in one of these registers, the user software must WRITE A ONE TO THAT BIT. Writing a zero has no effect on the register. Thus, in normal operation, the hardware only *sets* bits in these registers; whereas, the software only *clears* them.

This technique prevents software from inadvertently losing the indication from an event bit that is “set” by the hardware between the software read and the software write of this register.

All these registers are cleared after a total system reset ($\overline{\text{RESET}}$ and $\overline{\text{HALT}}$ asserted together) and after the M68000 RESET instruction. Also some of the blocks (IDMA, timer1, timer2, and communication processor) have a reset (RST) bit located in a register in that block. This RST bit will reset that entire block, including any event registers contained therein.

Examples:

1. To clear bit 0 of SCCE1, execute "MOVE.B #$01,SCCE1"

2. To clear bits 0 and 1 of SCC1, execute "MOVE.B #$03,SCCE1”
3. To clear all bits in SCCE1, execute "MOVE.B #$ff,SCCE1"

where SCCE1 is equated to the actual address of SCCE1.

NOTE

DO NOT use read-modify-write instructions to clear bits in an event register, or ALL bits in that register will inadvertently be cleared. Read-modify-write instructions include BSET, BCLR, AND, OR, etc. These instructions read the contents of a location, perform an operation, and write the result back, leaving the rest of the bits unchanged. Thus, if a bit is a one when read, it will be written back with a one, clearing that bit. For example, the instruction “BSET.B #0,SCCE1” will actually clear ALL bits in SCCE1, not just bit 0.

SECTION 3
SYSTEM INTEGRATION BLOCK (SIB)

The MC68302 contains an extensive SIB that simplifies the job of both the hardware and software designer. It integrates the M68000 core with the most common peripherals used in an M68000-based system. The independent direct memory access (IDMA) controller relieves the hardware designer of the extra effort and board logic needed to connect an external DMA controller. The interrupt controller can be used in a dedicated mode to generate interrupt acknowledge signals without external logic. Also, the chip-select signals and their associated wait-state logic eliminate the need to generate chip-select signals externally. The three timers simplify control and improve reliability. These and other features in the SIB conserve board space and cost while decreasing development time.

The SIB includes the following functions:

- IDMA Controller with Three Handshake Signals: $\overline{\text{DREQ}}$, $\overline{\text{DACK}}$, and $\overline{\text{DONE}}$
- Interrupt Controller with Two Modes of Operation
- Parallel Input/Output (I/O) Ports, Some with Interrupt Capability
- On-Chip 1152-Byte Dual-Port RAM
- Three Timers Including a Software Watchdog Timer
- Four Programmable Chip-Select Lines with Wait-State Generator Logic
- On-Chip Clock Generator with Output Signal
- System Control

  —System Status and Control Logic
  —Disable CPU Logic (M68000)
  —Bus Arbitration Logic with Low-Interrupt Latency Support
  —Hardware Watchdog for Monitoring Bus Activity
  —Low-Power (Standby) Modes
  —Freeze Control for Debugging
- Clock Control

  —Adjustable CLKO Drive
  —Three-state RCLK1 and TCLK1
  —Disable BRG1
- DRAM Refresh Controller

3.1 DMA CONTROL

The IMP includes seven on-chip DMA channels, six serial DMA (SDMA) channels for the three serial communications controllers (SCCs) and one IDMA. The SDMA channels are discussed in 4.2 SDMA Channels. The IDMA is discussed in the following paragraphs.

3.1.1 Key Features

The IDMA (Independent DMA Controller) has the following key features:

- Two Address Pointers and One Counter
- Support of Memory-to-Memory, Peripheral-to-Memory, and Memory-to-Peripheral Data Transfers
- Three I/O Lines, $\overline{\text{DREQ}}$, $\overline{\text{DACK}}$, and $\overline{\text{DONE}}$, for Externally Requested Data Transfers
- Asynchronous M68000 Bus Structure with 24-Bit Address and 8-Bit or 16-Bit Data Bus
- Support for Data Blocks Located at Even or Odd Addresses
- Packing and Unpacking of Operands
- Fast Transfer Rates: Up to 4M bytes/second at 16.0 MHz with No Wait States
- Full Support of All M68000 Bus Exceptions: Halt, Bus Error, Reset, and Retry
- Flexible Request Generation:

  —Internal, Maximum Rate (One Burst)
  —Internal, Limited Rate (Limited Burst Bandwidth)
  —External, Burst ($\overline{\text{DREQ}}$ Level Sensitive)
  —External, Cycle Steal ($\overline{\text{DREQ}}$ Edge Sensitive)

The one general-purpose IDMA controller can operate in different modes of data transfer as programmed by the user. The IDMA is capable of transferring data between any combination of memory and I/O. In addition, data may be transferred in either byte or word quantities, and the source and destination addresses may be either odd or even. Note that the chip select and wait state generation logic on the MC68302 may be used with the IDMA, if desired.

Every IDMA cycle requires between two and four bus cycles, depending on the address boundary and transfer size. Each bus cycle is a standard M68000-type read or write cycle. If both the source and destination addresses are even, the IDMA fetches one word of data and immediately deposits it. If either the source or destination address begins on an odd boundary, the transfer is handled differently. For example, if the source address starts on an odd boundary and the destination address is even, the IDMA reads one byte from the source, then reads the second byte from the source, and finally stores the word in a single access. If the source is even and the destination odd, then the IDMA will read one word from the source and store it in two consecutive cycles. If both the source and destination are odd, the IDMA performs two read byte cycles followed by two write byte cycles until the transfer is complete.

If the IMP frequency is 16.0 MHz and zero wait state memory is used, then the maximum transfer rate is 4M byte/sec. This assumes that the operand size is 16-bits, the source and destination addresses are even, and the bus width is selected to be 16-bits.

The maximum transfer rate is calculated from the fact that 16 bits are moved every 8 clocks. The calculation is as follows:

$$\frac{\text{16 bits x 16M clocks/sec}}{\text{(2 bus cycles) x (4 clocks/bus cycle)}} = \frac{\text{2 bytes x 16M clocks/sec}}{\text{8 clocks}} = \frac{\text{4M bytes}}{\text{sec}}$$

The IDMA controller block diagram is shown in Figure 3-1.

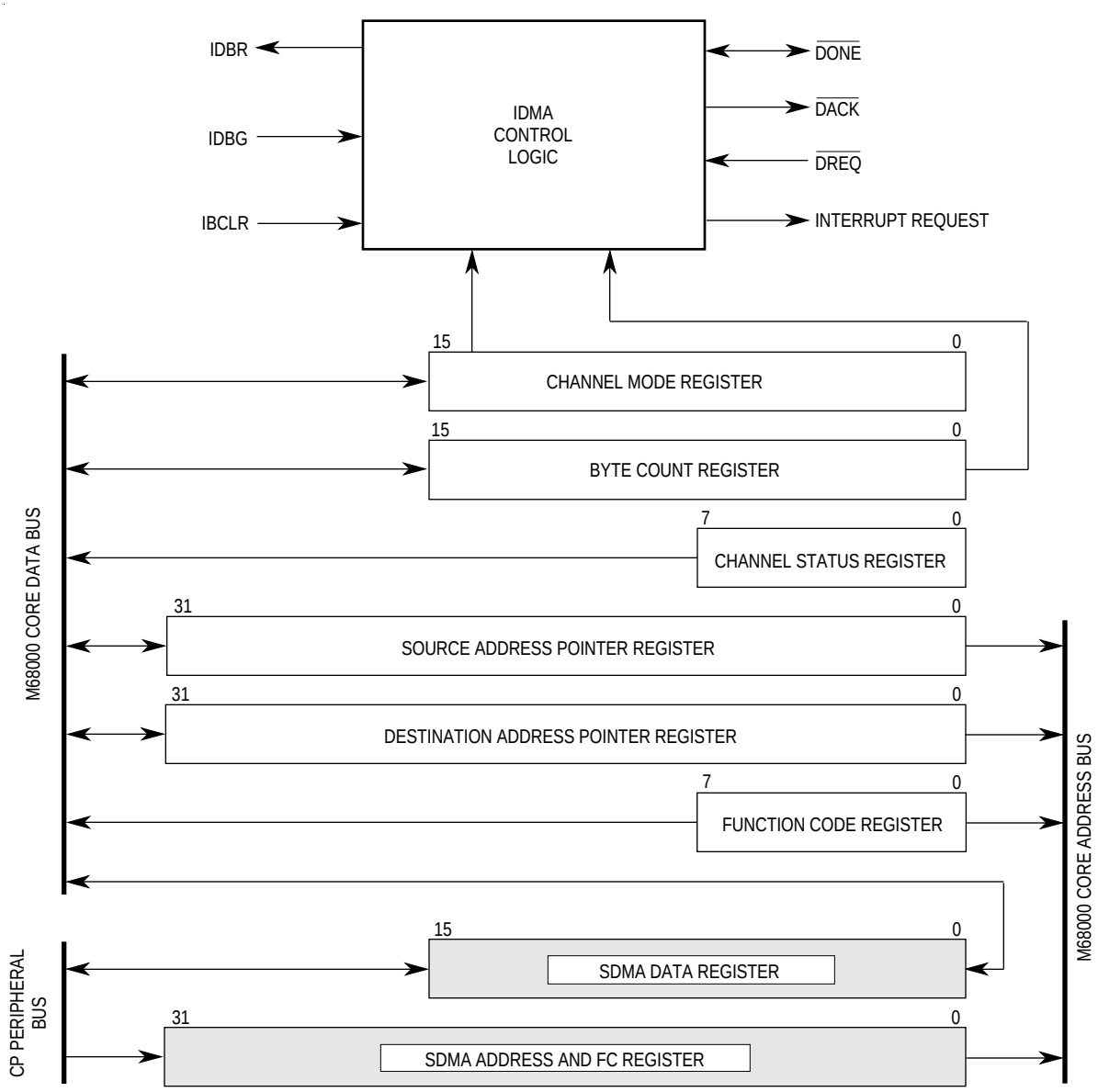


Figure 3-1. IDMA Controller Block Diagram

3.1.2 IDMA Registers (Independent DMA Controller)

The IDMA has six registers that define its specific operation. These registers include a 32-bit source address pointer register (SAPR), a 32-bit destination address pointer register

(DAPR), an 8-bit function code register (FCR), a 16-bit byte count register (BCR), a 16-bit channel mode register (CMR), and an 8-bit channel status register (CSR). These registers provide the addresses, transfer count, and configuration information necessary to set up a transfer. They also provide a means of controlling the IDMA and monitoring its status. All registers can be modified by the M68000 core. The IDMA also includes another 16-bit register, the data holding register (DHR), which is not accessible to the M68000 core and is used by the IDMA for temporary data storage.

3.1.2.1 Channel Mode Register (CMR)

The CMR, a 16-bit register, is reset to $0000.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	ECO	INTN	INTE	REQG		SAPI	DAPI	SSIZE		DSIZE		BT		RST	STR

Bit 15—Reserved for future use.

ECO—External Control Option

0 = If the request generation is programmed to be external in the REQG bits, the control signals ($\overline{\text{DACK}}$ and $\overline{\text{DONE}}$) are used in the source (read) portion of the transfer since the peripheral is the source.

1 = If the request generation is programmed to be external in the REQG bits, the control signals ($\overline{\text{DACK}}$ and $\overline{\text{DONE}}$) are used in the destination (write) portion of the transfer since the peripheral is the destination.

INTN—Interrupt Normal

0 = When the channel has completed an operand transfer without error conditions as indicated by $\overline{\text{DONE}}$, the channel does not generate an interrupt request to the IMP interrupt controller. The DONE bit remains set in the CSR.

1 = When the channel has completed an operand transfer without error conditions as indicated by $\overline{\text{DONE}}$, the channel generates an interrupt request to the IMP interrupt controller and sets DONE in the CSR.

NOTE

An interrupt will only be generated if the IDMA bit is set in the interrupt mask register (IMR).

INTE—Interrupt Error

0 = If a bus error occurs during an operand transfer either on the source read (BES) or the destination write (BED), the channel does not generate an interrupt to the IMP interrupt controller. The appropriate bit remains set in the CSR.

1 = If a bus error occurs during an operand transfer either on BES or BED, the channel generates an interrupt to the IMP interrupt controller and sets the appropriate bit (BES or BED) in the CSR.

NOTE

An interrupt will only be generated if the IDMA bit is set in the IMR.

REQG—Request Generation

The following decode shows the definitions for the REQG bits:

00 = Internal request at limited rate (limited burst bandwidth) set by burst transfer (BT) bits
01 = Internal request at maximum rate (one burst)
10 = External request burst transfer mode ($\overline{\text{DREQ}}$ level sensitive)
11 = External request cycle steal ($\overline{\text{DREQ}}$ edge sensitive)

SAPI—Source Address Pointer (SAP) Increment

0 = SAP is not incremented after each transfer.
1 = SAP is incremented by one or two after each transfer, according to the source size (SSIZE) bits and the starting address.

DAPI—Destination Address Pointer (DAP) Increment

0 = DAP is not incremented after each transfer.
1 = DAP is incremented by one or two after each transfer, according to the destination size (DSIZE) bits and the starting address.

SSIZE—Source Size

The following decode shows the definitions for the SSIZE bits.

00 = Reserved
01 = Byte
10 = Word
11 = Reserved

DSIZE—Destination Size

The following decode shows the definitions for the DSIZE bits.

00 = Reserved
01 = Byte
10 = Word
11 = Reserved

BT—Burst Transfer

The BT bits control the maximum percentage of the M68000 bus that the IDMA can use during each 1024 clock cycle period following the enabling of the IDMA. The IDMA runs for a consecutive number of cycles up to its burst transfer percentage if bus clear ($\overline{\text{BCLR}}$) is not asserted and the BCR is greater than zero. The following decode shows these percentages.

00 = IDMA gets up to 75% of the bus bandwidth.
01 = IDMA gets up to 50% of the bus bandwidth.
10 = IDMA gets up to 25% of the bus bandwidth.
11 = IDMA gets up to 12.5% of the bus bandwidth.

NOTE

These percentages are valid only when using internal limited request generation (REQG = 00).

RST—Software Reset

This bit will reset the IDMA to the same state as an external reset. The IDMA clears RST when the reset is complete.

0 = Normal operation
1 = The channel aborts any external pending or running bus cycles and terminates channel operation. Setting RST clears all bits in the CSR and CMR.

STR—Start Operation

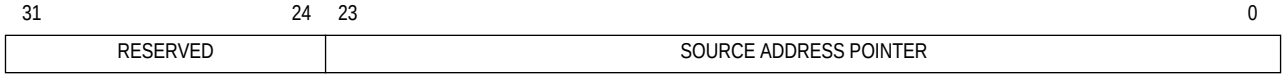
This bit starts the IDMA transfer if the REQG bits are programmed for an internal request. (The IDMA begins requesting the M68000 bus one clock after STR is set.) If the REQG bits are programmed for an external request, this bit must be set before the IDMA will recognize the first request on the $\overline{\text{DREQ}}$ input.

0 = Stop channel; clearing this bit will cause the IDMA to stop transferring data at the end of the current operand transfer. The IDMA internal state is not altered.
1 = Start channel; setting this bit will allow the IDMA to start (or continue if previously stopped) transferring data.

NOTE

STR is cleared automatically when the transfer is complete.

3.1.2.2 Source Address Pointer Register (SAPR)



The SAPR is a 32-bit register.

The SAPR contains 24 (A23–A0) address bits of the source operand used by the IDMA to access memory or memory-mapped peripheral controller registers. During the IDMA read cycle, the address on the master address bus is driven from this register. The SAPR may be programmed by the SAPI bit to be incremented or remain constant after each operand transfer.

The register is incremented using unsigned arithmetic and will roll over if an overflow occurs. For example, if a register contains $00FFFFFF and is incremented by one, it will roll over to $00000000. This register can be incremented by one or two, depending on the SSIZE bit and the starting address in this register.

3.1.2.3 Destination Address Pointer Register (DAPR)

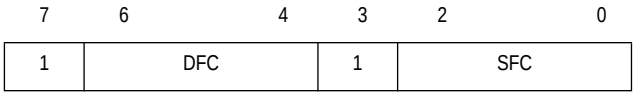
The DAPR is a 32-bit register.

The DAPR contains 24 (A23–A0) address bits of the destination operand used by the IDMA to access memory or memory-mapped peripheral controller registers. During the IDMA write cycle, the address on the master address bus is driven from this register. The DAPR may be programmed by the DAPI bit to be incremented or remain constant after each operand transfer.

The register is incremented using unsigned arithmetic and will roll over if overflow occurs. For example, if a register contains $00FFFFFF and is incremented by one, it will roll over to $00000000. This register can be incremented by one or two depending on the DSIZE bit and the starting address.

3.1.2.4 Function Code Register (FCR)

The FCR is an 8-bit register.



The SFC and the DFC bits define the source and destination function code values that are output by the IDMA and the appropriate address registers during an IDMA bus cycle. The address space on the function code lines may be used by an external memory management unit (MMU) or other memory-protection device to translate the IDMA logical addresses to proper physical addresses. The function code value programmed into the FCR is placed on pins FC2–FC0 during a bus cycle to further qualify the address bus value.

NOTE

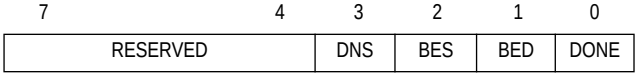
This register is undefined following power-on reset. The user should always initialize it and should not use the function code value “111” in this register.

3.1.2.5 Byte Count Register (BCR)

This 16-bit register specifies the amount of data to be transferred by the IDMA; up to 64K bytes (BCR = 0) is permitted. This register is decremented once for each byte transferred successfully. BCR may be even or odd as desired. DMA activity will terminate as soon as this register reaches zero. Thus, an odd number of bytes may be transferred in a 16-bit operand scenario.

3.1.2.6 Channel Status Register (CSR)

The CSR is an 8-bit register used to report events recognized by the IDMA controller. On recognition of an event, the IDMA sets its corresponding bit in the CSR (regardless of the INTE and INTN bits in the CMR). The CSR is a memory-mapped register which may be read at any time. A bit is cleared by writing a one and is left unchanged by writing a zero. More than one bit may be cleared at a time, and the register is cleared at reset.



Bits 7–4—These bits are reserved for future use.

DNS—Done Not Synchronized

This bit is set if operand packing is performed between 16-bit memory and an 8-bit peripheral and the $\overline{\text{DONE}}$ signal is asserted as an input to the IDMA (i.e., by the peripheral) during the first access of the 8-bit peripheral. In such a case, the IDMA will still attempt to finish the second access of the 8-bit peripheral even though $\overline{\text{DONE}}$ has been asserted (the access could be blocked with external logic); however, the DNS bit will be set to signify this condition. DNS will not be set if the transfer is terminated by an odd byte count, since, in this case, the exact number of requested bytes will be transferred by the IDMA.

BES—Bus Error Source

This bit indicates that the IDMA channel terminated with an error returned during the read cycle. The channel terminates the IDMA operation without setting DONE. BES is cleared by writing a one or by setting RST in the CMR. Writing a zero has no effect on BES.

BED—Bus Error Destination

This bit indicates that the IDMA channel terminated with an error during the write cycle. The channel terminates the IDMA operation without setting DONE. BED is cleared by writing a one or by setting RST in the CMR. Writing a zero has no effect on BED.

DONE—Normal Channel Transfer Done

This bit indicates that the IDMA channel has terminated normally. Normal channel termination is defined as 1) having decremented the BCR to zero with no errors occurring during any IDMA transfer bus cycle or 2) by the external peripheral asserting $\overline{\text{DONE}}$ with no errors occurring during any IDMA transfer bus cycle. DONE will not be set if the channel terminates due to an error. DONE is cleared by writing a one or by a software RST in the CMR. Writing a zero has no effect on this bit.

3.1.3 Interface Signals

The IDMA channel has three dedicated control signals: DMA request ($\overline{\text{DREQ}}$), DMA acknowledge ($\overline{\text{DACK}}$), and end of IDMA transfer ($\overline{\text{DONE}}$). The IDMA's use of the bus arbitration signals is described in 3.1.6 DMA Bus Arbitration. The peripheral used with these signals may be either a source or a destination of the transfers.

3.1.3.1 $\overline{\text{DREQ}}$ and $\overline{\text{DACK}}$

These are handshake signals between the peripheral requiring service and the IMP. When the peripheral requires IDMA service, it asserts $\overline{\text{DREQ}}$, and the IMP begins the IDMA process. When the IDMA service is in progress, $\overline{\text{DACK}}$ is asserted during accesses to the device. These signals are not used when the IDMA is programmed to internal request modes.

3.1.3.2 $\overline{\text{DONE}}$

This bidirectional signal is used to indicate the last IDMA transfer. With internal request modes, the IDMA activates $\overline{\text{DONE}}$ as an output during the last IDMA bus cycle. If DONE is externally asserted during internal request modes, the IDMA transfer is terminated. With external request modes, $\overline{\text{DONE}}$ may be used as an input to the IDMA controller indicating that the device being serviced requires no more transfers and that the transmission is to be terminated. $\overline{\text{DONE}}$ is an output if the transfer count is exhausted.

3.1.4 IDMA Operational Description

Every IDMA operation involves the following steps: IDMA channel initialization, data transfer, and block termination. In the initialization phase, the M68000 core (or external processor) loads the registers with control information, address pointers and transfer count, and then starts the channel. In the transfer phase, the IDMA accepts requests for operand transfers and provides addressing and bus control for the transfers. The termination phase occurs when the operation is complete and the IDMA interrupts the M68000 core, if interrupts are enabled.

3.1.4.1 Channel Initialization

To start a block transfer operation, the M68000 core must initialize IDMA registers with information describing the data block, device type, request generation method, and other special control options. See 3.1.2 IDMA Registers (Independent DMA Controller) and 3.1.5 IDMA Programming for further details.

3.1.4.2 Data Transfer

The IDMA supports dual address transfers only. Thus, each operand transfer consists of a source operand read and a destination operand write. The source operand is read from the address contained in the SAPR into the DHR. When the source and destination operand sizes differ, the operand read may take up to two bus cycles to complete. The operand is then written to the address contained in the DAPR. Again, this transfer may be up to two bus cycles long. In this manner, various combinations of peripheral, memory, and operand sizes may be used.

NOTE

When the SAPR and DAPR are programmed not to increment and the bus width is 16 bits, the SAPR and DAPR addresses must be even.

Source Operand Read

During this cycle, the SAPR drives the address bus, the FCR drives the source function codes, and the CMR drives the size control. The data is read from memory or the peripheral and placed temporarily into the data holding register (DHR) when the bus cycle is terminated with $\overline{\text{DTACK}}$. When the complete operand has been read, the SAPR is incremented by one or two, depending on the address and size information. See 3.1.2.2 Source Address Pointer Register (SAPR) for more details.

Destination Operand Write

During this cycle, the data in DHR is written to the device or memory selected by the address from the DAPR, using the destination function codes from the FCR and the size from the CMR. The same options exist for operand size and alignment as for the source operand read. When the complete operand is written, the DAPR is incremented by one or two, and the BCR is decremented by the number of bytes transferred. See 3.1.2.3 Destination Address Pointer Register (DAPR) and 3.1.2.5 Byte Count Register (BCR) for more details.

3.1.4.3 Address Sequencing

The manner in which the DAPR and SAPR are incremented during a transfer depends on the programming of the SAPI and DAPI bits, the source and destination sizes (DSIZE and SSIZE), and the system data bus width.

The IDMA will run at least two, and up to four, bus cycles to transfer each operand. With an 8-bit bus width, SSIZE and DSIZE are ignored, and each operand transfer requires two cycles. With a 16-bit bus width, the number of bus cycles required to transfer each operand is determined by DSIZE and SSIZE, whether the source and destination addresses are odd or even, and whether the BCR equals one. When SSIZE and DSIZE both select either a byte or word, there will be no operand packing, and the operand transfer will take two bus cycles. One exception occurs when DSIZE and SSIZE are words and the address is odd. In this case, there will be two (one byte each) memory cycles for each read or write at an odd address. When both the source and destination addresses are odd, four bus cycles are required to transfer each operand. When SSIZE and DSIZE are not equal, the IDMA will perform operand packing. If SSIZE is one byte, two read cycles are required to fetch the operand. If DSIZE is one byte, two write cycles are required to store the operand.

When SAPI and/or DAPI are programmed to increment either SAPR or DAPR, the amount (one or two) by which the address pointer increments depends upon DSIZE, SSIZE, and the bus width.

When operating in a 16-bit bus environment with an 8-bit peripheral, the peripheral may be placed on one-half of the bus (consecutive even or odd addresses only). In this case, SSIZE (or DSIZE) must be set to 16 bit, and the IDMA will perform data packing. As a result, the peripheral's addresses must be incremented twice after each peripheral bus cycle, which results in adding four to the address for each data transfer (two cycles per transfer). This is consistent with the M68000 MOVEP instruction. If the 8-bit peripheral is to be arranged with consecutive addresses, both SSIZE and DSIZE must be 8 bit.

Refer to Table 3-1 to see how the SAPR and DAPR will be incremented in all combinations.

Table 3-1. SAPR and DAPR Incrementing Rules

Bus Width	Source Size	Destination Size	SAPR Increment	DAPR Increment	Transfer Description
8 Bit	X	X	+1	+1	Read Byte—Write Byte Packing Is Not Possible
16 Bit	Byte	Byte	+1	+1	Read Byte—Write Byte Packing Is Not Desired
16 Bit	Byte	Word	+4	+2	Read Byte, Read Byte —Write Word Operand Packing
16 Bit	Word	Byte	+2	+4	Read Word—Write Byte, Write Byte Operand Unpacking
16 Bit	Word	Word	+2	+2	Read Word—Write Word

Refer toTable 3-2 for more details on the IDMA bus cycles.

Table 3-2. IDMA Bus Cycles

Source Size	Source Address	Destination Size	Destination Address	Cycles 8-bit Bus	Cycles 16-bit Bus
8	X	8	X	RW	RW
8	X	16	Even	RWRW*	RRW
8	X	16	Odd	RWRW*	RRWW
16	Even	8	X	RWRW*	RWW
16	Odd	8	X	RWRW*	RRWW
16	Even	16	Even	RWRW*	RW
16	Even	16	Odd	RWRW*	RWW
16	Odd	16	Even	RWRW*	RRW
16	Odd	16	Odd	RWRW*	RRWW

* - Considered as 2 operands.

3.1.4.4 Transfer Request Generation

IDMA transfers may be initiated by either internally or externally generated requests. Internally generated requests can be initiated by setting STR in the CMR. Externally generated transfers are those requested by an external device using $\overline{\text{DREQ}}$ in conjunction with the activation of STR.

Internal Maximum Rate

The first method of internal request generation is a nonstop transfer until the transfer count is exhausted. If this method is chosen, the IDMA will arbitrate for the bus and begin transferring data after STR is set and the IDMA becomes the bus master. If no exception occurs, all operands in the data block will be transferred in sequential bus cycles with the IDMA using 100 percent of the available bus bandwidth (unless an external bus master requests the bus or the M68000 core has an unmasked pending interrupt request and BCLM = 1). See 3.1.6 DMA Bus Arbitration for more details.

Internal Limited Rate

To guarantee that the IDMA will not use all the available system bus bandwidth during a transfer, internal requests can be limited to the amount of bus bandwidth allocated to the IDMA. Programming the REQG bits to “internal limited rate” and the BT bits to limit the percentage of bandwidth achieves this result. As soon as STR is set, the IDMA module arbitrates for the bus and begins to transfer data when it becomes bus master. If no exception occurs, transfers will continue uninterrupted, but the IDMA will not exceed the percentage of bus bandwidth programmed into the control register (12.5%, 25%, 50%, or 75%). This percentage is calculated over each ensuing 1024 internal clock cycle period.

For example, if 12.5% is chosen, the IDMA will attempt to use the bus for the first 128 clocks of each 1024 clock cycle period. However, because of other bus masters, the IDMA may not be able to take its 128 clock allotment in a single burst.

External Burst Mode

For external devices requiring very high data transfer rates, the external burst mode allows the IDMA to use all the bus bandwidth to service the device. In the burst mode, the

$\overline{\text{DREQ}}$ input to the IDMA is level-sensitive and is sampled at certain points to determine when a valid request is asserted by the device. The device requests service by asserting $\overline{\text{DREQ}}$ and leaving it asserted. In response, the IDMA arbitrates for the system bus and begins to perform an operand transfer. During each access to the device, the IDMA will assert $\overline{\text{DACK}}$ to indicate to the device that a request is being serviced. If $\overline{\text{DREQ}}$ remains asserted when the IDMA completes the peripheral cycle (the cycle during which $\overline{\text{DACK}}$ is asserted by the IDMA) one setup time (see specification. 80) before the S5 falling edge (i.e., before or with $\overline{\text{DTACK}}$), then a valid request for another operand transfer is recognized, and the IDMA will service the next request immediately. If $\overline{\text{DREQ}}$ is negated one setup time (see specification 80) before the S5 falling edge, a new request will not be recognized, and the IDMA will relinquish the bus.

NOTE:

If 8 to 16 bit packing occurs, then the $\overline{\text{DREQ}}$ is sampled during the last 8-bit cycle.

External Cycle Steal

For external devices that generate a pulsed signal for each operand to be transferred, the external cycle steal mode uses $\overline{\text{DREQ}}$ as a falling edge-sensitive input. The IDMA will respond to cycle-steal requests in the same manner as for all other requests. However, if subsequent $\overline{\text{DREQ}}$ pulses are generated before $\overline{\text{DACK}}$ is asserted in response to each request, they will be ignored. If $\overline{\text{DREQ}}$ is asserted after the IDMA asserts $\overline{\text{DACK}}$ for the previous request but one setup time (see specification 80) before the S5 falling edge, then the new request will be serviced before the bus is relinquished. If a new request has not been generated by one setup time (see specification 80) before the S5 falling edge, the bus will be released to the next bus master.

3.1.4.5 Block Transfer Termination

The user may stop the channel by clearing STR. Additionally, the channel operation can be terminated for any of the following reasons: transfer count exhausted, external device termination, or error termination. This is independent of how requests are generated to the IDMA.

Transfer Count Exhausted

When the channel begins an operand transfer, if the current value of the BCR is one or two (according to the operand size in the CMR), $\overline{\text{DONE}}$ is asserted during the last bus cycle to the device to indicate that the channel operation will be terminated when the current operand transfer has successfully completed. In the memory to memory case, $\overline{\text{DONE}}$ is asserted during the last access to memory (source or destination) as defined by the ECO bit. When the operand transfer has completed and the BCR has been decremented to zero, the channel operation is terminated, STR is cleared, and an interrupt is generated if INTN is set. The SAPR and/or DAPR are also incremented in the normal fashion.

NOTE

If the channel is started with BCR value set to zero, the channel will transfer 64K bytes.

External Device Termination

If desired, a transfer may be terminated by the device even before the BCR is decremented to zero. If $\overline{\text{DONE}}$ is asserted one setup time prior to the S5 falling edge (i.e., before or with $\overline{\text{DTACK}}$) during a device access, then the channel operation will be terminated following the operand transfer (see the DNS bit in the CSR). STR is cleared, and an interrupt is generated if INTN is set. The BCR is also decremented, and the SAPR and/or DAPR are incremented in the normal fashion. The use of DONE is not limited to external request generation only; it may also be used to externally terminate an internally generated IDMA transfer sequence.

Error Termination

When a fatal error occurs during an IDMA bus cycle, a bus error is used to abort the cycle and terminate the channel operation. STR is cleared, either BED or BES is set, and an error interrupt is generated if INTE is set.

3.1.5 IDMA Programming

Once the channel has been initialized with all parameters required for a transfer operation, it is started by setting the start operation (STR) bit in the CMR. After the channel has been started, any register that describes the current operation may be read but not modified (SAPR/DAPR, FCR, or BCR).

Once STR has been set, the channel is active and either accepts operand transfer requests in external mode or generates requests automatically in internal mode. When the first valid external request is recognized, the IDMA arbitrates for the bus. The $\overline{\text{DREQ}}$ input is ignored until STR is set.

STR is cleared automatically when the BCR reaches zero and the channel transfer is either terminated by $\overline{\text{DONE}}$ or the IDMA cycle is terminated by a bus error.

Channel transfer operation may be suspended at any time by clearing STR. In response, any operand transfer in progress will be completed, and the bus will be released. No further bus cycles will be started while STR remains negated. During this time, the M68000 core may access IDMA internal registers to determine channel status or to alter operation. When STR is set again, if a transfer request is pending, the IDMA will arbitrate for the bus and continue normal operation.

Interrupt handling for the IDMA is configured globally through the interrupt pending register (IPR), the IMR, and the interrupt in-service register (ISR). Within the CMR in the IDMA, two bits are used to either mask or enable the presence of an interrupt reported in the CSR of the IDMA. One bit is used for masking normal termination; the other bit is used for masking error termination. When these interrupt mask bits in the CMR (INTN and INTE) are cleared and the IDMA status changes, status bits are set in the CSR but not in the IPR. When either INTN or INTE is set and the corresponding event occurs, the appropriate bit is set in the IPR, and, if this bit is not masked, the interrupt controller will interrupt the M68000 core.

3.1.6 DMA Bus Arbitration

The IDMA controller uses the M68000 bus arbitration protocol to request bus mastership before entering the DMA mode of operation. The six SDMA channels have priority over the IDMA and can transfer data between any two IDMA bus cycles with $\overline{\text{BGACK}}$ remaining continuously low. Once the processor has initialized and started a DMA channel, an operand transfer request is made pending by either an external device or by using an internal request.

When the IDMA channel has an operand transfer request pending and $\overline{\text{BCLR}}$ is not asserted, the IDMA will request bus mastership from the internal bus arbiter using the internal signal IDBR (see Figure 3-12). The arbiter will assert the internal M68000 core bus request ($\overline{\text{CBR}}$) signal and will monitor the core bus grant ($\overline{\text{CBG}}$) and external $\overline{\text{BR}}$ to determine when it may grant the IDMA mastership. The IDMA will monitor the address strobe ($\overline{\text{AS}}$), $\overline{\text{HALT}}$, bus error ($\overline{\text{BERR}}$), and bus grant acknowledge ($\overline{\text{BGACK}}$) signals. These signals must be negated to indicate that the previous bus cycle has completed and the previous bus master has released the bus. When these conditions are met, the IDMA only asserts $\overline{\text{BGACK}}$ to indicate that it has taken control of the bus. When all operand transfers have occurred, the IDMA will release control of the bus by negating $\overline{\text{BGACK}}$.

Internally generated IDMA requests are affected by a mechanism supported to reduce the M68000 core interrupt latency and external bus master arbitration latency (see 3.8.5 Bus Arbitration Logic). The IDMA is forced to relinquish the bus when an external bus master requests the bus ($\overline{\text{BR}}$ is asserted) or when the M68000 core has an unmasked pending interrupt request. In these cases, the on-chip arbiter sends an internal bus-clear signal to the IDMA. In response, any operand transfer in progress will be fully completed (up to four bus cycles depending on the configuration), and bus ownership will be released.

When the IDMA regains the bus, it will continue transferring where it left off. If the core caused the bus to be relinquished, no further IDMA bus cycles will be started until IPA in the SCR is cleared. If the cause was an external request, no further IDMA bus cycles will be started while $\overline{\text{BR}}$ remains asserted. When $\overline{\text{BR}}$ is externally negated, if a transfer request is pending and IPA is cleared, the IDMA will arbitrate for the bus and continue normal operation.

3.1.7 Bus Exceptions

In any computer system, the possibility always exists that an error will occur during a bus cycle due to a hardware failure, random noise, or an improper access. When an asynchronous bus structure, such as that supported by the M68000 is used, it is easy to make provisions allowing a bus master to detect and respond to errors during a bus cycle. The IDMA recognizes the same bus exceptions as the M68000 core: reset, bus error, halt, and retry.

NOTE

These exceptions also apply to the SDMA channels except that the bus error reporting method is different. See 4.5.8.4 Bus Error on SDMA Access for further details.

3.1.7.1 Reset

Upon an external chip reset, the IDMA channel immediately aborts the channel operation, returns to the idle state, and clears CSR and CMR (including the STR bit). If a bus cycle is in progress when reset is detected, the cycle is terminated, the control and address/data pins are three-stated, and bus ownership is released. The IDMA can also be reset by RST in the CMR.

3.1.7.2 Bus Error

When a fatal error occurs during a bus cycle, a bus error exception is used to abort the cycle and systematically terminate that channel's operation. The IDMA terminates the current bus cycle, signals an error in the CSR, and generates a maskable interrupt. The IDMA clears STR and waits for a restart of the channel and the negation of $\overline{\text{BERR}}$ before starting any new bus cycles.

NOTE

Any data that was previously read from the source into the DHR will be lost.

3.1.7.3 Halt

IDMA transfer operation may be suspended at any time by asserting $\overline{\text{HALT}}$ to the IDMA. In response, any bus cycle in progress is completed (after $\overline{\text{DTACK}}$ is asserted), and bus ownership is released. No further bus cycles will be started while $\overline{\text{HALT}}$ remains asserted. When the IDMA is in the middle of an operand transfer when halted and $\overline{\text{HALT}}$ is subsequently negated, and if a new transfer request is pending, then IDMA will arbitrate for the bus and continue normal operation.

3.1.7.4 Relinquish and Retry

When $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ are asserted during a bus cycle, the IDMA terminates the bus cycle, releases the bus, and suspends any further operation until these signals are negated. When $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ are negated, the IDMA will arbitrate for the bus, re-execute the interrupted bus cycle, and continue normal operation.

3.2 INTERRUPT CONTROLLER

The IMP interrupt controller accepts and prioritizes both internal and external interrupt requests and generates a vector number during the CPU interrupt acknowledge cycle. Interrupt nesting is also provided so that an interrupt service routine of a lower priority interrupt may be suspended by a higher priority interrupt request. The interrupt controller block diagram is shown in Figure 3-2.

The on-chip interrupt controller has the following features:

- Two Operational Modes: Normal and Dedicated
- Eighteen Prioritized Interrupt Sources (Internal and External)
- A Fully Nested Interrupt Environment
- Unique Vector Number for Each Internal/External Source Generated
- Three Interrupt Request and Interrupt Acknowledge Pairs

- $\overline{\text{DTACK}}$ Generation When Vectors Supplied Internally

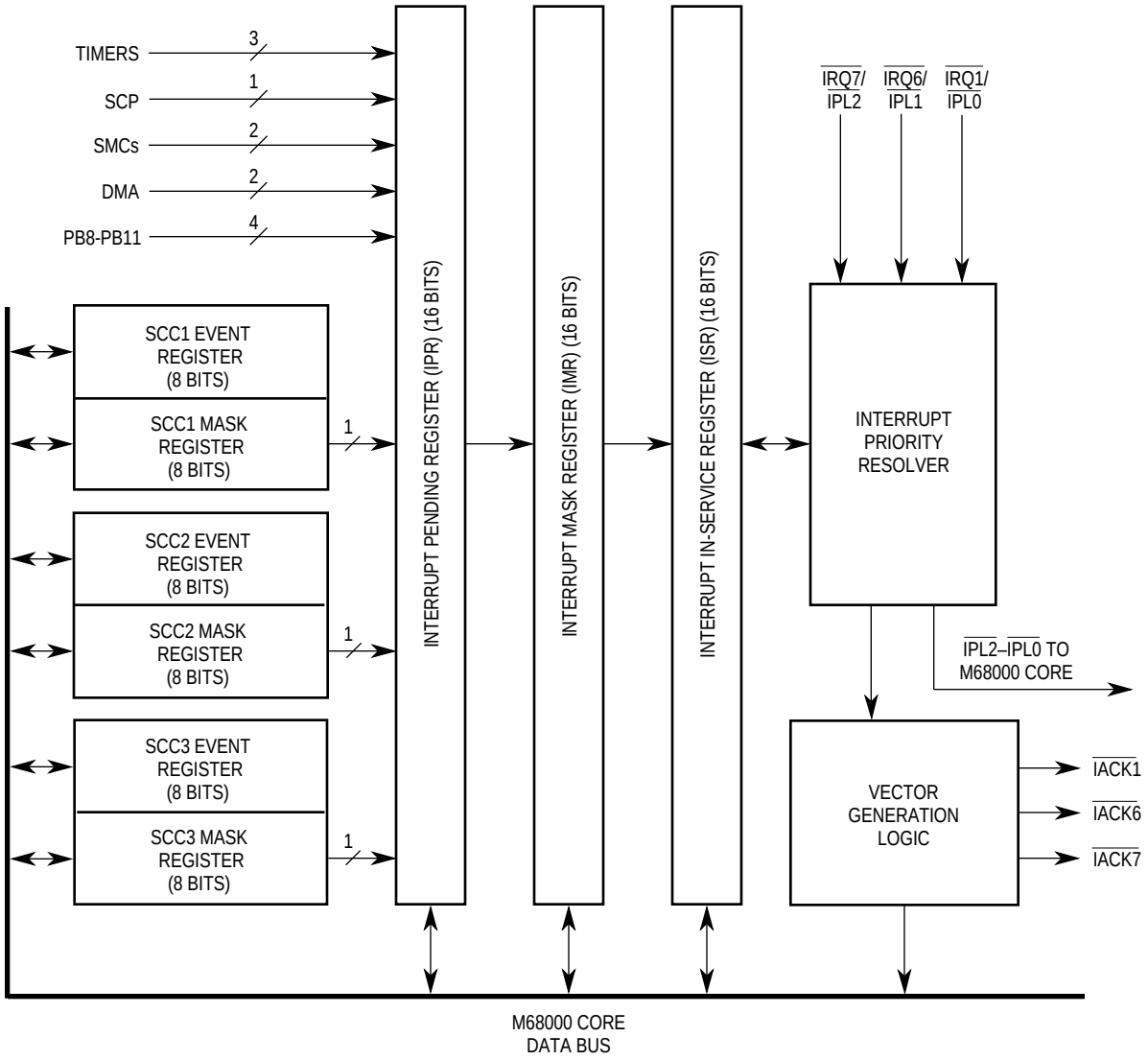


Figure 3-2. Interrupt Controller Block Diagram

3.2.1 Overview

An overview of IMP interrupt processing is presented in the following paragraphs.

3.2.1.1 IMP Interrupt Processing Overview

Interrupt processing on the IMP involves four steps. A typical sequence of these four steps is as follows:

1. The interrupt controller on the IMP collects interrupt events from on and off-chip peripherals, prioritizes them, and presents the highest priority request to the M68000 core.
2. The M68000 responds to the interrupt request by executing an interrupt acknowledge

bus cycle after the completion of the current instruction.

3. The interrupt controller recognizes the interrupt acknowledge cycle and places the interrupt vector for that interrupt request onto the M68000 bus.
4. The M68000 reads the vector, reads the address of the interrupt handler in the exception vector table, and then begins execution at that address.

Steps 2 and 4 are the responsibility of the M68000 core on the IMP; whereas, steps 1 and 3 are the responsibility of the interrupt controller on the IMP.

The M68000 core is not modified on the IMP; thus, steps 2 and 4 operate exactly as they would on the MC68000. In step 2, the M68000 status register (SR) is available to mask interrupts globally or to determine which priority levels can currently generate interrupts (see 2.5 Interrupt Processing for more details). Also in step 2, the interrupt acknowledge cycle is executed.

The interrupt acknowledge cycle carries out a standard M68000 bus read cycle, except that FC2–FC0 are encoded as 111, A3–A1 are encoded with the interrupt priority level (1–7, with 7 (i.e., 111) being the highest), and A19–A16 are driven high. $\overline{\text{UDS}}$ and $\overline{\text{LDS}}$ are both driven low.

In step 4, the M68000 reads the vector number, multiplies it by 4 to get the vector address, fetches a 4-byte program address from that vector address (seeTable 2-5), and then jumps to that 4-byte address. That 4-byte address is the location of the first instruction in the interrupt handler.

Steps 1 and 3 are the responsibility of the interrupt controller on the IMP. In steps 1 and 3, a number of configuration options are available. For instance, in step 1, there are two modes for handling external interrupts: normal and dedicated. In step 3, there are several different ways of generating vectors. These and other interrupt controller options are introduced in the following paragraphs.

3.2.1.2 Interrupt Controller Overview

The interrupt controller receives interrupts from internal sources such as the timers, the IDMA controller, the serial communication controllers, and the parallel I/O pins (port B pins 11–8). These interrupts are called internal requests (INRQ). The interrupt controller allows for masking each INRQ interrupt source. When multiple events within a peripheral can cause the INRQ interrupt, each event is also maskable in a register in that peripheral.

In addition to the INRQ interrupts, the interrupt controller can also receive external requests (EXRQ). EXRQ interrupts are input to the IMP according to normal or dedicated mode. In the normal mode, EXRQ interrupts are encoded on the $\overline{\text{IPL2}}$–$\overline{\text{IPL0}}$ lines. In the dedicated mode, EXRQ interrupts are presented directly as $\overline{\text{IRQ7}}$, $\overline{\text{IRQ6}}$, and $\overline{\text{IRQ1}}$.

Normal Mode

In this mode, the three external interrupt request pins are configured as $\overline{\text{IPL2}}$–$\overline{\text{IPL0}}$ as in the original MC68000. Up to seven levels of interrupt priority may be encoded. Level 4 is reserved for IMP INRQ interrupts and may not be generated by an external device.

Dedicated Mode

In this mode, the three interrupt request pins are configured as $\overline{IRQ7}$, $\overline{IRQ6}$, and $\overline{IRQ1}$ to provide dedicated request lines for three external sources at priority levels 1, 6, and 7. Each of these lines may be programmed to be edge-triggered or level-sensitive. In addition to level 4, which is reserved for INRQ interrupts, interrupt priority levels 2, 3, and 5 must not be assigned to external devices in this mode.

All INRQ and EXRQ sources are prioritized within the interrupt controller. The M68000 supports seven priority levels. Level 7, the highest priority level, is nonmaskable. EXRQ sources are given their own separate priority level. Priority level 4 is reserved exclusively for the INRQ sources with all the INRQ sources being further prioritized within this level. If more than one INRQ or EXRQ interrupt request is pending, the interrupt controller presents the highest priority interrupt to the M68000 core through an internal, hidden set of $\overline{IPL2}$–$\overline{IPL0}$ lines.

When the M68000 core executes the interrupt acknowledge cycle, a vector must be provided. If an INRQ source generated the interrupt, the interrupt controller always provides the vector. If an EXRQ source generated the interrupt, three options are available to generate the vector.

First, in most cases the interrupt controller can be configured to provide the vector to the M68000 core. This is usually the preferred solution.

Second, the external peripheral can generate the vector. To assist this process, the interrupt controller can provide up to three interrupt acknowledge outputs ($\overline{IACK7}$, $\overline{IACK6}$, and $\overline{IACK1}$).

Third, the external peripheral can assert the autovector ($\overline{AVEC}$) pin to cause the M68000 to use an autovector. The autovector method maps each interrupt level to a fixed vector location in the exception vector table, regardless of how many interrupt sources exist at that level.

To improve interrupt latency timing, a fast interrupt latency technique is supported in the IMP. On recognition of an interrupt, the IMP can assert the bus clear ($\overline{BCLR}$) signal externally, which can be used to force other bus masters off the bus. This involves the IPA and BCLM bits in the system control register (see 3.8 System Control).

3.2.2 Interrupt Priorities

INRQ and EXRQ interrupts are assigned to an interrupt priority level. INRQ interrupts are also assigned relative priorities within their given interrupt priority level. A fully nested interrupt environment is provided so that a higher priority interrupt is serviced before a lower priority interrupt.

3.2.2.1 INRQ and EXRQ Priority Levels

Seven levels of interrupt priority may be implemented in IMP system designs, with level 7 having the highest priority. INRQ interrupts are assigned to level 4 (fixed). EXRQ interrupts are assigned by the user to any of the remaining six priority levels in normal mode. In dedicated mode, EXRQ interrupts may be assigned to priority levels 7, 6, and 1.

Table 3-3 indicates the interrupt levels available in both normal and dedicated modes. This table also shows the $\overline{IPL2}$–$\overline{IPL0}$ encoding that should be provided by external logic for each EXRQ interrupt level in normal mode. For the dedicated mode, this table shows the IMP input pins ($\overline{IRQ7}$, $\overline{IRQ6}$, and $\overline{IRQ1}$) that should be asserted by an external device according to the desired interrupt priority level.

Table 3-3. EXRQ and INRQ Prioritization

Priority Level	Normal Mode $\overline{IPL2}$–$\overline{IPL0}$	Dedicated Mode $\overline{IRQ7}$, $\overline{IRQ6}$, $\overline{IRQ1}$	Interrupt Source
7 (Highest)	000	$\overline{IRQ7}$	EXRQ
6	001	$\overline{IRQ6}$	EXRQ
5	010	*	EXRQ
4	*	*	INRQ
3	100	*	EXRQ
2	101	*	EXRQ
1 (Lowest)	110	$\overline{IRQ1}$	EXRQ

* Priority level not available to an external device in this mode.

3.2.2.2 INRQ Interrupt Source Priorities

Although all INRQ interrupts are presented at level 4, the interrupt controller further organizes interrupt servicing of the 15 INRQ interrupts according to the priorities illustrated in Table 3-4. The interrupt from the port B pin 11 (PB11) has the highest priority, and the interrupt from the port B pin 8 (PB8) has the lowest priority. A single interrupt priority within level 4 is associated with each table entry. The IDMA entry is associated with the general-purpose DMA channel only, and not with the SDMA channels that service the SCCs. Those interrupts are reported through each individual SCC channel or, in the case of a bus error, through the SDMA channels bus error entry.

Table 3-4. INRQ Prioritization within Interrupt Level 4

Priority Level	Interrupt Source Description	Multiple Interrupt Events
Highest	General-Purpose Interrupt 3 (PB11)	No
	General-Purpose Interrupt 2 (PB10)	No
	SCC1	Yes
	SDMA Channels Bus Error	No
	IDMA Channel	Yes
	SCC2	Yes
	Timer 1	Yes
	SCC3	Yes
	General-Purpose Interrupt 1 (PB9)	No
	Timer 2	Yes
	SCP	No
	Timer 3	No
	SMC1	No
	SMC2	No
	General-Purpose Interrupt 0 (PB8)	No
Lowest	Error	—

3.2.2.3 Nested Interrupts

The following rules apply to nested interrupts:

1. The interrupt controller responds to all EXRQ and INRQ interrupts based upon their assigned priority level. The highest priority interrupt request is presented to the M68000 core for servicing. After the vector number corresponding to this interrupt is passed to the core during an interrupt acknowledge cycle, an INRQ interrupt request is cleared in IPR. (EXRQ requests must be cleared externally.) The remaining interrupt

requests, if any, are then assessed by priority so that another interrupt request may be presented to the core.

2. The 3-bit mask in the M68000 core status register (SR) ensures that a subsequent interrupt request at a higher interrupt priority level will suspend handling of a lower priority interrupt. The 3-bit mask indicates the current M68000 priority. Interrupts are inhibited for all priority levels less than or equal to the current M68000 priority. Priority level 7 cannot be inhibited by the mask; it is a nonmaskable interrupt level.
3. The interrupt controller allows a higher priority INRQ interrupt to be presented to the M68000 core before the servicing of a lower priority INRQ interrupt is completed. This is achieved using the interrupt in-service register (ISR). Each bit in the ISR corresponds to an INRQ interrupt source.
4. During an interrupt acknowledge cycle for an INRQ interrupt, the in–service bit is set by the interrupt controller for that interrupt source. When this bit is set, any subsequent INRQ interrupt requests at this priority level or lower are disabled until servicing of the current interrupt is completed and the in-service bit is cleared by the user. Pending interrupts for these sources are still set by the corresponding interrupt pending bit.
5. Thus, in the interrupt service routine for the INRQ interrupt, the user can lower the M68000 core mask to level 3 in the status register to allow higher priority level 4 (INRQ) interrupts to generate an interrupt request. This capability provides nesting of INRQ interrupt requests for sources within level 4. This capability is similar to the way the M68000 core interrupt mask provides nesting of interrupt requests for the seven interrupt priority levels.

3.2.3 Masking Interrupt Sources and Events

The user may mask EXRQ and INRQ interrupts to prevent an interrupt request to the M68000 core. EXRQ interrupt masking is handled external to the IMP—e.g., by programming a mask register within an external device. INRQ interrupt masking is accomplished by programming the IMR. Each bit in the IMR corresponds to one of 15 INRQ interrupt sources.

When a masked INRQ interrupt source has a pending interrupt request, the corresponding bit is set in the IPR, even though the interrupt is not generated to the core. By masking all interrupt sources using the IMR, the user may implement a polling interrupt servicing scheme for INRQ interrupts, as discussed in 3.2.5.2 Interrupt Pending Register (IPR).

When an INRQ interrupt source from an on-chip peripheral has multiple interrupt events, the user can individually mask these events by programming that peripheral's mask register (see Figure 3-3). Table 3-4 indicates the interrupt sources that have multiple interrupt events. In this case, when a masked event occurs, an interrupt request is not generated for the associated interrupt source, and the corresponding bit in the IPR is not set. If the corresponding bit in the IPR is already set, then masking the event in the peripheral mask register causes the IPR bit to be cleared. To determine the cause of a pending interrupt when an interrupt source has multiple interrupt events, the user interrupt service routine must read the event register within that on-chip peripheral. By clearing all unmasked bits in the event register, the IPR bit is also cleared.

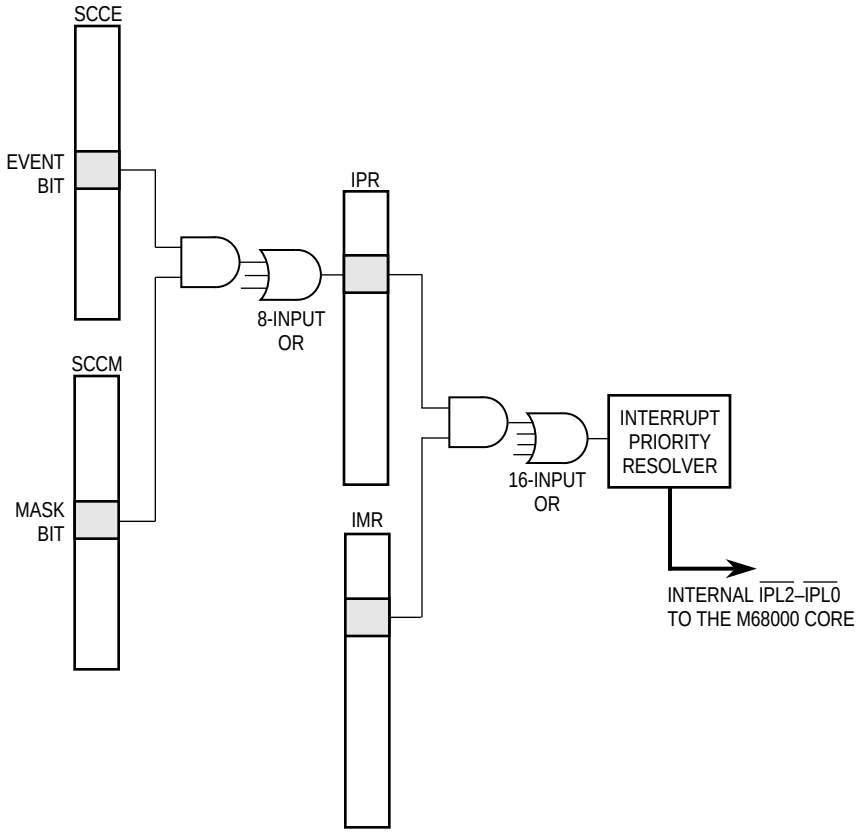


Figure 3-3. Interrupt Request Logic Diagram for SCCs

3.2.4 Interrupt Vector

Pending EXRQ interrupts and unmasked INRQ interrupts are presented to the M68000 core in order of priority. The M68000 core responds to an interrupt request by initiating an interrupt acknowledge cycle to receive a vector number, which allows the core to locate the interrupt's service routine.

If an INRQ source generated the interrupt, the interrupt controller always provides the vector corresponding to the highest priority, unmasked, pending interrupt. If an EXRQ source generated the interrupt, three options are available to generate the vector.

Option 1. By programming the GIMR, the user can enable the interrupt controller to provide the vector for any combination of EXRQ interrupt levels 1, 6, and 7. This is available regardless of whether normal or dedicated mode is selected. Whenever a vector is provided by the interrupt controller, $\overline{\text{DTACK}}$ is also provided by the interrupt controller during that interrupt acknowledge cycle. $\overline{\text{DTACK}}$ is an output from the IMP in this case.

The IMP can generate vectors for up to seven external peripherals by connecting the external request lines to $\overline{\text{IRQ7}}$, $\overline{\text{IRQ6}}$, $\overline{\text{IRQ1}}$, PB11, PB10, PB9, and PB8. PB11, PB10, PB9, and PB8 are prioritized within level 4.

Option 2. The external peripheral can generate the vector. In this case the external device must decode the interrupt acknowledge cycle, put out the 8-bit vector, and generate $\overline{\text{DTACK}}$. The decoding of the interrupt acknowledge cycle can be provided by the $\overline{\text{IACK7}}$, $\overline{\text{IACK6}}$, and $\overline{\text{IACK1}}$ signals (enabled in the PBCNT register) if either normal or dedicated mode is chosen. These signals eliminate the need for external logic to perform the decoding of the A19–A16, A3–A1, and FC2–FC0 pins externally to detect the interrupt acknowledge cycle. If the $\overline{\text{IACK}}$ signals are not needed, they can be regained as general purpose parallel I/O pins. The external device must generate $\overline{\text{DTACK}}$ in this mode, and $\overline{\text{DTACK}}$ is an input to the IMP.

Option 3. The external peripheral can assert the $\overline{\text{AVEC}}$ pin to cause the M68000 to use an autovector. In this case, $\overline{\text{DTACK}}$ should not be asserted by the external device. $\overline{\text{AVEC}}$ is recognized by the M68000 core on the falling edge of S4 and should meet the asynchronous setup time to the falling edge of S4. The $\overline{\text{IACK}}$ signals can be used to help generate the $\overline{\text{AVEC}}$ signal for priority levels 1, 6, and 7, if needed.

NOTE

If $\overline{\text{AVEC}}$ is asserted during an interrupt acknowledge cycle, an autovector is taken, regardless of the vector on the bus. $\overline{\text{AVEC}}$ should not be asserted during level 4 interrupt acknowledge cycles.

When the IMP generates the vector, the following procedure is used. The three most significant bits of the interrupt vector number are programmed by the user in the GIMR. These three bits are concatenated with five bits generated by the interrupt controller to provide an 8-bit vector number to the core. The interrupt controller's encoding of the five low-order bits of the interrupt vector is shown in Table 3-5. An example vector calculation is shown in Figure 3-4. When the core initiates an interrupt acknowledge cycle for level 4 and there is no internal interrupt pending, the interrupt controller encodes the error code 00000 onto the five low-order bits of the interrupt vector.

Table 3-5. Encoding the Interrupt Vector

Priority Level	5-Bit Vector	Interrupt Source
7 (Highest)	10111	External Device
6	10110	External Device
5	None	External Device
4	01111	General-Purpose Interrupt 3 (PB11)
4	01110	General-Purpose Interrupt 2 (PB10)
4	01101	SCC1
4	01100	SDMA Channels Bus Error
4	01011	IDMA Channel
4	01010	SCC2
4	01001	Timer 1
4	01000	SCC3
4	00111	General-Purpose Interrupt 1 (PB9)
4	00110	Timer 2
4	00101	SCP
4	00100	Timer 3
4	00011	SMC1
4	00010	SMC2
4	00001	General-Purpose Interrupt 0 (PB8)
4	00000	Error
3	None	External Device
2	None	External Device
1 (Lowest)	10001	External Device

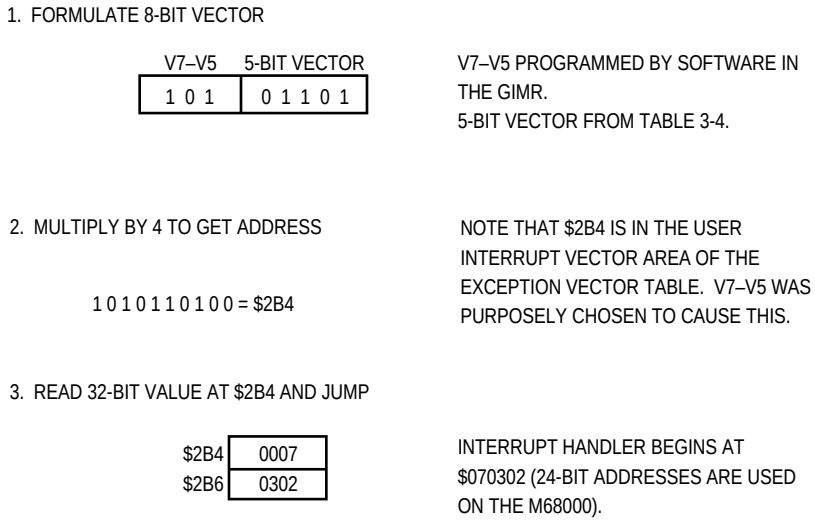


Figure 3-4. SCC1 Vector Calculation Example

3.2.5 Interrupt Controller Programming Model

The user communicates with the interrupt controller using four registers. The global interrupt mode register (GIMR) defines the interrupt controller's operational mode. The interrupt pending register (IPR) indicates which INRQ interrupt sources require interrupt service. The interrupt mask register (IMR) allows the user to prevent any of the INRQ interrupt sources from generating an interrupt request. The interrupt in-service register (ISR) provides a capability for nesting INRQ interrupt requests.

3.2.5.1 Global Interrupt Mode Register (GIMR)

The user normally writes the GIMR soon after a total system reset. The GIMR is initially $0000 and is reset only upon a total system reset. If bits V7–V5 of the GIMR are not written to specify an interrupt vector prior to the first interrupt condition, the interrupt controller will pass the vector $0F (the uninitialized interrupt vector), regardless of the interrupt source.

15	14	13	12	11	10	9	8	7 5	4 0
MOD	IV7	IV6	IV1	—	ET7	ET6	ET1	V7–V5	RESERVED

MOD—Mode

0 = Normal operational mode. Interrupt request lines are configured as $\overline{IPL2}$–$\overline{IPL0}$.
1 = Dedicated operational mode. Interrupt request lines are configured as $\overline{IRQ7}$, $\overline{IRQ6}$, and $\overline{IRQ1}$.

IV7—Level 7 Interrupt Vector

This bit is valid in both normal and dedicated modes.

0 = Internal vector. The interrupt controller will provide the vector number for a level 7 interrupt during the interrupt acknowledge cycle.
1 = External vector. The interrupt controller will not provide the vector number for a level 7 interrupt.

IV6—Level 6 Interrupt Vector

This bit is valid in both normal and dedicated modes.

0 = Internal vector. The interrupt controller will provide the vector number for a level 6 interrupt during the interrupt acknowledge cycle.
1 = External vector. The interrupt controller will not provide the vector number for a level 6 interrupt.

IV1—Level 1 Interrupt Vector

This bit is valid in both normal and dedicated modes.

0 = Internal vector. The interrupt controller will provide the vector number for a level 1 interrupt acknowledge cycle.
1 = External vector. The interrupt controller will not provide the vector number for a level 1 interrupt.

ET7—$\overline{\text{IRQ7}}$ Edge-/Level-Triggered

This bit is valid only in the dedicated mode.

0 = Level-triggered. An interrupt is made pending when $\overline{\text{IRQ7}}$ is low.

NOTE

The M68000 always treats level 7 as an edge-sensitive interrupt. Normally, users should not select the level-triggered option. The level-triggered option is useful when it is desired to make the negation of $\overline{\text{IRQ7}}$ cause the IOUT2–IOUT0 pins to cease driving a level 7 interrupt request when the MC68302 is used in the disable CPU mode. This situation is as follows:

For a slave-mode MC68302, when it is triggered by $\overline{\text{IRQ1}}$, $\overline{\text{IRQ6}}$, or $\overline{\text{IRQ7}}$ to generate an interrupt, its interrupt controller will output the interrupt request on pins IOUT2–IOUT0 to another processor (MC68302, MC68020, etc.) For cases when the slave MC68302 does not generate a level 4 vector (i.e., the VGE bit is cleared), one must set the ET1, ET6, and ET7 bits to level-triggered and then negate the $\overline{\text{IRQ1}}$, $\overline{\text{IRQ6}}$, and $\overline{\text{IRQ7}}$ lines externally in the interrupt handler code. If the ET1, ET6, and ET7 bits are set to edge-triggered and the VGE bit is clear, the IOUT2–IOUT0 pins will never be cleared.

1 = Edge-triggered. An interrupt is made pending when $\overline{\text{IRQ7}}$ changes from one to zero (falling edge).

ET6—IRQ6 Edge-/Level-Triggered

This bit is valid only in the dedicated mode.

0 = Level-triggered. An interrupt is made pending when $\overline{\text{IRQ6}}$ is low.

NOTE

While in disable CPU mode during the host processor interrupt acknowledge cycle for $\overline{\text{IRQ6}}$, if $\overline{\text{IRQ6}}$ is not continuously asserted, the interrupt controller will still provide the vector number (and $\overline{\text{DTACK}}$) according to the IV6 bit. The $\overline{\text{IACK6}}$ falling edge may be used externally to negate $\overline{\text{IRQ6}}$.

1 = Edge-triggered. An interrupt is made pending when $\overline{\text{IRQ6}}$ changes from one to zero (falling edge).

ET1—$\overline{\text{IRQ1}}$ Edge-/Level-Triggered

This bit is valid only in the dedicated mode.

0 = Level-triggered. An interrupt is made pending when $\overline{\text{IRQ1}}$ is low.

NOTE

While in disable CPU mode, during the host processor interrupt acknowledge cycle for $\overline{IRQ1}$, if $\overline{IRQ1}$ is not continuously asserted, the interrupt controller will still provide the vector number (and $\overline{DTACK}$) according to the IV1 bit. The $\overline{IACK6}$ falling edge can be used externally to negate $\overline{IRQ1}$.

1 = Edge-triggered. An interrupt is made pending when $\overline{IRQ1}$ changes from one to zero (falling edge).

V7–V5—Interrupt Vector Bits 7–5

These three bits are concatenated with five bits provided by the interrupt controller, which indicate the specific interrupt source, to form an 8-bit interrupt vector number. If these bits are not written, the vector $0F is provided.

Note:

These three bits should be greater than or equal to ‘010’ in order to put the interrupt vector in the area of the exception vector table for user vectors.

Bits 11 and 4–0—Reserved for future use.

3.2.5.2 Interrupt Pending Register (IPR)

Each bit in the 16-bit IPR corresponds to an INRQ interrupt source. When an INRQ interrupt is received, the interrupt controller sets the corresponding bit in the IPR.

In a vectored interrupt environment, the interrupt controller clears the IPR bit when the vector number corresponding to the INRQ interrupt source is passed to the M68000 core during an interrupt acknowledge cycle, unless an event register exists for that INRQ interrupt. In a polled interrupt scheme, the user must periodically read the IPR. When a pending interrupt is handled, the user should clear the corresponding bit in the IPR by writing a one to that bit. (If an event register exists, the unmasked event register bits should be cleared instead, causing the IPR bit to be cleared.) Since the user can only clear bits in this register, the bits that are written as zeros will not be affected. The IPR is cleared at reset.

NOTE

The ERR bit is set if the user drives the $\overline{IPL2}$–$\overline{IPL0}$ lines to interrupt level 4 and no INRQ interrupt is pending.

15	14	13	12	11	10	9	8
PB11	PB10	SCC1	SDMA	IDMA	SCC2	TIMER1	SCC3

7	6	5	4	3	2	1	0
PB9	TIMER2	SCP	TIMER3	SMC1	SMC2	PB8	ERR

3.2.5.3 Interrupt Mask Register (IMR)

Each bit in the 16-bit IMR corresponds to an INRQ interrupt source. The user masks an interrupt source by clearing the corresponding bit in the IMR. When a masked INRQ interrupt occurs, the corresponding bit in the IPR is set, but the IMR bit prevents the interrupt request from reaching the M68000 core. If an INRQ source is requesting interrupt service when the user clears the IMR bit, the request to the core will cease, but the IPR bit remains set. If the IMR bit is then set later by the user, the pending interrupt request will once again request interrupt service and will be processed by the core according to its assigned priority. The IMR, which can be read by the user at any time, is cleared by reset.

It is not possible to mask the ERR INRQ source in the IMR. Bit 0 of the IMR is undefined.

NOTE

If a bit in the IMR is masked at the same time that the interrupt at level 4 is causing the M68000 core to begin the interrupt acknowledge cycle, then the interrupt is not processed, and one of two possible cases will occur. First, if other unmasked interrupts are pending at level 4, then the interrupt controller will acknowledge the interrupt with a vector from the next highest priority unmasked interrupt source. Second, if no other interrupts are pending at level 4, then the interrupt controller will acknowledge the interrupt with the error vector (00000 binary).

To avoid handling the error vector, the user can raise the interrupt mask in the M68000 core status register (SR) to 4 before masking the interrupt source and then lower the level back to its original value. Also, if the interrupt source has multiple events (e.g., SCC1), then the interrupts for that peripheral can be masked within the peripheral mask register.

NOTE

To clear bits that were set by multiple interrupt events, the user should clear all the unmasked events in the corresponding on-chip peripheral's event register.

15	14	13	12	11	10	9	8
PB11	PB10	SCC1	SDMA	IDMA	SCC2	TIMER1	SCC3

7	6	5	4	3	2	1	0
PB9	TIMER2	SCP	TIMER3	SMC1	SMC2	PB8	—

3.2.5.4 Interrupt In-Service Register (ISR).

Each bit in the 16-bit ISR corresponds to an INRQ interrupt source. In a vectored interrupt environment, the interrupt controller sets the ISR bit when the vector number corresponding to the INRQ interrupt source is passed to the core during an interrupt acknowledge cycle. The user's interrupt service routine should clear this bit during the servicing of the interrupt. (If an event register exists for this peripheral, its bits should also be cleared by the user program.) To clear a bit in the ISR, the user writes a one to that bit. The user can only clear bits in this register, and bits that are written with zeros will not be affected. The ISR is cleared at reset.

This register may be read by the user to determine which INRQ interrupts are currently being processed. More than one bit in the ISR may be a one if the capability is used to allow higher priority level 4 interrupts to interrupt lower priority level 4 interrupts. See 3.2.2.3 Nested Interrupts for more details.

The user can control the extent to which level 4 interrupts may interrupt other level 4 interrupts by selectively clearing the ISR. A new INRQ interrupt will be processed if it has a higher priority than the highest priority INRQ interrupt having its ISR bit set. Thus, if an INRQ interrupt routine lowers the 3-bit mask in the M68000 core to level 3 and also clears its ISR bit at the beginning of the interrupt routine, then a lower priority INRQ interrupt can interrupt it as long as the lower priority is higher than any other ISR bits that are set.

If the INRQ error vector is taken, no bit in the ISR is set. Bit 0 of the ISR is always zero.

15	14	13	12	11	10	9	8
PB11	PB10	SCC1	SDMA	IDMA	SCC2	TIMER1	SCC3

7	6	5	4	3	2	1	0
PB9	TIMER2	SCP	TIMER3	SMC1	SMC2	PB8	0

3.2.6 Interrupt Handler Examples

The following examples illustrate proper interrupt handling on the IMP. Nesting of level 4 interrupts (a technique described earlier) is not implemented in the following examples.

Example 1—Timer 3 (Software Watchdog Timer) Interrupt Handler

1. Vector to interrupt handler.
2. (Handle Event)
3. Clear the TIMER3 bit in the ISR.
4. Execute RTE instruction.

Example 2— SCC1 Interrupt Handler

1. Vector to interrupt handler.

2. Immediately read the SCC1 event (SCCE1) register into a temporary location.
3. Decide which events in the SCCE1 will be handled in this handler and clear those bits in the SCCE1 as soon as possible.

(Handle events in the SCC1 Rx or Tx BD tables.)

At the end:

4. Clear the SCC1 bit in the ISR.
5. Execute RTE instruction. If any unmasked bits in SCCE1 remain at this time (either uncleared by the software or set by the IMP during the execution of this handler), this interrupt source will be made pending again immediately following the RTE instruction.

In example 1, the hardware clears the TIMER3 bit in the IPR during the interrupt acknowledge cycle. This is an example of a handler for an interrupt source without multiple events. In example 2, the IPR bit remains set as long as one or more unmasked event bits remain the in the SCCE1 register. This is an example of a handler for an interrupt source with multiple events.

Note that, in both cases, it is not necessary to clear the IPR bit; however, in both cases, it is necessary to clear the ISR bit to allow future interrupts from this source.

3.3 PARALLEL I/O PORTS

The IMP supports two general-purpose I/O ports, port A and port B, whose pins can be general-purpose I/O pins or dedicated peripheral interface pins. Some port B pins are always maintained as four general-purpose I/O pins, each with interrupt capability.

3.3.1 Port A

Each of the 16 port A pins are independently configured as a general-purpose I/O pin if the corresponding port A control register (PACNT) bit is cleared. Port A pins are configured as dedicated on-chip peripheral pins if the corresponding PACNT bit is set. An example block diagram of PA0 is given in Figure 3-5

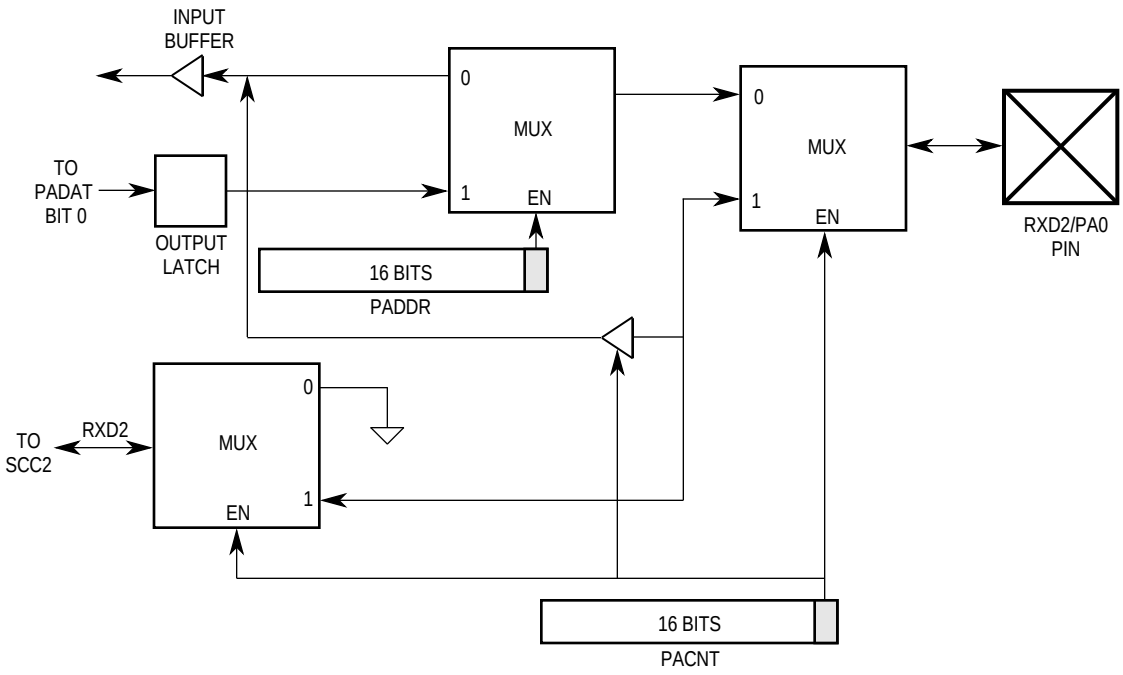


Figure 3-5. Parallel I/O Block Diagram for PA0

When acting as a general-purpose I/O pin, the signal direction for that pin is determined by the corresponding control bit in the port A data direction register (PADDR). The port I/O pin is configured as an input if the corresponding PADDR bit is cleared; it is configured as an output if the corresponding PADDR bit is set. All PACNT bits and PADDR bits are cleared on total system reset, configuring all port A pins as general-purpose input pins. (Note that these port pins do not have internal pullup resistors).

If a port A pin is selected as a general-purpose I/O pin, it may be accessed through the port A data register (PADAT). Data written to the PADAT is stored in an output latch. If a port A pin is configured as an output, the output latch data is gated onto the port pin. In this case, when the PADAT is read, the contents of the output latch associated with the output port pin are read. If a port A pin is configured as an input, data written to PADAT is still stored in the output latch but is prevented from reaching the port pin. In this case, when PADAT is read, the state of the port pin is read.

If a port A pin is selected as a dedicated on-chip peripheral pin, the corresponding bit in the PADDR is ignored, and the direction of the pin is determined by the operating mode of the on-chip peripheral. In this case, the PADAT contains the current state of the peripheral's input pin or output driver.

Certain pins may be selected as general-purpose I/O pins, even when other pins related to the same on-chip peripheral are used as dedicated pins. For example, a system that configures SCC2 to operate in a nonmultiplexed mode without the modem control lines and external clocks (RCLK2, TCLK2, $\overline{\text{CD2}}$, $\overline{\text{CTS2}}$, and $\overline{\text{RTS2}}$) may dedicate the data lines (RXD2 and TXD2) to SCC2 and configure the others as general-purpose I/O pins. What the peripheral

now receives as its input, given that some of its pins have been reassigned, is shown in Table 3-6. If an input pin to a channel (for example $\overline{CD2}$ or $\overline{CTS2}$) is used as a general-purpose I/O pin, then the input to the peripheral is automatically connected internally to V_{DD} or GND, based on the pin's function. This does not affect the operation of the port pins in their general-purpose I/O function.

NOTE

If the $\overline{DREQ}$/PA13 pin is selected to be PA13, then $\overline{DREQ}$ is tied low. If the IDMA is programmed for external requests, then it always recognizes an external request, and the entire block will be transferred in one burst.

Table 3-6. Port A Pin Functions

PACNT Bit = 1 Pin Function	PACNT Bit = 0 Pin Function	Input to SCC2/SCC3/IDMA
RXD2	PAO	GND
TXD2	PA1	—
RCLK2	PA2	GND
TCLK2	PA3	RCLK2 #
$\overline{CTS2}$	PA4	GND
$\overline{RTS2}$	PA5	—
$\overline{CD2}$	PA6	GND
SDS2/BRG2	PA7	—
RXD3	PA8	GND
TXD3	PA9	—
RCLK3	PA10	GND
TCLK3	PA11	RCLK3 #
BRG3	PA12	—
$\overline{DREQ}$	PA13	GND
$\overline{DACK}$	PA14	—
$\overline{DONE}$	PA15	V_{DD}

Allows a single external clock source on the RCLK pin to clock both the SCC receiver and transmitter.

3.3.2 Port B

Port B has 12 pins. PB7–PB0 may be configured as general-purpose I/O pins or as dedicated peripheral interface pins; whereas, PB11–PB8 are always maintained as four general-purpose pins, each with interrupt capability.

3.3.2.1 PB7–PB0

Each port B pin may be configured as a general-purpose I/O pin or as a dedicated peripheral interface pin. PB7–PB0 functions exactly like PA15–PA0, except that PB7–PB0 is controlled by the port B control register (PBCNT), the port B data direction register (PBDDR), and the port B data register (PBDAT), and PB7 is configured as an open-drain output ($\overline{WDOG}$) upon total system reset.

Table 3-7 shows the dedicated function of each pin. The third column shows the input to the peripheral when the pin is used as a general-purpose I/O pin.

Table 3-7. Port B Pin Functions

PBCNT Bit = 1 Pin Function	PBCNT Bit = 0 Pin Function	Input to Interrupt Control and Timers
IACK7	PB0	—
IACK6	PB1	—
IACK1	PB2	—
TIN1	PB3	GND
TOUT1	PB4	—
TIN2	PB5	GND
TOUT2	PB6	—
WDOG	PB7	—

3.3.2.2 PB11–PB8

PB11–PB8 are four general-purpose I/O pins continuously available as general-purpose I/O pins and, therefore, are not referenced in the PBCNT. PB8 operates like PB11–PB9 except that it can also be used as the DRAM refresh controller request pin, as selected in the system control register (SCR).

The direction of each pin is determined by the corresponding bit in the PBDDR. The port pin is configured as an input if the corresponding PBDDR bit is cleared; it is configured as an output if the corresponding PBDDR bit is set. PBDDR11–PBDDR8 are cleared on total system reset, configuring all PB11–PB8 pins as general-purpose input pins. (Note that the port pins do not have internal pullup resistors). The GIMR is also cleared on total system reset so that if any PB11–PB8 pin is left floating it will not cause a spurious interrupt.

The PB11–PB8 pins are accessed through the PBDAT. Data written to PBDAT11–PBDAT8 is stored in an output latch. If the port pin is configured as an output, the output latch data is gated onto the port pin. In this case, when PBDAT11–PBDAT8 is read, the contents of the output latch associated with the output port pin are read. If a port B pin is configured as an input, data written to PBDAT is still stored in the output latch but is prevented from reaching the port pin. In this case, when PBDAT is read, the state of the port pin is read.

When a PB11–PB8 pin is configured as an input, a high-to-low change will cause an interrupt request signal to be sent to the IMP interrupt controller. Each of the four interrupt requests is associated with a fixed internal interrupt priority level within level 4. (The priority at which each bit requests an interrupt is detailed in Table 3-4.) Each request can be masked independently in the IMP interrupt controller by clearing the appropriate bit in the IMR (PB11–PB8). The input signals to PB11–PB8 must meet specifications 190 and 191 shown in Table 6.16 of the AC Electrical Specifications.

3.3.3 I/O Port Registers

The I/O port consists of three memory-mapped read-write 16-bit registers for port A and three memory-mapped read-write 16-bit registers for port B. Refer to Figure 3-6 for the I/O port registers. The reserved bits are read as zeros.

Port A Control Register(PACNT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA	CA

0 = I/O 1 = Peripheral

Port A Data Direction Register(PADDR)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA	DA

0 = Input 1 = Output

Port A Data Register(PADAT)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA	PA

Port B Control Register(PBCNT)

15	8	7	6	5	4	3	2	1	0
RESERVED		CB	CB	CB	CB	CB	CB	CB	CB

0 = I/O 1 = Peripheral

Port B Data Direction Register(PBDDR)

15	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB

0 = Input 1 = Output

Port B Data Register(PBDAT)

15	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PB	PB	PB	PB	PB	PB	PB	PB	PB	PB	PB	PB

Figure 3-6. Parallel I/O Port Registers

3.4 DUAL-PORT RAM

The CP has 1152 bytes of static RAM configured as a dual-port memory. The dual-port RAM can be accessed by the CP main controller or by one of three bus masters: the M68000 core, the IDMA, or an external master. The M68000 core and the IDMA access the RAM synchro-

nously with no wait states. The external master requests the M68000 bus using the $\overline{BR}$ pin and is granted bus ownership. The external master must then access the RAM synchronously with respect to the IMP system clock with zero or one wait state, or asynchronously as determined by the EMWS and SAM bits in the system control register. Except for several locations initialized by the CP, the dual-port RAM is undefined at power-on reset but is not modified by successive resets. The RAM is divided into two parts: parameter RAM and system RAM.

The 576-byte parameter RAM area includes pointers, counters, and registers used with the serial ports. This area is accessed by the CP during communications processing. Any individual locations not required in a given application may be used as general-purpose RAM.

The 576-byte system RAM is a general-purpose RAM, which may be used as M68000 data and/or program RAM or CP microcode RAM. As data RAM, it can include serial port data buffers or can be used for other purposes such as a no-wait-state cache for the M68000 core. As CP microcode RAM, it is used exclusively to store microcode for the CP main controller, allowing the development of special protocols or protocol enhancements, under special arrangement with Motorola. Appendix C discusses available offerings.

The RAM block diagram is shown in Figure 3-7. The M68000 core, the IDMA, and the external master access the RAM through the IMP bus interface unit (BIU) using the M68000 bus. When an access is made, the BIU generates a wait signal to the CP main controller to prevent simultaneous access of the RAM. The CP main controller waits for one cycle to allow the RAM to service the M68000 bus cycle and then regenerates its RAM cycle. This mechanism allows the RAM to be accessed synchronously by the M68000 core, IDMA, or external master without wait states. Thus, during the four-clock M68000 memory cycle, three internal accesses by the CP main controller may occur. The BIU also provides the $\overline{DTACK}$ signal output when the RAM and on-chip registers are accessed by any M68000 bus master.

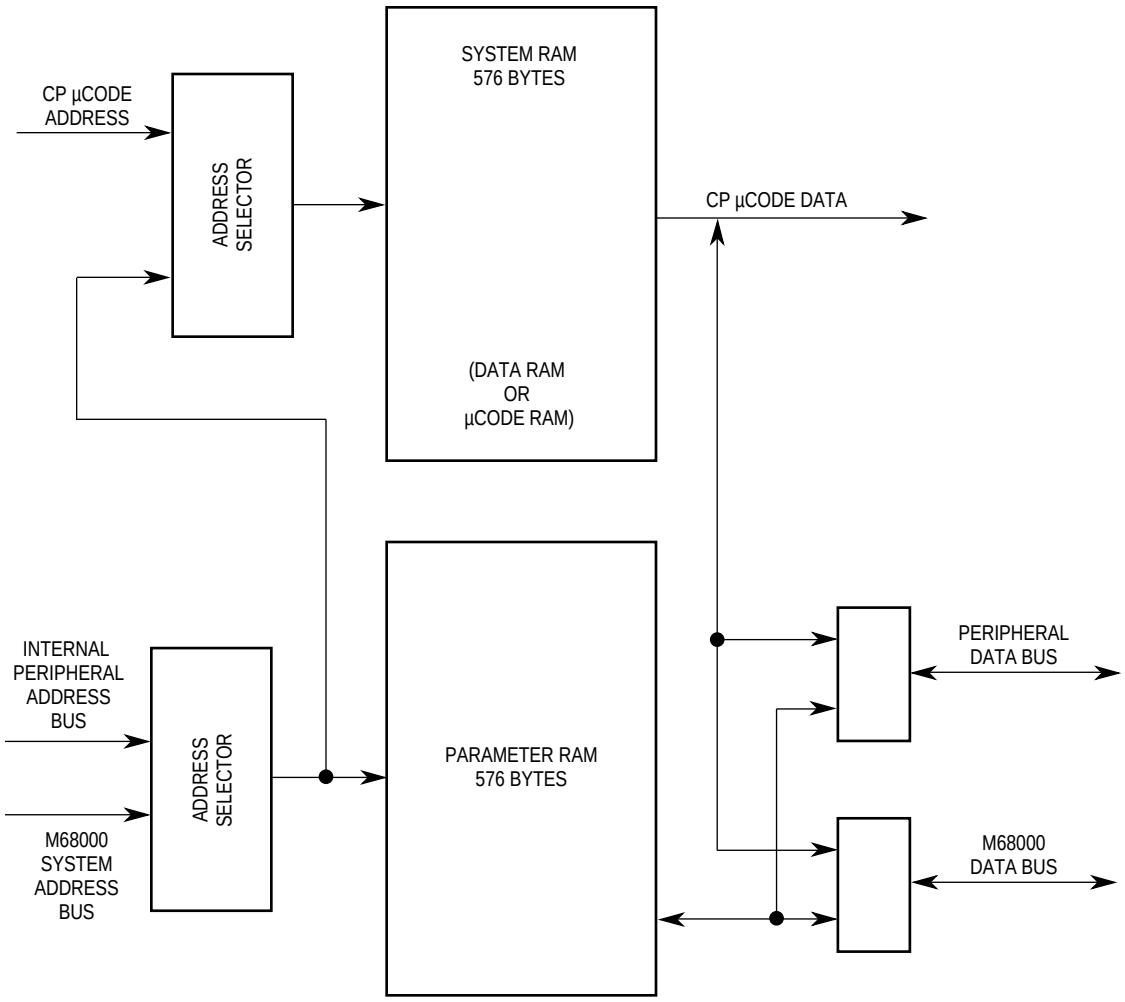


Figure 3-7. RAM Block Diagram

3.5 TIMERS

The MC68302 includes three timer units: two identical general-purpose timers and a software watchdog timer.

Each general-purpose timer consists of a timer mode register (TMR), a timer capture register (TCR), a timer counter (TCN), a timer reference register (TRR), and a timer event register (TER). The TMR contains the prescaler value programmed by the user. The software watchdog timer, which has a watchdog reference register (WRR) and a watchdog counter (WCN), uses a fixed prescaler value. The timer block diagram is shown in Figure 3-8.

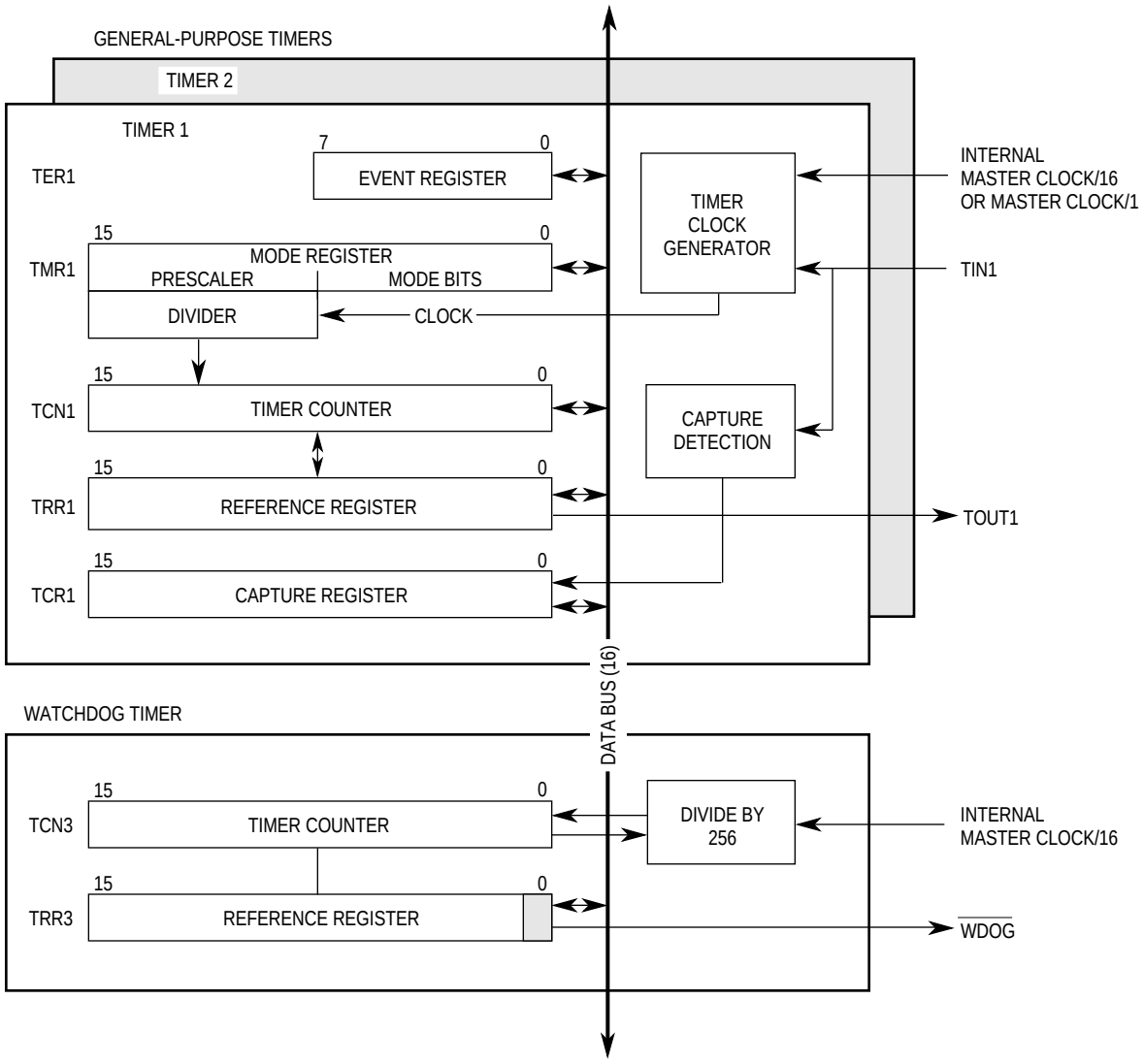


Figure 3-8. Timer Block Diagram

3.5.1 Timer Key Features

The two identical general-purpose timer units have the following features:

- Maximum Period of 16 Seconds (at 16.67 MHz)
- 60-ns Resolution (at 16.67 MHz)
- Programmable Sources for the Clock Input
- Input Capture Capability
- Output Compare with Programmable Mode for the Output Pin
- Two Timers Cascadable to Form a 32-Bit Timer
- Free Run and Restart Modes

The watchdog timer has the following features:

- A 16-Bit Counter and Reference Register
- Maximum Period of 16.78 Seconds (at 16 MHz)
- 0.5 ms Resolution (at 16 MHz)
- Output Signal (WDOG)
- Interrupt Capability

3.5.2 General Purpose Timer Units

The clock input to the prescaler may be selected from the main clock (divided by 1 or by 16) or from the corresponding timer input (TIN) pin. TIN is internally synchronized to the internal clock. The clock input source is selected by the ICLK bits of the corresponding TMR. The prescaler is programmed to divide the clock input by values from 1 to 256. The output of the prescaler is used as an input to the 16-bit counter.

The resolution of the timer is one clock cycle (60 ns at 16.67 MHz). The maximum period (when the reference value is all ones) is 268,435,456 cycles (16.78 seconds at 16.00 MHz).

Each timer may be configured to count until a reference is reached and then either resets to zero on the next clock or continues to run. The free run/restart (FRR) bit of the corresponding TMR selects each mode. Upon reaching the reference value, the corresponding TER bit is set, and an interrupt is issued if the output reference interrupt enable (ORI) bit in TMR is set.

Each timer may output a signal on the timer output ($\overline{\text{TOUT1}}$ or $\overline{\text{TOUT2}}$) pin when the reference value is reached, as selected by the output mode (OM) bit of the corresponding TMR. This signal can be an active-low pulse for one clock cycle or a toggle of the current output. The output can also be used as an input to the other timer, resulting in a 32-bit timer.

Each timer has a 16-bit TCR, which is used to latch the value of the counter when a defined transition (of TIN1 or TIN2) is sensed by the corresponding input capture edge detector. The type of transition triggering the capture is selected by the capture edge and enable interrupt (CE) bits in the corresponding TMR. Upon a capture or reference event, the corresponding TER bit is set, and a maskable interrupt is issued.

The timer registers may be modified at any time by the user.

3.5.2.1 Timer Mode Register (TMR1, TMR2)

TMR1 and TMR2 are identical 16-bit registers. TMR1 and TMR2, which are memory-mapped read-write registers to the user, are cleared by reset.

15 – 8	7 – 6	5	4	3	2 – 1	0
PRESCALER VALUE (PS)	CE	OM	ORI	FRR	ICLK	RST

RST—Reset Timer

This bit performs a software reset of the timer identical to that of an external reset.

0 = Reset timer (software reset), includes clearing the TMR, TRR, and TCN.
1 = Enable timer

ICLK—Input Clock Source for the Timer

00 = Stop count
01 = Master clock
10 = Master clock divided by 16. Note that this clock source is not synchronized to the timer; thus, successive timeouts may vary slightly in length.
11 = Corresponding TIN pin, TIN1 or TIN2 (falling edge)

FRR—Free Run/Restart

0 = Free run—timer count continues to increment after the reference value is reached.
1 = Restart—timer count is reset immediately after the reference value is reached.

ORI—Output Reference Interrupt Enable

0 = Disable interrupt for reference reached (does not affect interrupt on capture function)
1 = Enable interrupt upon reaching the reference value

OM—Output Mode

0 = Active-low pulse for one CLKO clock cycle (60 ns at 16.67 MHz)
1 = Toggle output

NOTE

After reset, the $\overline{\text{TOUT}}$ signal begins in a high state, but is not available externally until the PBCNT register is configured for this function.

CE—Capture Edge and Enable Interrupt

00 = Capture function is disabled
01 = Capture on rising edge only and enable interrupt on capture event
10 = Capture on falling edge only and enable interrupt on capture event
11 = Capture on any edge and enable interrupt on capture event

PS—Prescaler Value

The prescaler is programmed to divide the clock input by values from 1 to 256. The value 00000000 divides the clock by 1; the value 11111111 divides the clock by 256. The resolution of the timer varies directly with the size of the prescaler. In order to make smaller adjustments to the timer as needed, the prescaler should be as small as possible (see 3.5.2.6 General Purpose Timer Example).

3.5.2.2 Timer Reference Registers (TRR1, TRR2)

Each TRR is a 16-bit register containing the reference value for the timeout. TRR1 and TRR2 are memory-mapped read-write registers.

When working in the MC68008 mode (BUSW is low), writing the high byte of TRR1 and TRR2 will disable the timer's compare logic until the low byte is written.

TRR1 and TRR2 are set to all ones by reset. The reference value is not “reached” until TCN increments to equal TRR.

3.5.2.3 Timer Capture Registers (TCR1, TCR2)

Each TCR is a 16-bit register used to latch the value of the counter during a capture operation when an edge occurs on the respective TIN1 or TIN2 pin. TCR1 and TCR2 appear as memory-mapped read-only registers to the user.

When working in the MC68008 mode (BUSW is low), reading the high byte of TCR1 and TCR2 will disable the timer's capture logic until the low byte is read.

TCR1 and TCR2 are cleared at reset.

3.5.2.4 Timer Counter (TCN1, TCN2)

TCN1 and TCN2 are 16-bit up-counters. Each is memory-mapped and can be read and written by the user. A read cycle to TCN1 and TCN2 yields the current value of the timer and does not affect the counting operation.

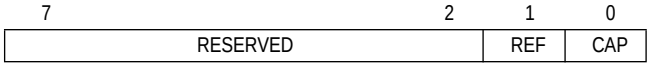
When working in the MC68008 mode (BUSW is low), reading the high byte of TCN1 and TCN2 will latch the low byte into a temporary register; a subsequent read cycle on the low byte yields the value of the temporary register.

A write cycle to TCN1 and TCN2 causes both the counter register and the corresponding prescaler to be reset to zero. In MC68008 mode (BUSW is low), a write cycle to either the high or low byte of the TCN will reset the counter register and the corresponding prescaler to zero.

3.5.2.5 Timer Event Registers (TER1, TER2)

Each TER is an 8-bit register used to report events recognized by any of the timers. On recognition of an event, the timer will set the appropriate bit in the TER, regardless of the corresponding interrupt enable bits (ORI and CE) in the TMR. TER1 and TER2, which appear to the user as memory-mapped registers, may be read at any time.

A bit is cleared by writing a one to that bit (writing a zero does not affect a bit's value). More than one bit may be cleared at a time. Both bits must be cleared before the timer will negate the INRQ to the interrupt controller. This register is cleared at reset.



CAP—Capture Event

The counter value has been latched into the TCR. The CE bits in the TMR are used to enable the interrupt request caused by this event.

REF—Output Reference Event

The counter has reached the TRR value. The ORI bit in the TMR is used to enable the interrupt request caused by this event.

Bits 7–2—Reserved for future use.

3.5.2.6 General Purpose Timer Example

This section gives two examples on how to program the general purpose timers.

3.5.2.6.1 Timer Example 1

Generate an interrupt every 10 mS using the 20 MHz system clock.

1. Take the desired interrupt period and divide by the timer clock period to get an initial count value to calculate prescaler.

$$\frac{Tout}{Tin} = \frac{10ms}{\frac{1}{20MHz}} = Count = 200,000$$

2. To calculate the value for the clock divider, divide the count by 65536 (2^{16}).

$$\frac{Count}{65536} = Divider = 3.05176$$

3. The divider must be rounded up to the next integer value. A clock divider of 4 then changes the input timer period to Tin*4. A new count is calculated based on the new timer period, and this value will be written to the TRR. The prescaler in the TMR is equal to the clock divider minus 1 (or 4-1 = 3).

$$\frac{Tout}{Tin(Divider)} = \frac{10ms}{50ns(4)} = 50,000$$

4. Program the TRR to $C350 (= 50000 decimal).
5. Program the TMR to $031B (prescaler = 3, ORI =1 to enable interrupt, FRR = 1 to re-start counter after reference is reached, ICLK = 01 to use the master clock, and RST = 1 to enabled the timer).

Fine adjustments can be made to the timer by varying the TRR up or down.

3.5.2.6.2 Timer Example 2

Generate a 100 Hz square wave using the 20 MHz system clock. As in Timer Example 1, the period is 10 mS, so we can use the same Prescaler and Reference values. When OM is set, the TOUT pin only toggles when the reference value is reached. Therefore the reference value must be divided by two in order to generate two edges every 100 mS.

1. Program the Port B control register to change the port pin from a general purpose input pin to TOUT.
2. Program the TRR to $61A8 (= 50000/2).
3. Program the TMR to $321B (prescaler = 3, OM =1 to toggle TOUT, FRR = 1 to restart

counter after reference is reached, ICLK = 01 to use the master clock, and RST = 1 to enabled the timer).

Fine adjustments can be made to the timer by varying the TRR up or down.

3.5.3 Timer 3 - Software Watchdog Timer

A watchdog timer is used to protect against system failures by providing a means to escape from unexpected input conditions, external events, or programming errors. Timer 3 may be used for this purpose. Once started, the watchdog timer must be cleared by software on a regular basis so that it never reaches its timeout value. Upon reaching the timeout value, the assumption may be made that a system failure has occurred, and steps can be taken to recover or reset the system.

3.5.3.1 Software Watchdog Timer Operation

The watchdog timer counts from zero to a maximum of 32767 (16.67 seconds at 16.00 MHz) with a resolution or step size of 8192 clock periods (0.5 ms at 16.00 MHz). This timer uses a 16-bit counter with an 8-bit prescaler value.

The watchdog timer uses the main clock divided by 16 as the input to the prescaler. The prescaler circuitry divides the clock input by a fixed value of 256. The output of this prescaler circuitry is connected to the input of the 16-bit counter. Since the least significant bit of the WCN is not used in the comparison with the WRR reference value, the effective value of the prescaler is 512.

The timer counts until the reference value is reached and then starts a new time count immediately. Upon reaching the reference value, the counter asserts the $\overline{\text{WDOG}}$ output for a period of 16 master clock (CLKO) cycles, and issues an interrupt to the interrupt controller. The value of the timer can be read any time.

To use the software watchdog function directly with the M68000 core, the timer 3 open-drain output pin ($\overline{\text{WDOG}}$) can be connected externally to the $\overline{\text{IPL2}}$–$\overline{\text{IPL0}}$ pins to generate a level 7 interrupt (normal mode), to $\overline{\text{IRQ7}}$ (dedicated mode), or to the $\overline{\text{RESET}}$ and $\overline{\text{HALT}}$ pin. After a total system reset, the $\overline{\text{WDOG}}$ pin function is enabled on pin PB7. The timer 3 counter is automatically enabled after reset.

The software watchdog timer has an 8-bit prescaler that is not accessible to the user, a read-only 16-bit counter, and a reference register (WRR).

3.5.3.2 Software Watchdog Reference Register (WRR)

WRR is a 16-bit register containing the reference value for the timeout. The EN bit of the register enables the timer. WRR appears as a memory-mapped read-write register to the user.

When operating in the MC68008 mode (BUSW is low), writing to the high byte of WRR will disable the timer compare logic until the low byte is written.

Reset initializes the register to $FFFF, enabling the watchdog timer and setting it to the maximum timeout period. This causes a timeout to occur if there is an error in the boot program.

15	1	0
REFERENCE VALUE		EN

3.5.3.3 Software Watchdog Counter (WCN)

WCN, a 16-bit up-counter, appears as a memory-mapped register and may be read at any time. Clearing EN in WRR causes the counter to be reset and disables the count operation.

A read cycle to WCN causes the current value of the timer to be read. When working in MC68008 mode (BUSW is low), reading the high byte of WCN will latch the low byte into a temporary register. When reading the low byte, the temporary register value is read. Reading the timer does not affect the counting operation.

A write cycle to WCN causes the counter and prescaler to be reset. In the MC68008 mode (BUSW is low), a write cycle to either the high or low byte resets the counter and the prescaler. A write cycle should be executed on a regular basis so that the watchdog timer is never allowed to reach the reference value during normal program operation.

3.6 EXTERNAL CHIP-SELECT SIGNALS AND WAIT-STATE LOGIC

The MC68302 provides a set of four programmable chip-select signals. Each chip-select signal has an identical internal structure. For each memory area, the user may also define an internally generated cycle termination signal ($\overline{\text{DTACK}}$). This feature eliminates board space that would be necessary for cycle termination logic.

The four chip-select signals allow four different classes of memory to be used: e.g., high-speed static RAM, slower dynamic RAM, EPROM, and nonvolatile RAM. If more than four chip selects are required, additional chip selects may be decoded externally, as on the MC68000.

The chip-select block diagram is shown in Figure 3-9.

The chip-select logic is active for memory cycles generated by internal bus masters (M68000 core, IDMA, SDMA, DRAM refresh) or external bus masters. These signals are driven externally on the falling edge of $\overline{\text{AS}}$ and are valid shortly after $\overline{\text{AS}}$ goes low.

For each chip select, the user programs the block size by choosing the starting address in the base register and the length in the option register. The starting address must be on a block boundary. Thus, an 8K block size must begin on an 8K address boundary, and a 64K block size must begin on a 64K address boundary, etc.

For a given chip-select block, the user may also choose 1) whether the chip-select block should be considered as read-only, write-only, or read/write, 2) whether the chip-select block should be active on only one particular function code signal combination or for all function codes, and 3) whether a $\overline{\text{DTACK}}$ should be automatically generated for this chip-select block, and after how many wait states.

$\overline{\text{DTACK}}$ generation occurs under the same constraints as the chip-select signal—if the chip-select signal does not activate, then neither will the $\overline{\text{DTACK}}$ signal.

Chip select 0 has the special property of being enabled upon system reset to the address range from 0 to 8K bytes. This property allows chip select 0 to function as the “boot ROM” select on system start-up. $\overline{\text{DTACK}}$ is initially enabled for six wait states on this chip select.

External masters may use the chip-select logic on the IMP during an external master access to external memory/peripherals. In this case, the external master chip-select timing diagram (see Figure 6-15) must be used. Since the chip-select logic is slightly slower when using external masters, an optional provision can be made to add an additional wait state to an external access by an external master. See the EMWS bit in the SCR for more details (3.8.3 System Control Bits).

A priority structure exists within the chip-select block. For a given address, the priority is as follows:

1. Access to any IMP internal address (BAR, dual-port RAM, etc.)
   No chip select asserted.
2. Chip Select 0
3. Chip Select 1
4. Chip Select 2
5. Chip Select 3

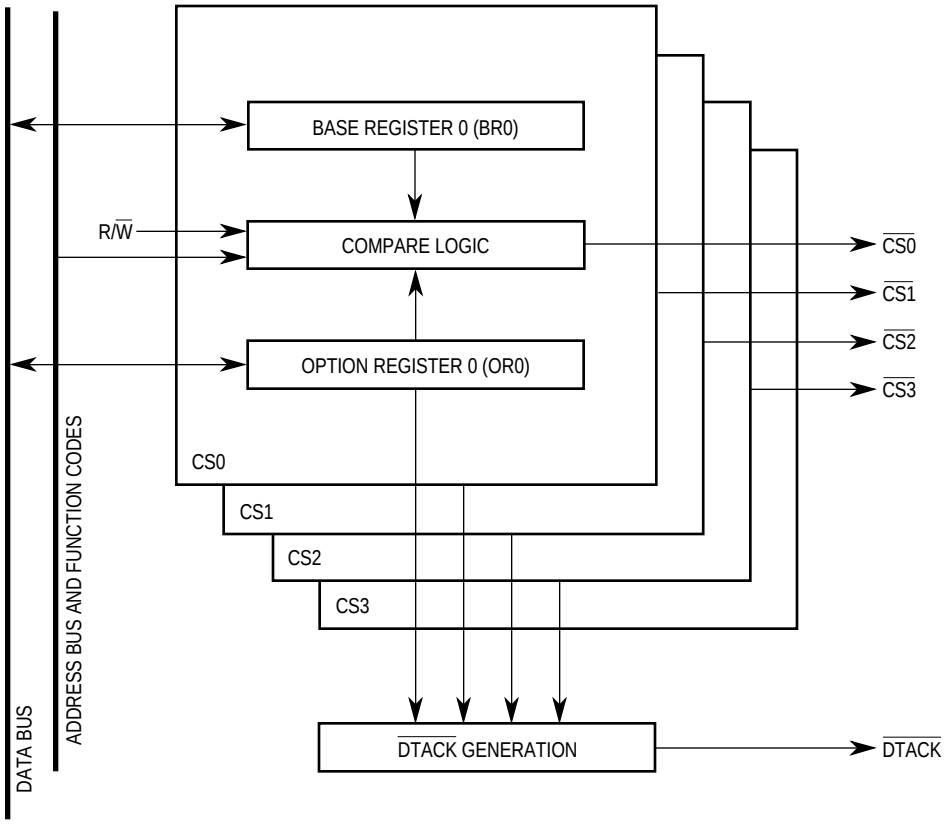


Figure 3-9. Chip-Select Block Diagram

The user should not normally program more than one chip-select line to the same area. When this occurs, the address compare logic will set address decode conflict (ADC) in the system control register (SCR) and generate $\overline{\text{BERR}}$ if address decode conflict enable (ADCE) is set. Only one chip-select line will be driven because of internal line priorities. $\overline{\text{CS0}}$ has the highest priority, and $\overline{\text{CS3}}$ the lowest. $\overline{\text{BERR}}$ will not be asserted on write accesses to the chip-select registers.

If one chip select is programmed to be read-only and another chip select is programmed to be write-only, then there will be no overlap conflict between these two chip selects, and the ADC bit will not be set.

When a bus master attempts to write to a read-only location, the chip-select logic will set write protect violation (WPV) in the SCR and generate $\overline{\text{BERR}}$ if write protect violation enable (WPVE) is set. The $\overline{\text{CS}}$ line will not be asserted.

NOTE

The chip-select logic is reset only on total system reset (assertion of $\overline{\text{RESET}}$ and $\overline{\text{HALT}}$). Accesses to the internal RAM and registers, including the system configuration registers (BAR and

SCR), will not activate the chip-select lines. Thus, it is convenient to use one of the chip-select lines to select external ROM/RAM that overlaps these register addresses, since, in this way, bus contention is completely avoided during a read access to these addresses. If, in a given application, it is not possible to use the chip-select lines for this purpose, the IAC signal may be used externally to prevent bus contention.

NOTE

The chip-select logic does not allow an address match during interrupt acknowledge cycles.

A special case occurs when the locked read-modify-write test and set (TAS) instruction is executed in combination with the chip selects. The assertion of wait states on the write portion of the cycle will only occur if the RMCST bit in the SCR is set. Refer to 3.8.3 System Control Bits for more details.

3.6.1 Chip-Select Logic Key Features

Key features of the chip-select logic are as follows:

- Four Programmable Chip-Select Lines
- Various Block Sizes: 8K, 16K, 32K, 64K, 128K, 256K, 512K, 1M, 2M, 4M, 8M, and 16M Bytes
- Read-Only, Write-Only, or Read-Write Select
- Internal $\overline{\text{DTACK}}$ Generation with Wait-State Options
- Default Line ($\overline{\text{CS0}}$) to Select an 8K-Boot ROM Containing the Reset Vector and Initial Program

3.6.2 Chip-Select Registers

Each of the four chip-select units has two registers that define its specific operation. These registers are a 16-bit base register (BR) and a 16-bit option register (OR) (e.g., BR0 and OR0). These registers may be modified by the M68000 core. The BR should normally be programmed after the OR since the BR contains the chip-select enable bit.

3.6.2.1 Base Register (BR3–BR0)

These 16-bit registers consist of a base address field, a read-write bit, and a function code field.

FC2–FC0 —Function Code Field

This field is contained in bits 15–13 of each BR. These bits are used to set the address space function code. The address compare logic uses these bits to determine whether an

address match exists within its address space and, therefore, whether to assert the chip-select line.

111 = Not supported; reserved. Chip select will not assert if this value is chosen.
110 = Value may be used.
•
•
•
000 = Value may be used.

After system reset, the FC field in BR3–BR0 defaults to supervisor program space (FC = 110) to select a ROM device containing the reset vector. Because of the priority mechanism and the EN bit, only the $\overline{CS0}$ line is active after a system reset.

NOTE

The FC bits can be masked and ignored by the chip-select logic using CFC in the OR.

Bits 12–2—Base Address

These bits are used to set the starting address of a particular address space. The address compare logic uses only A23–A13 to cause an address match within its block size. The base address should be located on a block boundary. For example, if the block size is 64k bytes, then the base address should be a multiple of 64k.

After system reset, the base address defaults to zero to select a ROM device on which the reset vector resides. All base address values default to zero on system reset, but, because of the priority mechanism, only $\overline{CS0}$ will be active.

NOTE

All address bits can be masked and ignored by the chip-select logic through the base address mask in the OR.

RW—Read/Write

0 = The chip-select line is asserted for read operations only.
1 = The chip-select line is asserted for write operations only.

After system reset, this bit defaults to zero (read-only operation).

NOTE

This bit can be masked and ignored by the read-write compare logic, as determined by MRW in the OR. The line is then asserted for both read and write cycles.

On write protect violation cycles (RW = 0 and MRW = 1), $\overline{BERR}$ will be generated if WPVE is set, and WPV will be set.

If the write protect mechanism is used by an external master, the R/$\overline{W}$ low to $\overline{AS}$ asserted timing should be 16 ns minimum.

EN—Enable

0 = The chip-select line is disabled.
1 = The chip-select line is enabled.

After system reset, only $\overline{CS0}$ is enabled; $\overline{CS3}$–$\overline{CS1}$ are disabled. In disable CPU mode, $\overline{CS3}$–$\overline{CS0}$ are disabled at system reset. The chip select does not require disabling before changing its parameters.

3.6.2.2 Option Registers (OR3–OR0)

These four 16-bit registers consist of a base address mask field, a read/write mask bit, a compare function code bit, and a $\overline{DTACK}$ generation field.

Bits 15–12—DTACK Field

These bits are used to determine whether $\overline{DTACK}$ is generated internally with a programmable number of wait states or externally by the peripheral. With internal $\overline{DTACK}$ generation, zero to six wait states can be automatically inserted before the $\overline{DTACK}$ pin is asserted as an output (see Port A Control Register (PACNT)).

Table 3-8. DTACK Field Encoding

Bits			Description
15	14	13	
0	0	0	No Wait State
0	0	1	1 Wait State
0	1	0	2 Wait States
0	1	1	3 Wait States
1	0	0	4 Wait States
1	0	1	5 Wait States
1	1	0	6 Wait States
1	1	1	External DTACK

When all the bits in this field are set to one, $\overline{DTACK}$ must be generated externally, and the IMP or external bus master waits for $\overline{DTACK}$ (input) to terminate its bus cycle. After system reset, the bits of the DTACK field default to six wait states.

The DTACK generator uses the IMP internal clock to generate the programmable number of wait states. For asynchronous external bus masters, the programmable number of wait states is counted directly from the internal clock. When no wait state is programmed (DTACK = 000), the DTACK generator will generate $\overline{DTACK}$ asynchronously.

The $\overline{CS}$ lines are asserted slightly earlier for internal IMP master memory cycles than for an external master using the $\overline{CS}$ lines. Set external master wait state (EMWS) in the SCR whenever these timing differences require an extra memory wait state for external masters.

NOTE

Do not assert $\overline{\text{DTACK}}$ externally when it is programmed to be generated internally.

Bits 12–2—Base Address Mask

These bits are used to set the block size of a particular chip-select line. The address compare logic uses only the address bits that are not masked (i.e., mask bit set to one) to detect an address match within its block size.

0 = The address bit in the corresponding BR is masked; the address compare logic does not use this address bit. The corresponding external address line value is a don't care in the comparison.
1 = The address bit in the corresponding BR is not masked; the address compare logic uses this address bit.

For example, for a 64K-byte block, this field should be M13, M14, M15 = 0 with the rest of the base address mask bits (M23–M16) equal to one.

After system reset, the bits of the base address mask field default to ones (selecting the smallest block size of 8K) to allow $\overline{\text{CS0}}$ to select the ROM device containing the reset vector.

MRW—Mask Read/Write

0 = The RW bit in the BR is masked. The chip select is asserted for both read and write operations.
1 = The RW bit in the BR is not masked. The chip select is asserted for read-only or write-only operations as programmed by the corresponding RW bit in BR3–BR0.

After system reset, this bit defaults to zero.

CFC—Compare Function Code

0 = The FC bits in the BR are ignored. The chip select is asserted without comparing the FC bits. If the application requires the user to recognize several address spaces (e.g., user space without distinguishing between data and program space), FC bits must be decoded externally.
1 = The FC bits on the BR are compared. The address space compare logic uses the FC bits to assert the $\overline{\text{CS}}$ line.

After system reset, this bit defaults to one.

NOTE

Even when CFC = 0, if the function code lines are internally or externally generated as “111”, the chip select will not be asserted.

3.6.3 Chip Select Example

Set up chip select 2 to assert for a 1 Megabyte block of external RAM beginning at $200000 with 1 wait state. Note that the address must be on a block boundary (i.e. the starting address of a 1 Megabyte block could not be $210000).

1. Calculate what the mask should be. For a 1 Megabyte block, the address lines A0 through A19 are used to address bytes within the block, so they need to be masked out.
2. Write $3E00 to OR2 (DTACK=1 for 1 wait state, M23-M20 = 1 to use these bits in the comparison, M19-M13 = 0 to mask these address bits, MRW = 0 to enable the chip select for both read and write, and CFC = 0 to mask off function code comparison).
3. Write $0401 to BR2 (FC2-FC0 = 0 don't care, A23-A13 = base address, RW = 0 don't care, and EN =1 to enable the chip select.

NOTE

The mask bits in the OR are used to mask the individual address bits, so in the previous example, if bit 12 (M23) was changed to a zero, then CS2 would assert for a 1 Megabyte block beginning at $200000 and a 1 Megabyte block at $A00000.

3.7 ON-CHIP CLOCK GENERATOR

The IMP has an on-chip clock generator that supplies clocks to both the internal M68000 core and peripherals and to an external pin. The clock circuitry uses three dedicated pins: EXTAL, XTAL, and CLKO.

The external clock/crystal (EXTAL) input provides two clock generation options. EXTAL may be used to interface the internal generator to an external crystal (see Figure 3-10). Typical circuit parameters are C1 = C2 = 25 pF and R = 700 kΩ using a parallel resonant crystal. Typical crystal parameters are Co < 10 pF and Rx = 50 Ω. The equivalent load capacitance (C_L) of this circuit is 20 pF, calculated as (C1 + C_{in})/2, where C1 = C2 = 25 pF and C_{in} = 15 pF maximum on the EXTAL pin.

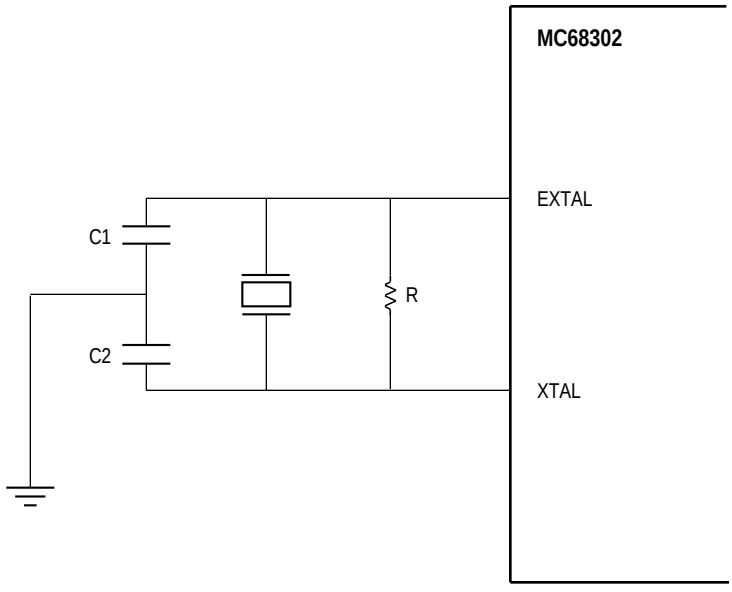


Figure 3-10. Using an External Crystal

EXTAL can also accept a CMOS-level clock input. The crystal output (XTAL) connects the internal crystal generator output to an external crystal. If an external clock is used, XTAL should be left unconnected. The CLKO pin, which drives the high-speed system clock, may be used to synchronize other peripherals to the IMP system clock.

3.8 SYSTEM CONTROL

The IMP system control consists of a System Control Register (SCR) that configures the following functions:

- System Status and Control Logic
- $\overline{AS}$ Control During Read-Modify-Write-Cycles
- Disable CPU (M68000) Logic
- Bus Arbitration Logic with Low-Interrupt Latency Support
- Hardware Watchdog
- Low-Power (Standby) Modes
- Freeze Control

3.8.1 System Control Register (SCR)

The SCR is a 32-bit register that consists of system status and control bits, a bus arbiter control bit, hardware watchdog control bits, low-power control bits, and freeze select bits. Refer to Figure 3-11, Table 3-7, and to the following paragraphs for a description of each bit in this register. The SCR is a memory-mapped read-write register. The address of this register is fixed at $0F4 in supervisor data space (FC = 5).

31	30	29	28	27	26	25	24
0	0	0	0	IPA	HWT	WPV	ADC

23	22	21	20	19	18	17	16
0	ERRE	VGE	WPVE	RMCST	EMWS	ADCE	BCLM

15	14	13	12	11	10	8
FRZW	FRZ2	FRZ1	SAM	HWDEN	HWDCN2–HWDCN0	

7	6	5	4	0
LPREC	LPP16	LPEN	LOW-POWER CLOCK DIVIDER	

Figure 3-11. System Control Register

Table 3-9. SCR Register Bits

Bit	Name	Section(s)
IPA	Interrupt Priority Active	3.8.2
HWT	Hardware Watchdog Timeout	3.8.2, 3.8.6
WPV	Write Protect Violation	3.8.2
ADC	Address Decode Conflict	3.8.2
ERRE	External RISC Request Enable	3.9
VGE	Vector Generation Enable	3.8.4
WPVE	Write Protect Violation Enable	3.8.3
RMCST	Read-Modify-Write Cycle Special Treatment	3.8.3
EMWS	External Master Wait State	3.8.3, 3.8.4
ADCE	Address Decode Conflict Enable	3.8.3
BCLM	Bus Clear Mask	3.8.2, 3.8.3, 3.8.5
FRZW	Freeze Watchdog Timer Enable	3.8.8
FRZ1	Freeze Timer 1 Enable	3.8.8
FRZ2	Freeze Timer 2 Enable	3.8.8
SAM	Synchronous Access Mode	3.8.3, 3.8.4
HWDEN	Hardware Watchdog Enable	3.8.6
HWDCN	Hardware Watchdog Count	3.8.6
LPREC	Low-Power Recovery	3.8.7
LPP16	Low-Power Clock Prescale Divide by 16	3.8.7
LPEN	Low-Power Enable	3.8.7
LPCD	Low-Power Clock Divider Selects	3.8.7

3.8.2 System Status Bits

The eight most significant bits of the SCR are used to report events recognized by the system control logic. On recognition of an event, this logic sets the corresponding bit in the SCR. The bits may be read at any time. A bit is reset by one and is left unchanged by zero. More than one bit may be reset at a time.

After system reset (simultaneous assertion of $\overline{\text{RESET}}$ and $\overline{\text{HALT}}$), these bits are cleared.

IPA—Interrupt Priority Active

This bit is set when the M68000 core has an unmasked interrupt request. When bus clear mask (BCLM) is set, $\overline{\text{BCLR}}$ and the internal bus clear to the IDMA are asserted.

NOTE

If BCLM is set, an interrupt handler will normally clear IPA at the end of the interrupt routine to allow an alternate bus master to regain the bus; however, if BCLM is cleared, no additional action need be taken in the interrupt handler.

In the case of nested interrupts, the user may wish to clear the IPA bit only at the end of the original lower priority interrupt routine to keep $\overline{\text{BCLR}}$ asserted until it completes. To guarantee that

this happens and that other pending interrupts at the same original priority level also execute with $\overline{BCLR}$ continuously asserted, the following technique may be used. Using a parallel I/O line connected to the IRQ1 line, the original priority level interrupt toggles this I/O line just before it executes the RTE instruction, causing a request for a level 1 interrupt. Since this is the lowest interrupt level, this routine will not be executed until all other pending interrupt routines have executed. Then in the level 1 interrupt routine, the IPA bit in the SCR is cleared.

HWT—Hardware Watchdog Timeout

This bit is set when the hardware watchdog (see 3.8.6 Hardware Watchdog) reaches the end of its time interval; $\overline{BERR}$ is generated following the watchdog timeout, even if this bit is already set.

WPV—Write Protect Violation

This bit is set when a bus master attempts to write to a location that has RW set to zero (read only) in its associated base register (BR3–BR0). Provided WPVE (bit 20) is set, $\overline{BERR}$ will be asserted on the bus cycle that sets this bit. If WPV and WPVE are both set when a write protect violation occurs, $\overline{BERR}$ will still be generated.

ADC—Address Decode Conflict

This bit is set when a conflict has occurred in the chip-select logic because two or more chip-select lines attempt assertion in the same bus cycle. This conflict may be caused by a programming error in which the user-allocated memory areas for each chip select overlap each other. Provided ADCE (bit 17) is set, the occurrence of ADC will cause $\overline{BERR}$ to be asserted. If this bit is already set when another address decode conflict occurs, $\overline{BERR}$ will still be generated. The chip-select logic will protect the IMP from issuing two simultaneous chip selects by employing a priority system.

NOTE

Regardless of the state of the chip-select programming, this bit will not be set and $\overline{BERR}$ will not be asserted for an address decode conflict occurring during access to a system configuration register. This is provided to guarantee access to the system configuration registers (BAR and SCR) during initialization.

3.8.3 System Control Bits

The system control logic uses six control bits in the SCR.

WPVE—Write Protect Violation Enable

0 = $\overline{BERR}$ is not asserted when a write protect violation occurs.
1 = $\overline{BERR}$ is asserted when a write protect violation occurs.

After system reset, this bit defaults to zero.

NOTE

WPV will be set, regardless of the value of WPVE.

RMCST—RMC Cycle Special Treatment

0 = The locked read-modify-write cycles of the TAS instruction will be identical to the M68000 ($\overline{AS}$ and $\overline{CS}$ will be asserted during the entire cycle). The arbiter will issue $\overline{BG}$, regardless of the M68000 core $\overline{RMC}$. If an IMP chip select is used, the $\overline{DTACK}$ generator will insert wait states on the read cycle only.

1 = The MC68302 uses $\overline{RMC}$ to negate $\overline{AS}$ and $\overline{CS}$ at the end of the read portion of the RMC cycle and reasserts $\overline{AS}$ and $\overline{CS}$ at the beginning of the write portion. $\overline{BG}$ will not be asserted until the end of the write portion. If an IMP chip select is used, the $\overline{DTACK}$ generator will insert wait states on both the read and write portion of the cycles.

The assertion of the $\overline{RMC}$ by the M68000 core is seen by the arbiter and will prevent the arbiter from issuing bus grants until the completion of M68000-initiated locked read-modify-write activity. After system reset, this bit defaults to zero.

EMWS—External Master Wait State (EMWS);

When EMWS is set and an external master is using the chip-select logic for $\overline{DTACK}$ generation or is synchronously reading from the internal peripherals (SAM = 1), one additional wait state will be inserted in external master cycle to external memory and peripherals and also in every cycle from the external master to MC68302 internal memory and peripherals. When EMWS is cleared, all synchronous internal accesses will be with zero wait states, and the chip-select logic will generate $\overline{DTACK}$ after the exact programmed number of wait states. The chip-select lines are asserted slightly earlier for internal master memory cycles than for an external master. EMWS should be set whenever these timing differences will necessitate an additional wait state for external masters. After system reset, this bit defaults to zero.

ADCE—Address Decode Conflict Enable

0 = $\overline{BERR}$ is not asserted by a conflict in the chip-select logic when two or more chip-select lines are programmed to overlap the same area.

1 = $\overline{BERR}$ is asserted by a conflict in the chip-select logic when two or more chip-select lines are programmed to overlap the same area.

After system reset, this bit defaults to zero.

NOTE

ADC will be set, regardless of the value of ADCE.

BCLM—Bus Clear Mask

0 = The arbiter does not use the M68000 core internal IPEND signal to assert the internal and external bus clear signals.

1 = The arbiter uses the M68000 core internal IPEND signal to assert the internal and external bus clear signals.

After system reset, this bit defaults to zero. If BCLM is set, then the typical maximum interrupt latency is about 78 clocks in a zero-wait-state system. This assumes a standard instruction mix, that the IDMA is just beginning a four-bus-cycle transfer when the interrupt becomes pending, and that an SDMA has an access pending (one bus cycle). Interrupt execution time is 44 clocks and includes the time to execute the interrupt acknowledge cycle, save the status register and PC value on the stack, and then vector to the first location of the interrupt service routine. Thus, the calculation is 78 = 14 (instruction completion) + 20 (DMAs) + 44 (interrupt execution).

SDMA operation is not affected by the BCLM bit. Note that the SDMA accesses only one byte/word of external memory at a time before giving up the bus and that accesses are relatively infrequent. External bus master operation may or may not be affected by the BCLM bit, depending on whether the $\overline{\text{BCLR}}$ signal is used to clear the external master off the bus.

Without using the BCLM bit, the maximum interrupt latency includes the maximum time that the IDMA or external bus master could use the bus in the worst case. Note that the IDMA can limit its bus usage if its requests are generated internally.

NOTE

The IPA status bit will be set, regardless of the BCLM value.

SAM—Synchronous Access Mode

This bit controls how external masters may access the MC68302 peripheral area. This bit is not relevant for applications that do not have external bus masters that access the MC68302. In applications such as disable CPU mode, in which the M68000 core is not operating, the user should note that SAM may be changed by an external master on the first access of the MC68302, but that first write access must be asynchronous with three wait states. (If $\overline{\text{DTACK}}$ is used to terminate bus cycles, this change need not influence hardware.)

0 = Asynchronous accesses. All accesses to the MC68302 internal RAM and registers (including BAR and SCR) by an external master are asynchronous to the MC68302 clock. Read and write accesses are with three wait states, and $\overline{\text{DTACK}}$ is asserted by the MC68302 assuming three wait-state accesses. This is the default value.

1 = Synchronous accesses. All accesses to the MC68302 internal RAM and registers (including BAR and SCR) must be synchronous to the MC68302 clock. Synchronous read accesses may occur with one wait state if EMWS is also set to one.

3.8.4 Disable CPU Logic (M68000)

The MC68302 can be configured to operate solely as a peripheral to an external processor. In this mode, the on-chip M68000 CPU should be disabled by strapping DISCPU high during system reset ($\overline{\text{RESET}}$ and $\overline{\text{HALT}}$ asserted simultaneously). The internal accesses to the MC68302 peripherals and memory may be asynchronous or synchronous. During synchronous reads, one wait state may be used if required (EMWS bit set). The following pins change their functionality in this mode:

1. $\overline{\text{BR}}$ will be an output from the IDMA and SDMA to the external M68000 bus, rather than being an input to the MC68302.

2. $\overline{BG}$ will be an input to the IDMA and SDMA from the external M68000 bus, rather than being an output from the MC68302. When BG is sampled as low by the MC68302, it waits for $\overline{AS}$, $\overline{BERR}$, $\overline{HALT}$, and $\overline{BGACK}$ to be negated, and then asserts $\overline{BGACK}$ and performs one or more bus cycles. See Section 6 for timing diagrams.
3. $\overline{BCLR}$ will be an input to the IDMA, but will remain an output from the SDMA.
4. The interrupt controller will output its interrupt request lines ($\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$) normally sent to the M68000 core on pins $\overline{IOUT0}$, $\overline{IOUT1}$, and $\overline{IOUT2}$, respectively. $\overline{AVEC}$, $\overline{RMC}$, and $\overline{CS0}$, which share pins with $\overline{IOUT0}$, $\overline{IOUT1}$, and $\overline{IOUT2}$, respectively, are not available in this mode.

DISCPU should remain continuously high during disable CPU mode operation. Although the $\overline{CS0}$ pin is not available as an output from the device in disable CPU mode, it may be enabled to provide $\overline{DTACK}$ generation. In disable CPU mode, BR0 is initially $C000.

Accesses by an external master to the MC68302 RAM and registers may be asynchronous or synchronous to the MC68302 clock. (This feature is actually available regardless of disable CPU mode). See the SAM and EMWS bits in the SCR for details.

In disable CPU mode, the interrupt controller may be programmed to generate or not generate interrupt vectors during interrupt acknowledge cycles. When multiple MC68302 devices share a single M68000 bus, vector generation at level 4 should be prevented on all but one MC68302. When using disable CPU mode to implement an interface, such as between the MC68020 and a single MC68302, vector generation can be enabled. For this purpose, the VGE bit is defined.

VGE—Vector Generation Enable

0 = In disable CPU mode, the MC68302 will not output interrupt vectors during interrupt acknowledge cycles.
1 = In disable CPU mode, the MC68302 will output interrupt vectors for internal level 4 interrupts (and for levels 1, 6, and/or 7 as enabled in the interrupt controller) during interrupt acknowledge cycles.

NOTE

Do not use the function code value “111” during external accesses to the IMP, except during interrupt acknowledge cycles.

In disable CPU mode, the low-power modes will be entered immediately upon the setting of the LPEN bit in the SCR by an external master. In this case, low-power mode will continue until the LPEN bit is cleared. Users may wish to use a low-power mode in conjunction with disable CPU mode to save power consumed by the disabled M68000 core.

All MC68302 functionality not expressly mentioned in this section is retained in disable CPU mode and operates identically as before.

NOTE

Even without the use of the disable CPU logic, another processor can be granted access to the IMP on-chip peripherals by re-

questing the M68000 bus with $\overline{BR}$. See 3.8.6 Hardware Watchdog for further details.

3.8.5 Bus Arbitration Logic

Both internal and external bus arbitration are discussed in the following paragraphs.

3.8.5.1 Internal Bus Arbitration

The IMP bus arbiter supports three bus request sources in the following standard priority:

1. External bus master ($\overline{BR}$ pin)
2. SDMA for the SCCs (six channels)
3. IDMA (one channel)

When one of these sources desires the bus, the M68000 core will be forced off through an internal bus request signal ($\overline{CBR}$) from the bus arbiter to the M68000 core (see Figure 3-12). When the arbiter detects the assertion of the M68000 core bus grant ($\overline{CBG}$) signal, it asserts the requester's bus grant signal according to its priority. Thus, as seen externally, the SDMA and IDMA channels do not affect $\overline{BR}$ and $\overline{BG}$, but only $\overline{BGACK}$ (unless disable CPU mode is used).

The MC68302 provides several options for changing the preceding bus master priority list. The options are configured by setting the BCLM bit in the SCR and deciding whether or not the $\overline{BCLR}$ pin is used externally to cause external bus masters to relinquish the bus (see Table 3-10).

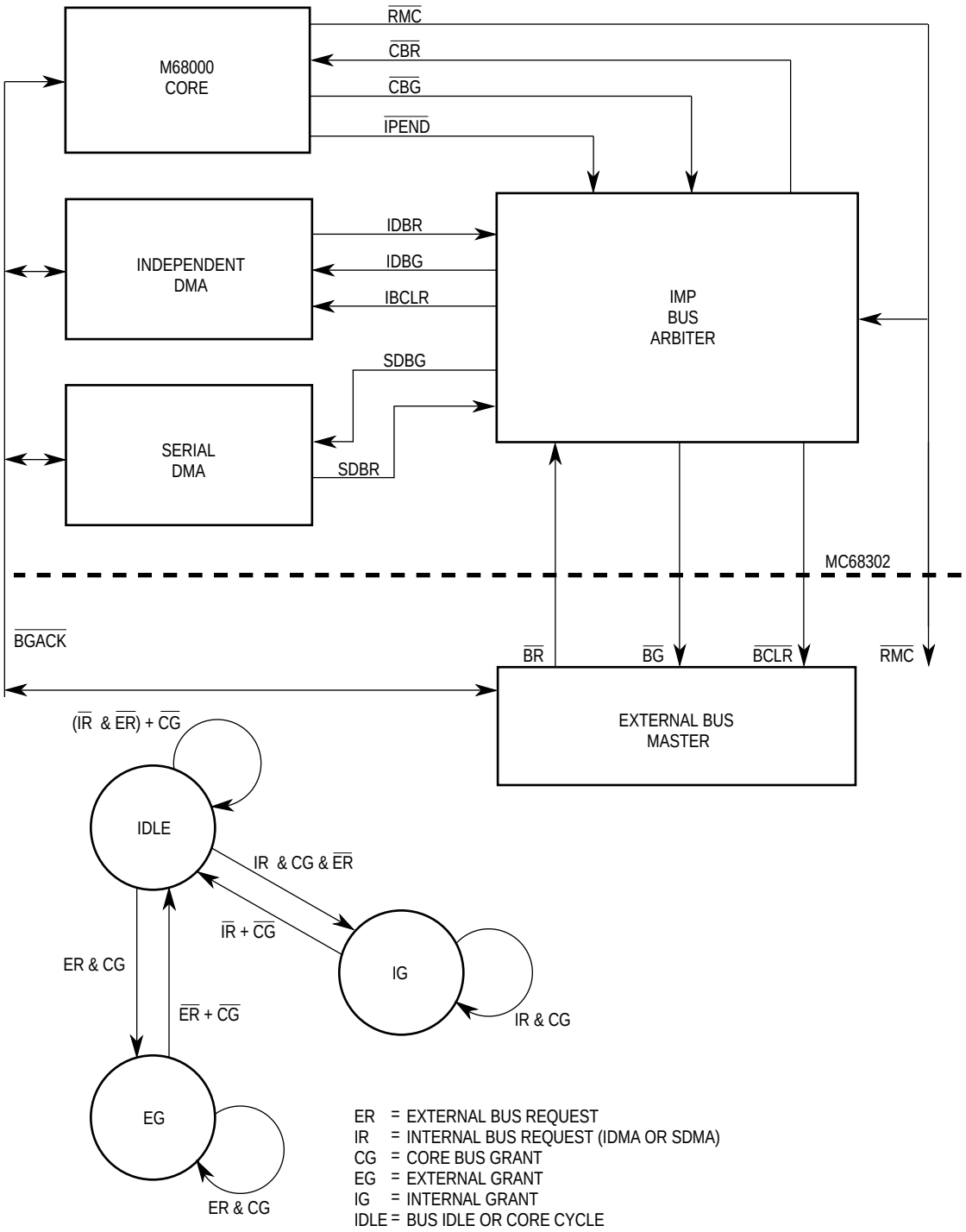


Figure 3-12. IMP Bus Arbiter

Table 3-10. Bus Arbitration Priority Table

$\overline{\text{BCLR}}$ Ignored BCLM = 0	$\overline{\text{BCLR}}$ Used BCLM = 0	$\overline{\text{BCLR}}$ Ignored BCLM = 1	$\overline{\text{BCLR}}$ Used BCLM = 1
$\overline{\text{BR}}$ Pin SDMA IDMA M68000 Interrupts M68000	SDMA IDMA $\overline{\text{BR}}$ Pin M68000 Interrupts M68000	$\overline{\text{BR}}$ Pin SDMA M68000 Interrupts IDMA[4] M68000	SDMA M68000 Interrupts IDMA[4] $\overline{\text{BR}}$ Pin M68000

NOTES:
1. The SDMA on a given IMP always has a higher priority than the IDMA on that IMP.
2. This table assumes the M68000 core is not in disable CPU mode. In disable CPU mode, the SDMA and IDMA make requests to the M68000 bus when they wish to become bus masters.
3. "BCLR Used" means that the BCLR pin is used externally to force the external bus master off the bus, even though its priority is still the highest in the system from the standpoint of the IMP bus arbiter.
4. The bus arbitration priority for IDMA in the two rightmost columns of the table applies only to the case when the IDMA request is internally generated; for the cases of external request, the bus arbitration priority of IDMA is right below that of SDMA.

The IMP bus arbiter also supports an M68000 core low-interrupt latency option. When the M68000 core processor has an unmasked interrupt request, it asserts an internal interrupt pending signal (IPEND). The bus arbiter uses this signal according to BCLM in the SCR to assert external ($\overline{\text{BCLR}}$) and internal bus-clear (IBCLR) signals. These bus-clear signals allow the M68000 core to eliminate long latencies potentially associated with an external bus master or the IDMA, respectively.

The external $\overline{\text{BCLR}}$ is asserted whenever 1) one of the SDMA channels requests the bus when the IDMA is not the bus master or 2) the M68000 core has an unmasked pending interrupt request, provided BCLM in the SCR is set. In this case, $\overline{\text{BCLR}}$ will be asserted until the interrupt priority active (IPA) bit in the SCR is cleared. To implement this feature, $\overline{\text{BCLR}}$ would be used to force external devices to release bus ownership.

IBCLR to the IDMA is asserted whenever 1) an external bus master requests the bus ($\overline{\text{BR}}$ asserted); 2) the M68000 core has an unmasked pending interrupt request, provided BCLM in the SCR is set and the IDMA request is internally generated, and in this case, BCLR will be asserted until IPA is cleared (Note that $\overline{\text{BCLR}}$ could be used to negate $\overline{\text{DREQ}}$ when the IDMA is in external request mode); 3) the M68000 CPU is disabled, and BCLR is asserted.

The IBCLR signal causes the IDMA to release bus ownership at the end of the current operand transfer. IBCLR is not routed to the SDMA channels since they always release bus ownership after one operand transfer.

RMC is issued by the M68000 core and can be used by the internal bus arbiter to delay issuance of BG during read-modify-write cycles. This is controlled by the RMCST bit in the SCR. Otherwise, the MC68000/MC68008 core may be forced off the bus after any bus cycle.

3.8.5.2 External Bus Arbitration

An external bus master may gain ownership of the M68000 bus by asserting the bus request ($\overline{\text{BR}}$) pin. After gaining ownership, it may access the IMP registers or RAM or any system memory address. Chip selects and system control functions, such as the hardware watchdog, continue to operate.

When an external master desires to gain ownership, the standard M68000 bus arbitration protocol should be used:

1. Issue $\overline{BR}$ (to the IMP on-chip bus arbiter).
2. Wait for $\overline{BG}$ (from the IMP on-chip bus arbiter).
3. When $\overline{BG}$ is asserted, wait for the negation of both $\overline{AS}$ and $\overline{BGACK}$.
4. Assert $\overline{BGACK}$ and begin external master bus cycles.
5. Negate $\overline{BR}$ (to the IMP on-chip bus arbiter), causing $\overline{BG}$ to be negated by the IMP on-chip bus arbiter.
6. Negate $\overline{BGACK}$ after the external master bus cycles have completed.

This protocol is also followed by the on-chip bus masters (IDMA, SDMA, and DRAM refresh) except that they request the bus internally from the on-chip bus arbiter.

In the disable CPU mode, the IMP makes requests for the bus rather than granting the bus. In such a system, the IMP functions as an external master, and the external processor (e.g., an MC68030) need not assert $\overline{BGACK}$ as it accesses the IMP's on-chip RAM and registers.

NOTE

When the IMP's BUSW pin is low causing the M68000 core to operate as an MC68008, the $\overline{BGACK}$ signal should still be used in bus arbitration control. On the original MC68008, the $\overline{BGACK}$ signal was not available externally, and therefore could not be used.

3.8.6 Hardware Watchdog

The hardware watchdog logic is used to assert $\overline{BERR}$ and set HWT when a bus cycle is not terminated by $\overline{DTACK}$ and after a programmable number of clock cycles has elapsed. The hardware watchdog logic has a 10-bit downcounter and a 4-bit prescaler. When enabled, the watchdog timer commences counting clock cycles as $\overline{AS}$ is asserted (for internal or external bus masters). The count is terminated normally by the negation of $\overline{AS}$; however, if the count reaches zero before $\overline{AS}$ is negated, $\overline{BERR}$ will be asserted until $\overline{AS}$ is negated. The hardware watchdog will operate with internal as well as external bus masters.

The hardware watchdog logic uses four bits in the SCR.

HWDEN—Hardware Watchdog Enable

0 = The hardware watchdog is disabled.
1 = The hardware watchdog is enabled.

After system reset, this bit defaults to one to enable the hardware watchdog.

HWDCN–HWDCN0—Hardware Watchdog Count 2–0

000 = $\overline{\text{BERR}}$ is asserted after 128 clock cycles (8 μs, 16-MHz clock)
001 = $\overline{\text{BERR}}$ is asserted after 256 clock cycles (16 μs, 16-MHz clock)
010 = $\overline{\text{BERR}}$ is asserted after 512 clock cycles (32 μs, 16-MHz clock)
011 = $\overline{\text{BERR}}$ is asserted after 1K clock cycles (64 μs, 16-MHz clock)
100 = $\overline{\text{BERR}}$ is asserted after 2K clock cycles (128 μs, 16-MHz clock)
101 = $\overline{\text{BERR}}$ is asserted after 4K clock cycles (256 μs, 16-MHz clock)
110 = $\overline{\text{BERR}}$ is asserted after 8K clock cycles (512 μs, 16-MHz clock)
111 = $\overline{\text{BERR}}$ is asserted after 16K clock cycles (1 ms, 16-MHz clock)

After system reset, these bits default to all ones; thus, $\overline{\text{BERR}}$ will be asserted after 1 ms for a 16-MHz system clock.

NOTE

Successive timeouts of the hardware watchdog may vary slightly in length. The counter resolution is 16 clock cycles.

3.8.7 Reducing Power Consumption

There are a number of ways to reduce power consumption on the IMP. They can be classified as general power-saving tips and low-power modes.

3.8.7.1 Power-Saving Tips

Without using any of the IMP low-power modes, power consumption may be reduced in the following ways.

1. The system clock frequency of the IMP may be reduced to the lower limit of its operating frequency range (e.g., 8 MHz) as specified in Section 6 Electrical Characteristics.
2. When not used, the SCCs should be disabled by clearing the ENT and ENR bits in the SCM registers.
3. If not needed, the SCC baud rate generators should be disabled or caused to clock at a low frequency. The baud rate generators are initialized to a very fast clock rate after reset, which can be reduced by programming the SCON register.
4. The two general-purpose timer prescalers should be set to the maximum divider value, and the timers should be disabled if not used.
5. Any unneeded peripheral output pins that are multiplexed with parallel I/O pins should be left configured as parallel I/O pins. The smaller the number of output transistors switching, the less current used.

3.8.7.2 Low-Power (Standby) Modes

The IMP also supports several types of low-power modes. The low-power modes on the IMP are used when no processing is required from the M68000 core and when it is desirable to reduce system power consumption to its minimum value. All low-power modes are entered by first setting the low-power enable (LPEN) bit, and then executing the M68000 STOP instruction.

At the end of the STOP instruction, a major change to the IMP occurs. The M68000 core immediately goes into a standby state in which it executes no instructions. In this state, the clock internally sent to the M68000 core is internally divided, saving power. The amount of this divide ratio is configured by the user. At the same time, however, the rest of the IMP continues to operate at the normal system frequency (i.e., the frequency on the EXTAL pin). All peripherals continue to operate normally during this time. Also, during low-power modes, all IMP external signals continue to function normally and at full speed.

In all modes, any of the 16 possible internal interrupt request (INRQ) sources can cause the IMP to leave a low-power mode. Masked interrupt sources will never cause a lower power mode to be exited. If it is desired to have an external signal cause the IMP to exit a low-power mode, it must be routed to one of the PB11–PB8 port pins with interrupt capability, so that an INRQ interrupt can be generated.

There are three low-power modes: low power, lowest power, and lowest power with external clock. Low-power mode allows execution to resume immediately upon recognition of the interrupt, with no loss of any IMP state information. Lowest power mode requires execution to resume with an internal M68000 reset. The M68000 state is lost, but the rest of the IMP peripheral states are completely retained. The lowest power mode with external clock offers the absolute minimum power consumption with the IMP, but requires external hardware.

3.8.7.2.1 Low-Power Mode

This mode is possible if the user-selected low-power frequency applied to the M68000 core remains above the operating limits specified in Section 6 Electrical Characteristics (e.g., 8 MHz). In this mode, LPREC is set to zero. Once an INRQ interrupt becomes pending, the system control block switches the M68000 core back to full frequency and power, and begins handling the interrupt in the usual manner. No M68000 core or peripheral status is lost in this mode. Note: The CLKO signal will remain at the same frequency that is on the EXTAL input.

The following list gives a step-by-step example of how to use the low-power mode. For this example, an interrupt from either timer 1 or timer 2 causes the IMP to exit the low-power mode. This example also assumes an initial operating frequency of 16.67 MHz for the IMP.

1. Set the lower byte of the SCR (location $F7) to $20. This sets the LPEN bit and sets the clock divider to a value of 2 (divide by 2).
2. Disable all interrupts except TIMER1 and TIMER2 in the IMR.
3. Turn off any unneeded peripherals, such as the SCCs, by clearing the ENR and ENT bits. Also turn off any unneeded baud rate generators by setting the EXTC bits in the SCON registers. This procedure can save as much as 4 mA per SCC at 16.67 MHz. (EXTC is cleared by default on power-on reset.)
4. Execute the STOP instruction. The low-power mode is now entered.
5. When a timer 1 or 2 interrupt occurs, the M68000 resumes execution with the timer 1 or 2 interrupt handler. After the RTE instruction, execution continues with the instruction following the STOP instruction in step 4 above. All IMP state information is retained.

3.8.7.2.2 Lowest Power Mode

In this mode, the processor frequency can be further reduced beyond the minimum system frequency limit (e.g., lower than the limit of 8 MHz). In this mode, the LPREC bit must be set to one by the user, causing the M68000 core to be reset as the lowest power mode is exited. The M68000 core is given an internal reset sequence for 16 to 32 clock cycles, and execution resumes with the fetching of the reset vector. The RESET pin does not externally assert during the internal reset sequence. The entire M68000 core status is lost in this mode (A0–A7, D0–D7, PC, SR, etc.); however, the IMP peripheral status is retained (this includes the dual-port RAM, internal registers, BAR, etc.).

The following list gives a step-by-step example of how to use the lowest power mode. For this example, an external wakeup signal is issued to the PB11 pin to exit the lowest power mode.

1. Set the lower byte of the SCR (location $F7) to $FF. This sets the LPREC bit, the LPEN bit, and sets the clock divider to its maximum value (divide by 1024).
2. Disable all interrupts except PB11 in the IMR.
3. Turn off any unneeded peripherals, such as the SCCs, by clearing the ENR and ENT bits. Also turn off any unneeded baud rate generators by setting the EXTC bits in the SCON registers. This procedure can save as much as 4 mA per SCC at 16.67 MHz. (EXTC is cleared by default after reset.)
4. Execute the STOP instruction. Lowest power mode is now entered.
5. A wakeup signal comes from the system to the PB11 pin.
6. The IMP then generates the PB11 interrupt and a reset is automatically generated to the M68000 core.
7. After the IMP is reset, software processing continues from the exception vector table reset vector address. The M68000 is reset, but the rest of the IMP retains its state.

3.8.7.2.3 Lowest Power Mode with External Clock

After the IMP is safely in the lowest power mode the EXTAL frequency can be externally reduced to a lower frequency. In this mode, the clock dividing should not be done in the LPCD bits, but rather externally on the EXTAL pin.

NOTE

The input to EXTAL must be greater than or equal to 25kHz.

The major difference in this mode, is that the entire IMP is now running at a lower clock rate. Any IMP on-chip peripherals and any bus cycles executed by one of the on-chip masters are thus slowed down.

NOTE

The use of external clocks with the SCCs allows the original serial rates to be maintained; however, before attempting this, the SCC performance data should be carefully reviewed (see Ap-

pendix A SCC Performance). Also, the minimum 1:2.5 serial to CLKO clock ratio must be maintained at all times.

The following list gives a step-by-step example of how to achieve the lowest possible power using an external clock. For this example, an external wakeup signal is issued to the PB11 pin to exit the lowest power mode.

1. Set the lower byte of the SCR (location $F7) to $A0. This sets the LPREC bit and the LPEN bits only.
2. Disable all interrupts except PB11 in the IMR.
3. Turn off any unneeded peripherals, such as the SCCs, by clearing the ENR and ENT bits. Also, turn off any unneeded baud rate generators by setting the EXTC bits in the SCON registers. This procedure can save as much as 4 mA per SCC at 16.67 MHz. (EXTC is cleared by default on after reset.)
4. Start off a timer now to toggle a $\overline{\text{TOUT}}$ pin in approximately 20 clocks. Do not wait for this to occur, but continue on to the next step.
5. Execute the STOP instruction. The IMP is now safely in the lowest power mode.
6. Use the toggled $\overline{\text{TOUT}}$ pin to switch the EXTAL clock rate to approximately 50 kHz. Ensure no glitches occur on the EXTAL signal which exceed the maximum clock frequency.
7. Power consumption is now the lowest.
8. A wakeup signal comes from the system.
9. The wakeup signal switches the clock frequency back to the 8–16.67-MHz range and pulls the PB11 pin low. These two events can happen simultaneously.
10. The IMP generates the PB11 interrupt, and a M68000 core reset is generated.
11. After the IMP is reset, software processing continues from the exception vector table reset vector address. The M68000 is reset, but the rest of the IMP retains its state.

The low-power logic uses eight bits in the SCR.

LPCD4–LPCD0—Low-power Clock Divider Selects

The low-power clock divider select bits (LPCD4—LPCD0) specify the divide ratio of the low-power clock divider equal to LPCD4—LPCD0 + 1. The system clock is divided by 2, then divided by the clock divider value (1 to 32). Thus, a divide ratio of 2 to 64 (LPCD4—LPCD0 0 to 31) can be selected. After a system reset, these bits default to zero.

LPEN—Low-power Enable

0 = The low-power modes are disabled.
1 = The low-power modes are enabled.

After a system reset, this bit defaults to zero to disable the low-power modes.

LPP16—Low-power Clock Prescale Divide by 16

0 = The low-power clock divider input clock is the main clock.
1 = The low-power clock divider input clock is the main clock divided by 16. Thus, a divide ratio of 32 to 1024 (LPCD4—LPCD0 0 to 31) can be selected.

After a system reset, this bit defaults to zero.

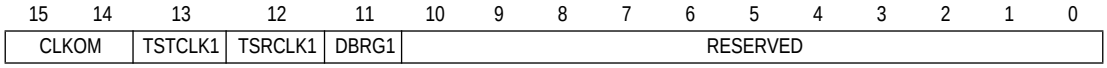
LPREC—Low-Power Recovery

0 = Nondestructive recovery from low power. The processor returns to full frequency and then proceeds using currently held status value. This is called low-power mode.
1 = Destructive recovery from low power. The processor returns to full frequency and then drives RESET for 16 clock cycles. This is called lowest power mode.

After a system reset, the bit defaults to zero.

3.9 CLOCK CONTROL REGISTER

The CKCR is a 16-bit register is a memory-mapped read-write register. The address of this register is fixed at $0FA in supervisor data space (FC = 5). This register controls the state of CLKO, RCLK1, TCLK1, and BRG1. This register is cleared at reset.



CLKOM—CLKO Mode

These bits may be written at any time to change the mode of the CLKO pin. Changes to CLKO are made while the CLKO signal is high. No spikes on CLKO will occur when the CLKOM bits are changed.

00 = The CLKO pin functions normally
01 = The CLKO pin output driver is two thirds its normal strength. Specification 5a at 16.67 MHz is 2 to 14 ns and at 20 MHz is 2 to 11 ns. The output drive derating factor for CLKO in this mode is not specified.
01 = The CLKO pin output driver is one third its normal strength. Specification 5a at 16.67 MHz is 2 to 20ns and at 20 MHz is 2 to 16ns. The output drive derating factor for CLKO in this mode is not specified.
11 = The CLKO pin output is disabled, but is driven high by an internal pullup. Significant power savings can be obtained by disabling CLKO. Typical power savings may range between 2 and 6 mA, depending on the CLKO loading. Disabling CLKO can also reduce noise and electromagnetic interference on the printed circuit board.

TSTCLK1—Three-state TCLK1

0 = Normal operation
1 = The TCLK1 pin is three-stated. This option may be used to prevent contention on the TCLK1 pin if an external clock is provided to the TCLK1 pin while the SCC1 baud rate generator is output on TCLK1. This option may also be chosen if it is required to run the SCC1 baud rate generator at high speed (for instance in a high speed UART application), but the TCLK1 output is not needed, and it is desired to

reduce power. An external pullup should be used if TCLK1 is not driven externally. TSTCLK1 may be toggled at any time, but the SCC1 transmitter should be disabled and re-enabled if any dynamic change is made on TSTCLK1 during the operation of the SCC1 transmitter.

TSRCLK1—Three-state RCLK1

0 = Normal operation

1 = The RCLK1 pin is three-stated. This option may be used to prevent contention on the RCLK1 pin if an external clock is provided to the RCLK1 pin while the SCC1 baud rate generator is output on RCLK1. This option may also be chosen if it is required to run the SCC1 baud rate generator at high speed (for instance in a high speed UART application), but the RCLK1 output is not needed, and it is desired to reduce power. An external pullup should be used if RCLK1 is not driven externally. TSRCLK1 may be toggled at any time, but the SCC1 receiver should be disabled and re-enabled if any dynamic change is made on TSRCLK1 during the operation of the SCC1 receiver.

DBRG1—Disable BRG1

0 = Normal operation

1= The BRG1 pin is disabled and is driven high. This option should be chosen if it is required to run the SCC1 baud rate generator at high speed, but the BRG1 output is not needed and it is desired to reduce power. Although DBRG1 may be modified at any time, the user should note that glitches on BRG1 are not prevented by the MC68302 when the state of DBRG1 is changed.

Bits 10 - 0—Reserved. Should be written with zeros.

3.9.1 Freeze Control

Used to freeze the activity of selected peripherals, $\overline{\text{FRZ}}$ is useful for system debugging purposes. When $\overline{\text{FRZ}}$ is asserted:

- The CP main controller freezes its activity on the next clock (CLKO) and will continue in a frozen state as long as $\overline{\text{FRZ}}$ remains asserted. No new interrupt requests and no memory accesses (internal or external) will occur, and the main controller will not access the serial channels.
- The IDMA completes any bus cycle that is in progress (after $\overline{\text{DTACK}}$ is asserted) and releases bus ownership. No further bus cycles will be started as long as $\overline{\text{FRZ}}$ remains asserted.
- Each timer can be programmed to freeze by setting the appropriate bit in the SCR. After a one-clock (CLKO) delay, the selected timers will freeze their activity (count, capture) as long as $\overline{\text{FRZ}}$ remains asserted.

NOTE

Regardless of whether or not the freeze logic is used, FRZ must be negated during system reset.

FRZ1—Freeze Timer 1 Enable

0 = Freeze timer 1 logic is disabled.
1 = Freeze timer 1 logic is enabled.

After system reset, this bit defaults to zero.

FRZ2—Freeze Timer 2 Enable

0 = Freeze timer 2 logic is disabled.
1 = Freeze timer 2 logic is enabled.

After system reset, this bit defaults to zero.

FRZW—Freeze Watchdog Timer Enable

0 = Freeze watchdog timer logic is disabled.
1 = Freeze watchdog timer logic is enabled.

After system reset, this bit defaults to zero.

No other MC68302 peripherals are directly affected by the freeze logic; however, consequential errors such as receiver overruns in the SCC FIFOs may occur due to the CP main controller being disabled. Note that use of the freeze logic does not clear any IPR bits that were already set.

3.10 DYNAMIC RAM REFRESH CONTROLLER

The communications processor (CP) main (RISC) controller may be configured to handle the dynamic RAM (DRAM) refresh task without any intervention from the M68000 core. Use of this feature requires a timer or SCC baud rate generator (either from the MC68302 or externally), the I/O pin PB8, and two transmit buffer descriptors from SCC2 (Tx BD6 and Tx BD7).

The DRAM refresh controller routine executes in 25 clock cycles. Assuming a refresh cycle every 15.625 μs, two wait state DRAMs, and a 16.67-MHz EXTAL frequency, this routine uses about 10 percent of the microcontroller bandwidth and 4 percent of the M68000 bus bandwidth. The refresh cycle will not be executed during a period that a bus exception (i.e., $\overline{\text{RESET}}$, $\overline{\text{HALT}}$, or $\overline{\text{BERR}}$) is active. The refresh cycle is a standard M68000-type read cycle (an SDMA byte read cycle). It does not generate row address strobe (RAS) and column address strobe (CAS) to the external DRAM. These functions require an external PAL. Use of the DRAM refresh controller will slightly reduce the maximum possible serial data rates of the SCCs.

3.10.1 Hardware Setup

An output of timer 1 or timer 2 (the $\overline{\text{TOUT}}$ pin) or one of the SCC's baud rate generator outputs (BRG3–BRG1) should be connected externally to PB8. A high-to-low transition on this edge causes a request to be generated to the main controller to perform one refresh cycle. The DRAM refresh request takes priority over all SCC channels and commands given to the CP command register.

A block diagram of an MC68302 DRAM system is shown in Figure 3-13. The MC68302 generates standard M68000 read and write cycles that must be converted to DRAM read and write cycles. The address buffers provide the multiplexing of the row and column addresses

to the DRAM bank. The PAL generates the RAS and CAS lines for the DRAM chips and controls the address multiplexing in the external address buffers. One of the MC68000 chip-select lines can be used as the DRAM bank enable signal, if desired.

The refresh operation is a byte read operation. Thus, $\overline{\text{UDS}}$ or $\overline{\text{LDS}}$ will be asserted from the MC68302, but not both. A refresh to an odd address will assert $\overline{\text{LDS}}$; whereas, a refresh to an even address will assert $\overline{\text{UDS}}$.

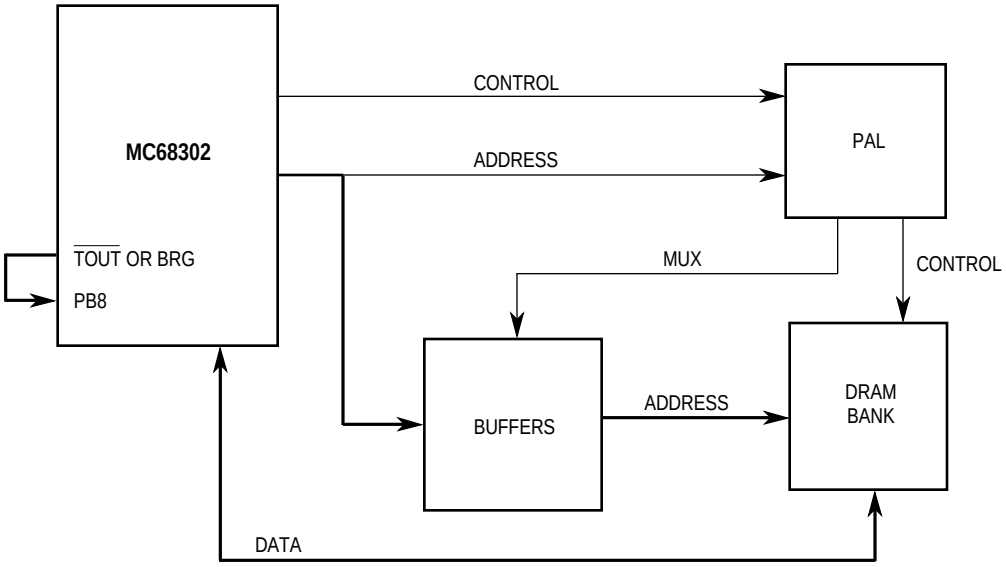


Figure 3-13. DRAM Control Block Diagram

3.10.2 DRAM Refresh Controller Bus Timing

The DRAM refresh controller bus cycles are actually SDMA byte read accesses (see 4.2 SDMA Channels for more details). All timings, signals, and arbitration characteristics of SDMA accesses apply to the DRAM refresh controller accesses. For example, DRAM refresh cycles activate the $\overline{\text{BCLR}}$ signal, just like the SDMA. Note that the function code bits may be used to distinguish DRAM refresh cycles from SDMA cycles, if desired.

A bus error on a DRAM refresh controller access causes the $\overline{\text{BERR}}$ channel number at offset BASE + $67C to be written with a $0001. This is also the value written if the SCC1 receive SDMA channel experiences a bus error; thus, these two sources cannot be distinguished upon a bus error. The DRAM refresh SDMA channel and SCC1 receive SDMA channel are separate and independent in all other respects.

3.10.3 Refresh Request Calculations

A typical 1-Mbyte DRAM needs one refresh cycle every 15.625 µs. The DRAM refresh controller is configured to execute one refresh cycle per request; thus, the PB8 pin should see a high-to-low transition every 15.625 µs. This is once every 260 cycles for a 16.67-MHz clock. Note that one refresh per request minimizes the speed loss on the SCC channels.

3.10.4 Initialization

The user should first initialize the refresh routine parameters in the SCC2 parameter RAM. These parameters are the DRAM low starting address, the DRAM high starting address, the DRAM address increment step (number of bytes in a row), the count (number of rows), and a temporary count. Then, mask the PB8 bit in the IMR (unless an interrupt is desired on each refresh request). Next, the timer or baud rate generator should be programmed to provide the desired refresh clock to the PB8 pin. Next, the ERRE bit in the SCR should be set. Then, upon every high-to-low transition of PB8, the refresh routine executes one refresh (read) cycle.

ERRE—External RISC Request Enable

0 = Normal operation.
1 = When this bit is set, a high-to-low transition on PB8 causes the CP to execute the DRAM refresh routine.

3.10.5 DRAM Refresh Memory Map

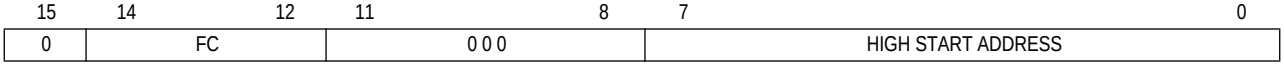
The DRAM refresh memory map replaces the SCC2 TxBD6 and TxBD7 structures in the parameter RAM. The wrap bit must therefore be set in SCC2 TxBD5 so that only six TxBDs are used for SCC2. These parameters should be written before the DRAM refresh controller receives its first request, but may be read at any time. They are undefined at reset.

Table 3-11. DRAM Refresh Memory Map Table

Address	Name	Width	Description
Base + 570 #	DRAM-High	Word	Dynamic RAM High Address and FC
Base + 572 #	DRAM-Low	Word	Dynamic RAM Low Address
Base + 574 #	INCREMENT	Word	Increment Step (number of bytes/row)
Base + 576 #	COUNT	Word	RAM Refresh Cycle Count (number of rows)
Base + 578	T-ptr-H	Word	Temporary Refresh High Address and FC
Base + 57A	T-ptr-L	Word	Temporary Refresh Low Address
Base + 57C #	T-count	Word	Temporary Refresh Cycles Count
Base + 57E	RESERVED	Word	Reserved

Initialized by the user (M68000 core).

DRAM_High—Dynamic RAM High Address and Function Codes



This 16-bit parameter contains the dynamic RAM address space function code output during the refresh cycle and the high eight bits of the dynamic RAM starting address. This parameter should be initialized by the user before activating the refresh routine.

NOTE

The FC bits should not be programmed to the value “111.”

DRAM_Low—Dynamic RAM Low Address

This 16-bit parameter contains the lower 16 bits of the dynamic RAM starting address. This parameter should be initialized by the user before activating the refresh routine.

INCREMENT—Increment Step

This 16-bit parameter contains the number of bytes in a row. The refresh routine will increment its pointer with this parameter value every refresh cycle. This parameter should be initialized by the user before activating the refresh routine.

COUNT—RAM Refresh Cycle Count

This 16-bit parameter contains the number of rows in the DRAM. The refresh routine will execute the COUNT number of refresh cycles before wrapping back to the RAM base address. This parameter should be initialized by the user before activating the refresh routine.

T_ptr_H and T_ptr_L—Temporary Pointer High and Low

These two 16--bit parameters contain the next refresh cycle address and function code to be used by the CP. They correspond to DRAM_High and DRAM_Low, respectively.

T_count—Temporary Count

This 16-bit parameter contains the number of refresh cycles that the DRAM refresh controller must still perform before it will wrap to the beginning of the DRAM. This parameter should be initialized to zero by the user before activating the refresh routine.

3.10.6 Programming Example

An example of programming the DRAM parameters is given for the Motorola MC514256 DRAM. This 1M-bit DRAM is organized in a 256K $\times$ 4 arrangement. There are 512 rows and 512 columns on this device. A bank of 4 of these DRAMs is assumed in this example, giving 512K-bytes of memory. If this bank is placed at location $000000 in the MC68302 address space, its range would then be $0 to $7FFFFF. Assuming a RAS-only refresh technique is used, acceptable parameters would be as follows:

DRAM_High = $0000
DRAM_Low = $0100
INCREMENT = $0002
COUNT = $0200
T_Count = $0000

The value of $0000 in DRAM_High results in the refresh access using a function code of 000. Usually, the function code is not required by the DRAM control logic but may assist in the identification of DRAM refresh accesses during debugging. The starting address is picked to be $000100 (instead of $000000) to avoid refreshing the BAR and SCR registers on the IMP. Depending on the PAL design, an increment value of $0002 can actually refresh a word at a time, even though the refresh access from the MC68302 is a byte read. The COUNT value is the number of word refreshes required in the entire DRAM bank.

SECTION 4
COMMUNICATIONS PROCESSOR (CP)

The CP includes the following modules:

- Main Controller (RISC Processor)
- Six Serial Direct Memory Access (SDMA) Channels
- A Command Set Register
- Serial Channels Physical Interface Including:

  —Motorola Interchip Digital Link (IDL)
  —General Circuit Interface (GCI), also known as IOM-2
  —Pulse Code Modulation (PCM) Highway Interface
  —Nonmultiplexed Serial Interface (NMSI) Implementing Standard
  —Modem Signals
- Three Independent Full Duplex Serial Communication Controllers (SCCs) Supporting the Following Protocols:

  —High-Level/Synchronous Data Link Control (HDLC/SDLC)
  —Universal Asynchronous Receiver Transmitter (UART)
  —Binary Synchronous Communication (BISYNC)
  —Synchronous/Asynchronous Digital Data Communications Message
  —Protocol (DDCMP)
  —Transparent Modes
  —V.110 Rate Adaption
- Serial Communication Port (SCP) for Synchronous Communication
- Two Serial Management Controllers (SMCs) to Support the IDL and GCI Management Channels

4.1 MAIN CONTROLLER

The CP main controller is a RISC processor that services the three SCCs, the SCP, and the SMCs. Its primary responsibilities are to work with the serial channels to implement the user-chosen protocol and to manage the SDMA channels that transfer data between the SCCs and memory. The CP main controller also executes commands issued by the M68000 core (or an external processor) and generates interrupts to the interrupt controller.

The operation of the main controller is transparent to the user, executing microcode located in a private internal ROM (see Figure 4-1). Commands may be explicitly written to the main controller by the M68000 core through the CP command register. Additionally, commands and status are exchanged between the main controller and the M68000 core through the

buffer descriptors of the serial channels. Also, a number of protocol-specific parameters are exchanged through several parameter RAM areas in the internal dual-port RAM.

The RISC controller uses the peripheral bus to communicate with all its peripherals. Each SCC has a separate transmit and receive FIFO. Depending on the protocol chosen, the transmit FIFO is either 3 bytes or 4 words, and the receive FIFO is either 3 bytes or 3 words. Each SCC is configured by parameters written to the dual-port RAM and by SCC hardware registers that are written by the M68000 core (or an external master). The SCC registers that configure each SCC are the SCON, DSR, and SCM. There are three sets of these registers, one for each SCC. The serial channels physical interface is configured by the M68000 core through the SIMODE and SIMASK registers.

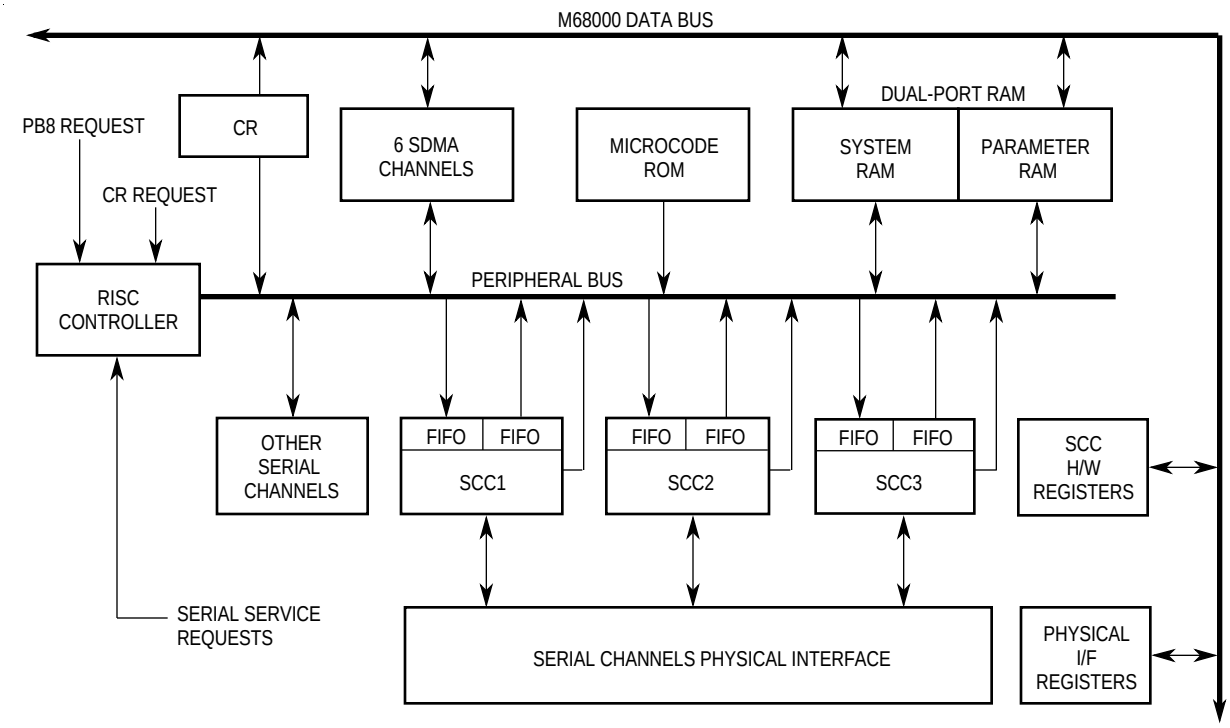


Figure 4-1. Simplified CP Architecture

Simultaneous access of the dual-port RAM by the main controller and the M68000 core (or external processor) is prevented. During a standard four-clock cycle access of the dual-port RAM by the M68000 core, three main controller accesses are permitted. The main controller is delayed one clock cycle, at most, in accessing the dual-port RAM.

The main controller has a priority scheduler that determines which microcode routine is called when more than one internal request is pending. Requests are serviced in the following priority:

1. CP or System Reset
2. SDMA Bus Error

3. DRAM Refresh Controller
4. Commands Issued to the Command Register
5. SCC1 Receive Channel
6. SCC1 Transmit Channel
7. SCC2 Receive Channel
8. SCC2 Transmit Channel
9. SCC3 Receive Channel
10. SCC3 Transmit Channel
11. SMC1 Receive Channel
12. SMC1 Transmit Channel
13. SMC2 Receive Channel
14. SMC2 Transmit Channel
15. SCP Receive Channel
16. SCP Transmit Channel

For details on the DRAM refresh controller, see 3.10 Dynamic Ram Refresh Controller.

4.2 SDMA CHANNELS

Six serial (SDMA) channels are associated with the three full-duplex SCCs. Each channel is permanently assigned to service the receive or transmit operation of one of the SCCs and is always available, regardless of the SCC protocol chosen.

The SDMA channels allow flexibility in managing the data flow. The user can, on a buffer-by-buffer basis, determine whether data should be transferred between the SCCs and external memory or between the SCCs and on-chip dual-port RAM. This choice is controlled in each SCC buffer descriptor. The SCC to external memory path bypasses the dual-port RAM by allowing the SDMA channel to arbitrate for the M68000 bus directly. The SCC to dual-port RAM path saves external memory and eliminates the need to arbitrate for the bus.

Figure 4-2 shows the paths of the data flow. Data from the SCCs may be routed directly to external RAM as shown in path 1. In path 2, data is sent over the peripheral bus to the internal dual-port RAM. The SMCs and SCP, shown in path 3, always route their data to the dual-port RAM since they only receive and transmit a byte at a time.

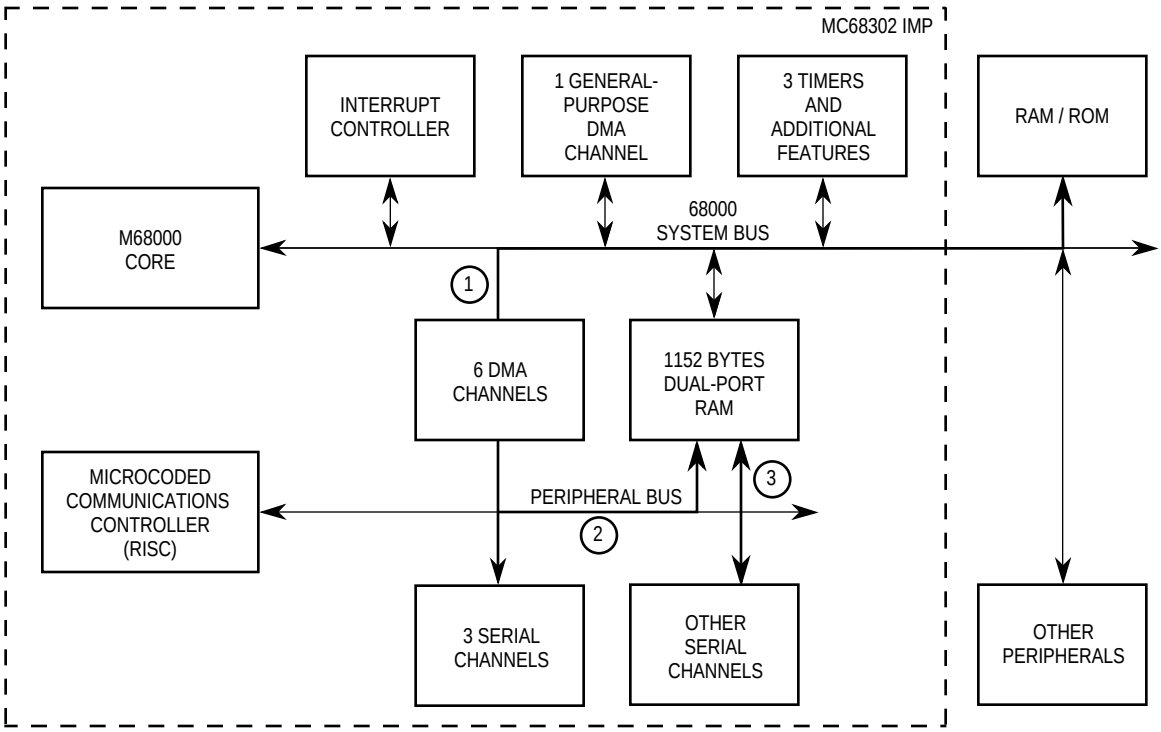


Figure 4-2. Three Serial Data Flow Paths

The SDMA channels implement bus-cycle-stealing data transfers controlled by microcode in the CP main controller. Having no user-accessible registers associated with them, the channels are effectively controlled by the choice of SCC configuration options.

When one SDMA channel needs to transfer data to or from external memory, it will request the M68000 bus with the internal signal SDBR, wait for SDBG, and then only assert the external signal $\overline{\text{BGACK}}$ (see 3.8.5 Bus Arbitration Logic). It remains the bus master for only one bus cycle. The six SDMA channels have priority over the IDMA controller. If the IDMA is bus master when an SDMA channel needs to transfer over the M68000 bus, the SDMA will steal a cycle from the IDMA with no arbitration overhead while $\overline{\text{BGACK}}$ remains continuously low and $\overline{\text{BCLR}}$ remains high. Each SDMA channel may be programmed with a separate function code, if desired. The SDMA channel will read 16 bits at a time. It will write 8 bits at a time except during the HDLC or transparent protocols where it writes 16 bits at a time. Each bus cycle is a standard M68000-type bus cycle. The chip select and wait state generation logic on the MC68302 may be used with the SDMA channels.

NOTE

When external buffer memory is used, the M68000 bus arbitration delay must be less than what would cause the SCC internal FIFOs to overrun or underrun. This aspect is discussed in more detail in 4.5 Serial Communication Controllers (SCCs) and in Appendix A SCC Performance.

The SDMA will assert the external $\overline{\text{BCLR}}$ pin when it requests the bus. $\overline{\text{BCLR}}$ can be used to clear an external bus master from the external bus, if desired. For instance, $\overline{\text{BCLR}}$ can be connected through logic to the external master's $\overline{\text{HALT}}$ signal, and then be negated externally when the external master's AS signal is negated. $\overline{\text{BCLR}}$ as seen from the MC68302 is negated by the SDMA during its access to memory.

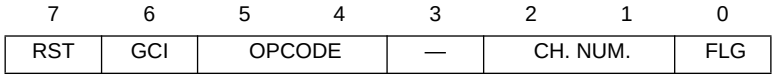
The SDMA keeps the M68000 bus for only one operand (8 or 16 bit) transfer before giving it up. If the SDMA begins a word operation on an 8-bit bus, it will complete that operation before giving up the bus, unless a bus exception such as reset, halt, retry, or bus error occurs. Reset suspends and resets all SDMA activity. Halt suspends activity after the current bus cycle. For information on a bus error during an SDMA access, see 4.5.8.4 Bus Error on SDMA Access.

SDMA operation occurs regardless of the value of the BCLM bit in the SCR, and thus is not affected by the low interrupt latency mechanism.

4.3 COMMAND SET

The M68000 core processor (or an external processor) issues commands to the CP by writing to the CP command register (CR). Only one CR exists on the MC68302. The M68000 core should set the least significant bit (FLG) of the command register when it issues commands. The CP clears FLG after completing the command to indicate to the M68000 core that it is ready for the next command. Subsequent commands to the CR may be given only after FLG is cleared. The software reset (issued with the RST bit) command may be given regardless of the state of FLG, but the M68000 core should still set FLG when setting RST.

The CR, an 8-bit, memory-mapped, read-write register, is cleared by reset.



RST—Software Reset Command

This bit is set by the M68000 core and cleared by the CP. This command is useful when the M68000 core wants to reset the registers and parameters for all channels (SCCs, SCP, SMCs). The main controller in the CP detects this command by hardware, clears the FLG bit within two clocks, and resets the entire CP in approximately 60 clocks. User initialization of the CP registers may begin as soon as the FLG bit is cleared. The CP reset resets the SCCs to the state following a hardware reset, but it does not affect the serial interface (the port A and B registers, the configuration of the SIMODE and SIMASK registers, and the SCON registers). Note that this operation does not clear IPR bits in the interrupt controller.

GCI-OPCODE—GCI Commands and Command Opcodes

0 = When the GCI bit is zero, the commands are as follows:

OPCODE—Command Opcode

These bits are set by the M68000 core to define the specific SCC command. The precise meaning of each command below depends on the protocol chosen.

00 = STOP TRANSMIT Command
01 = RESTART TRANSMIT Command
10 = ENTER HUNT MODE Command
11 = RESET RECEIVER BCS CALCULATION (used only in BISYNC mode)

The detailed command description for the UART protocol is presented in 4.5.11 UART Controller.

The detailed command description for the HDLC protocol is presented in 4.5.12 HDLC Controller.

The detailed command description for the BISYNC protocol is presented in 4.5.13 BI-SYNC Controller.

The detailed command description for the DDCMP protocol is presented in 4.5.14 DDC-MP Controller.

The detailed command description for the V.110 protocol is presented in 4.5.15 V.110 Controller.

The detailed command description for the transparent protocol is presented in 4.5.16 Transparent Controller.

1 = When GCI is set in conjunction with the opcode bits, the two GCI commands (ABORT REQUEST and TIMEOUT) are generated. The accompanying CH. NUM. should be 10, and FLG should be set.

OPCODE—Command Opcode (GCI Mode Only)

These bits are set by the M68000 core to define the specific GCI command. See 4.7 Serial Management Controllers (SMCs) for more details.

00 = TRANSMIT ABORT REQUEST; the GCI receiver sends an abort request on the E bit.
01 = TIMEOUT Command
10 = Reserved
11 = Reserved

Bit 3—Reserved bit; should be set to zero.

CH. NUM.—Channel Number

These bits are set by the M68000 core to define the specific SCC channel that the command is to operate upon.

00 = SCC1
01 = SCC2
10 = SCC3
11 = Reserved

FLG—Command Semaphore Flag

The bit is set by the M68000 core and cleared by the CP.

0 = The CP is ready to receive a new command.

1 = The CR contains a command that the CP is currently processing. The CP clears this bit at the end of command execution. Note that the execution of the STOP TRANSMIT or RESTART TRANSMIT commands may not affect the TXD pin until many clocks after the FLG bit is cleared by the CP due to the transmit FIFO latency.

4.3.1 Command Execution Latency

Commands are executed at a priority higher than the SCCs, but less than the priority of the DRAM refresh controller. The longest command, the ENTER HUNT MODE command, executes in 41 clocks. All other commands execute in less than 20 clocks. The maximum command latency is calculated as follows:

- Command execution time (41 or 20) +
- 25 clocks if DRAM refresh controller is used +

—205 clocks if any SCC is enabled with BISYNC; or
—165 clocks if any SCC is enabled with Transparent; or
—165 clocks if any SCC is enabled with HDLC; or
—150 clocks if any SCC is enabled with UART; or
—140 clocks if any SCC is enabled with DDCMP; else
—0

For example, if HDLC and UART modes are used on the SCCs with the DRAM refresh controller operating, the maximum command latency is 41 + 25 + 165 = 231 clocks = 13 μs at 16.67 MHz. The equations assume that the DRAM refresh cycle occurs once during the command latency. Note that commands are typically given only in special error-handling situations and that the typical latency is much less than the worst case value.

4.4 SERIAL CHANNELS PHYSICAL INTERFACE

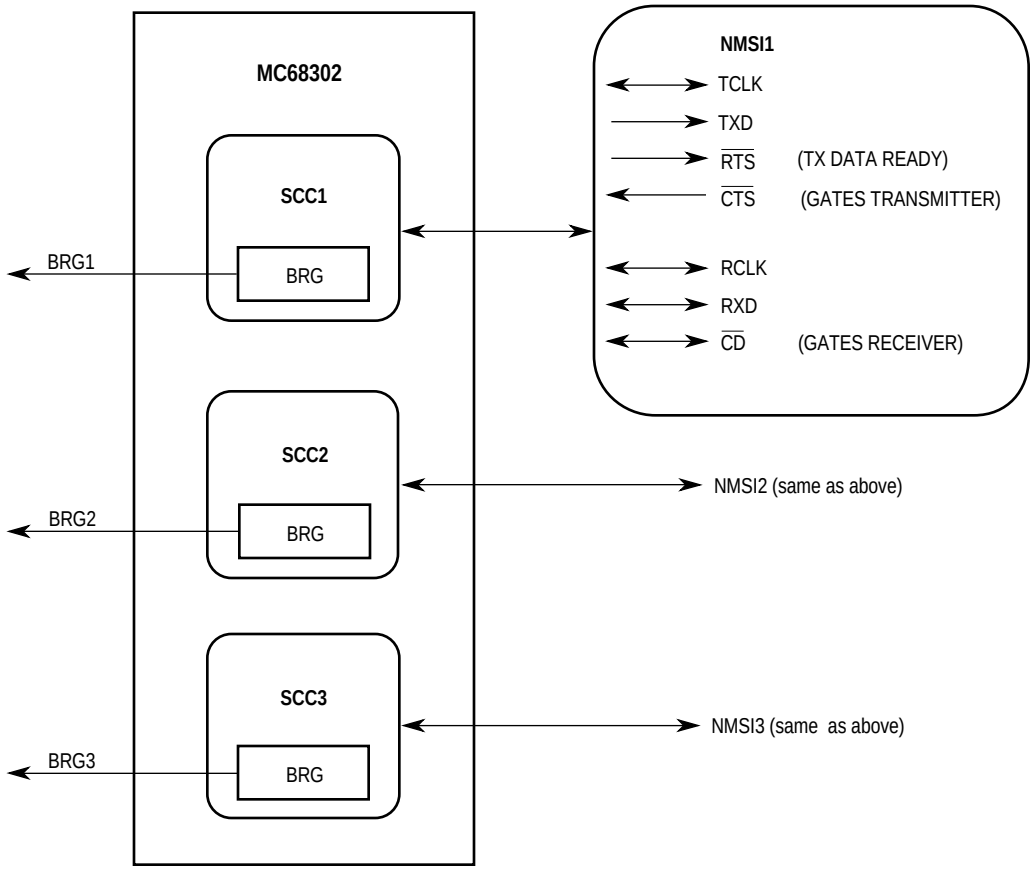
The serial channels physical interface joins the physical layer serial lines to the three SCCs and the two SMCs. (The separate three-wire SCP interface is described in 4.6 Serial Communication Port (SCP).)

The MC68302 supports four different external physical interfaces from the SCCs:

1. NMSI—Nonmultiplexed Serial Interface
2. PCM—Pulse Code Modulation Highway
3. IDL—Interchip Digital Link
4. GCI—General Circuit Interface

The most generic physical interface on the MC68302 is the nonmultiplexed serial interface (NMSI). The NMSI consists of seven of the basic modem (or RS-232) signals: TXD, TCLK, RXD, RCLK, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$. Each SCC can have its own set of NMSI signals as shown in Figure 4-3. In addition to the NMSI, the baud rate generator clocks may be output on separate BRG pins as shown. All NMSI2 pins are multiplexed with parallel I/O pins. The user may choose which NMSI2 pins are used by the SCC2 and which are used as parallel I/O. On NMSI3, the TXD, TCLK, RXD, and RCLK pins are multiplexed with parallel I/O lines;

$\overline{RTS}$, $\overline{CTS}$, and $\overline{CD}$ are multiplexed with the SCP. See 4.6 Serial Communication Port (SCP) for more details on the SCP.



NMSI — Nonmultiplexed serial interface (also called the modem I/F).

Figure 4-3. NMSI Physical Interface

The other three physical interfaces, PCM, IDL, and GCI here are called multiplexed interfaces since they allow data from one, two, or all three SCCs to be time multiplexed together on the same pins. Note that if a multiplexed mode is chosen, the first SCC to use that mode must be SCC1 since the three multiplexed modes share pins with SCC1. After choosing a multiplexed mode, the user may decide whether SCC2 and SCC3 should be part of the multiplexed interface or whether they should have their own set of NMSI pins (see Figure 4-4). If SCC2 or SCC3 is part of the multiplexed interface, all NMSI2 and NMSI3 pins may be used for other functions such as parallel I/O. If a multiplexed mode is chosen, the baud rate generator clock is output on the BRG or TCLK pin, depending on whether the NMSI mode or multiplexed mode, respectively, was chosen for that SCC.

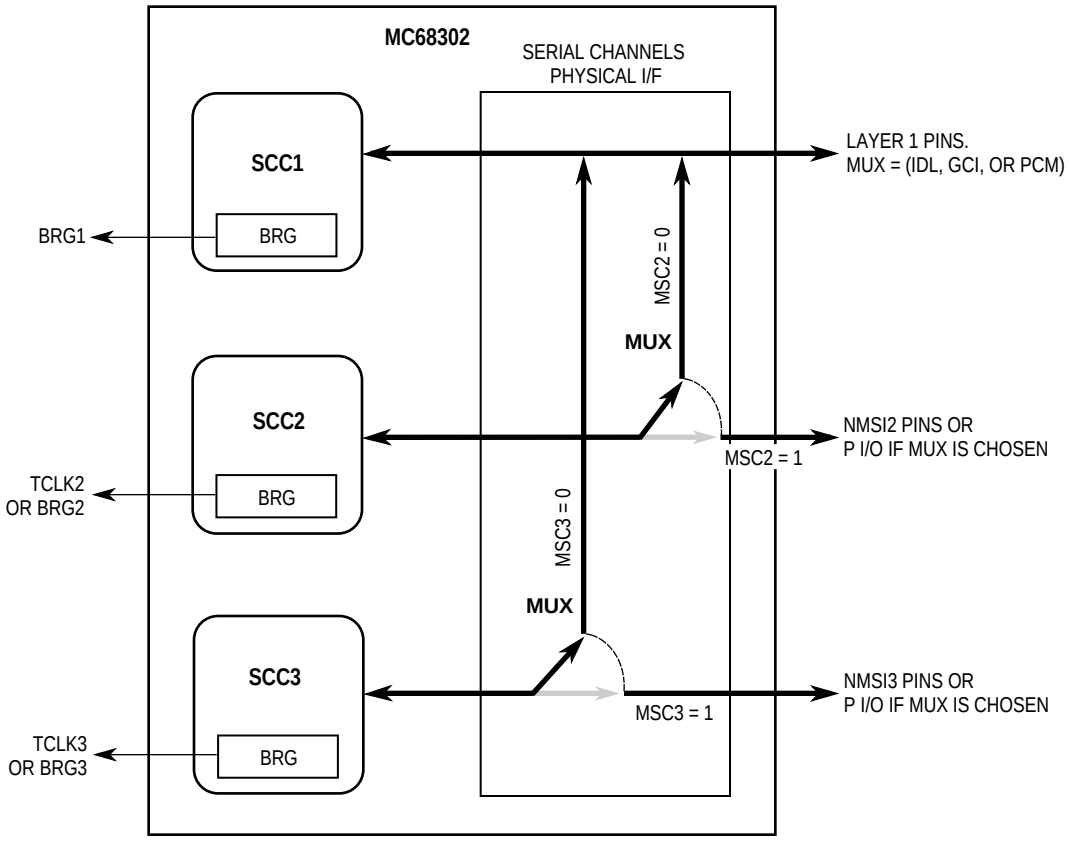


Figure 4-4. Multiplexed Mode on SCC1 Opens Additional Configuration Possibilities

There are five serial channel physical interface combinations for the three SCCs (see Table 4-1).

Table 4-1. The Five Possible SCC Combinations

SCC	1	2	3	4	5
SCC1	NMSI	MUX	MUX	MUX	MUX
SCC2	NMSI	NMSI	MUX	NMSI	MUX
SCC3	NMSI	NMSI	NMSI	MUX	MUX

NOTE: *MUX* is defined as one of the following: IDL, GCI, or PCM highway.

The PCM highway interface is a flexible time-division multiplexed interface. It allows the MC68302 to connect to popular time-slot interfaces such as T1 and CEPT as well as user-defined time-slot interfaces.

The IDL and GCI (IOM-2) interfaces are used to connect to semiconductor devices that support the Integrated Services Digital Network (ISDN). IDL and GCI allow the MC68302 to communicate over any of the 2B + D ISDN basic rate channels.

When using the IDL or GCI buses, additional control functions in the frame structure are required. These functions are supported in the MC68302 through two SMC channels: SMC1 and SMC2. (For other matters relating to the SMCs, refer to 4.7 Serial Management Controllers (SMCs)).

The serial interface also supports two testing modes: echo and loopback. Echo mode provides a return signal from the physical interface by retransmitting the signal it has received. The physical interface echo mode differs from the individual SCC echo mode in that it can operate on the entire multiplexed signal rather than just on a particular SCC channel (which may further have particular bits masked). Loopback mode causes the physical interface to receive the same signal it is transmitting. The physical interface loopback mode checks more than the individual SCC loopback mode; it checks the physical interface and the internal channel routes.

Refer to Figure 4-5 for the serial channels physical interface block diagram.

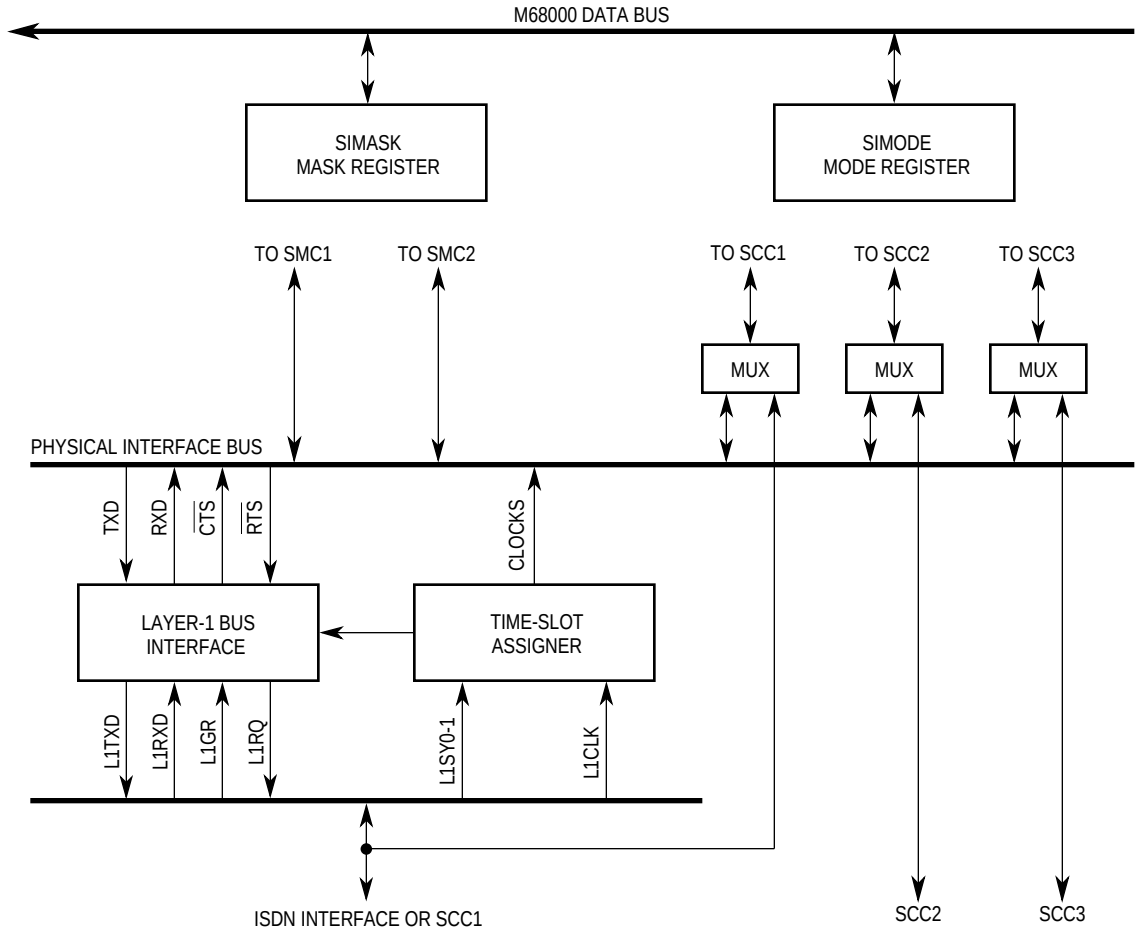


Figure 4-5. Serial Channels Physical Interface Block Diagram

4.4.1 IDL Interface

The IDL interface is a full-duplex ISDN interface used to interconnect a physical layer device (such as the Motorola ISDN S/T transceiver MC145474) to the integrated multiprotocol processor (IMP). Data on five channels (B1, B2, D, A, and M) is transferred in a 20-bit frame every 125 µs, providing 160-kbps full-duplex bandwidth. The IMP is an IDL slave device that is clocked by the IDL bus master (physical layer device). The IMP provides direct connections to the MC145474. Refer to Figure 4-6 for the IDL bus signals.

The IMP supports 10-bit IDL as shown in Figure 4-6; it does not support 8-bit IDL.

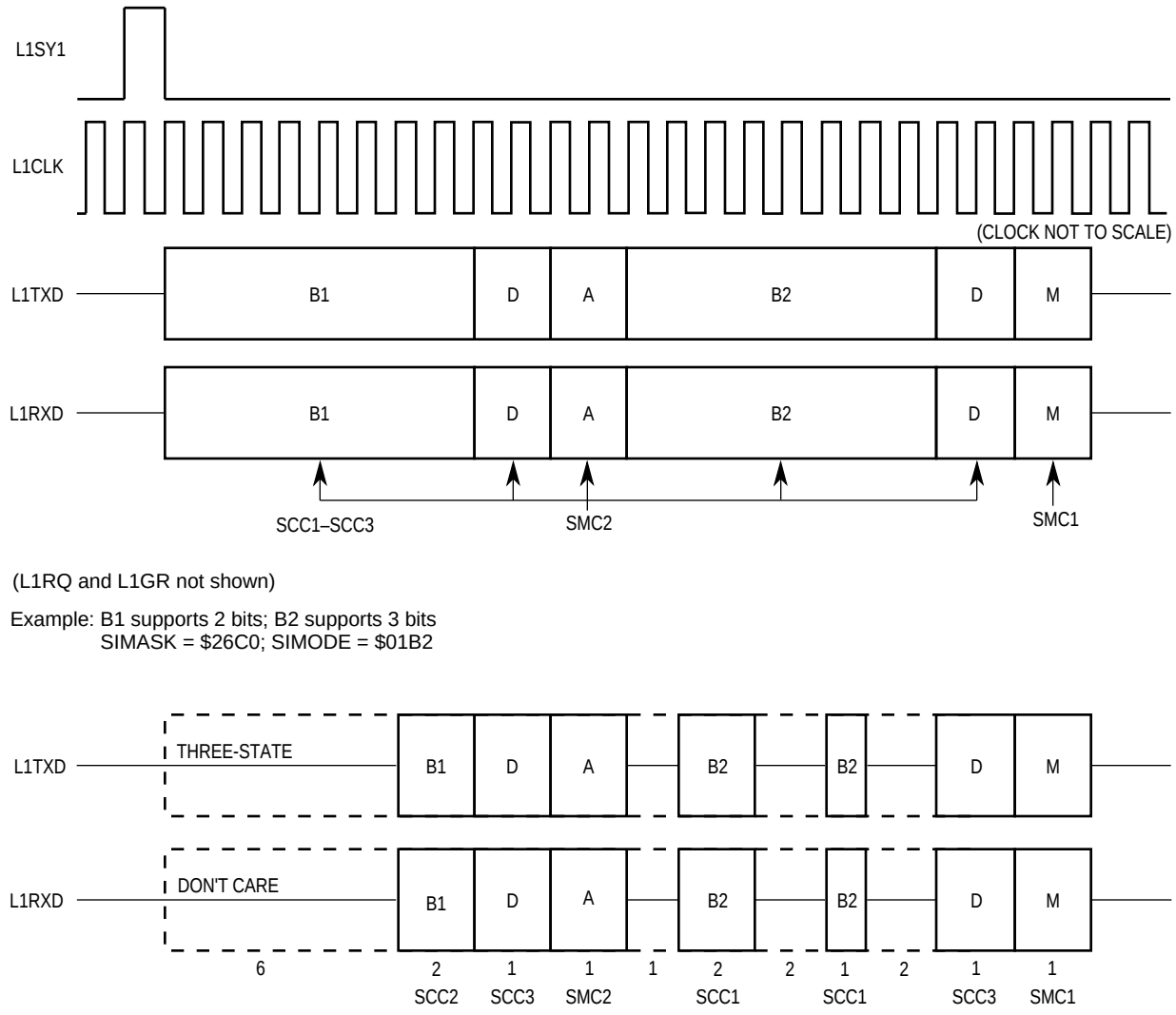


Figure 4-6. IDL Bus Signals

An application of the IDL interface is to build a basic rate ISDN terminal adaptor (see Figure 4-7). In such an application, the IDL interface is used to connect the 2B + D channels between the IMP, CODEC, and S/T transceiver. One of the IMP SCCs would be configured to HDLC mode to handle the D channel; another IMP SCC would be used to rate adapt the

terminal data stream over the B channel. That SCC would be configured for HDLC mode if V.120 rate adaption is required, or for V.110 mode if V.110 rate adaption is required. The second B channel could be routed to the CODEC as a digital voice channel, if desired. The SCP is used to send initialization commands and periodically check status from the S/T transceiver. The SCC connected to the terminal would be configured for UART, BISYNC, or DDCMP mode depending on the terminal protocol used.

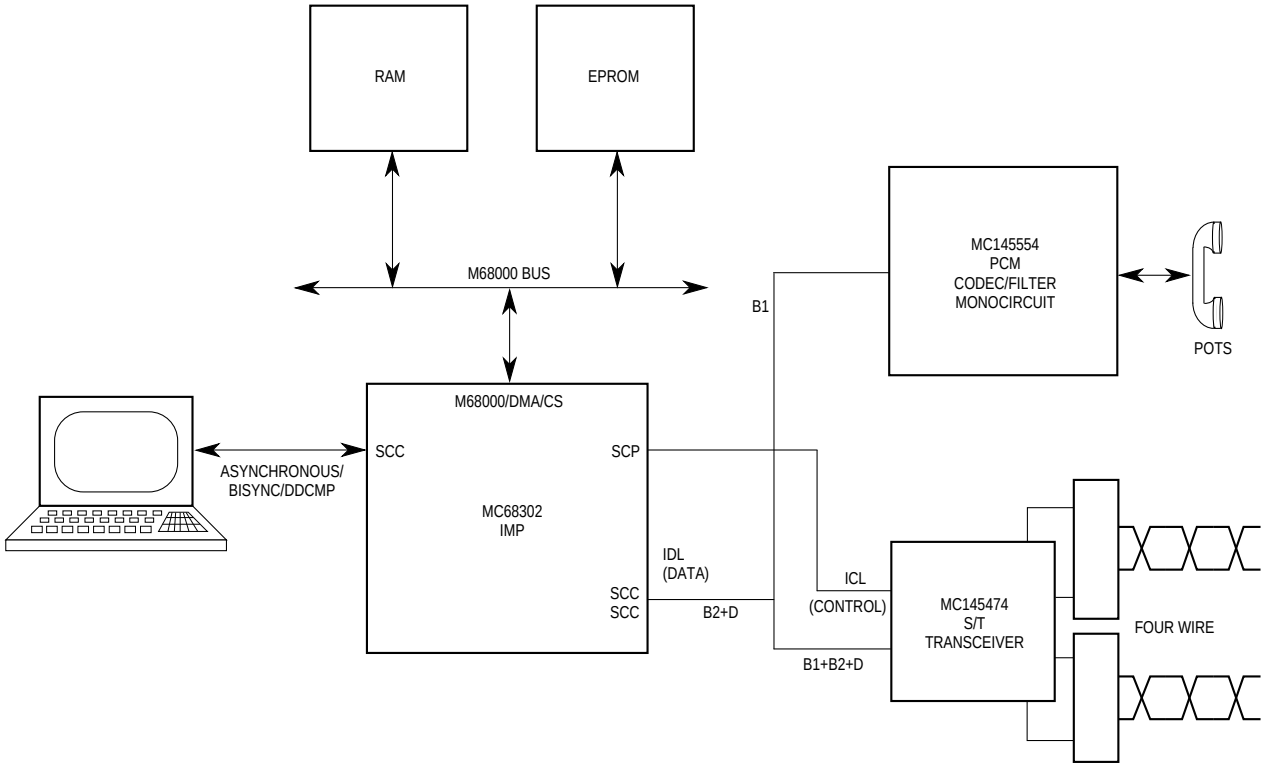


Figure 4-7. IDL Terminal Adaptor

The IMP has two output data strobe lines (SDS1 and SDS2) for selecting either or both the B1 and B2 channels. These signals are used for interfacing devices that do not support the IDL bus. These signals, configured by the SIMASK register, are active only for bits that are not masked. The IDL signals are as follows:

L1CLK	IDL clock; input to the IMP.
L1TXD	IDL transmit data; output from the IMP. Valid only for the bits that are supported by the IDL; three-stated otherwise.
L1RXD	IDL receive data; input to the IMP. Valid for the 20 bits of the IDL; ignored for other signals that may be present.
L1SY1	IDL SYNC signal; input to the IMP. This signal indicates that the 20 clock periods following the pulse designate the IDL frame.
L1RQ	Request permission to transmit on the D channel; output from the IMP.
L1GR	Grant permission to transmit on the D channel; input to the IMP.
SDS1	Serial data strobe 1
SDS2	Serial data strobe 2

NOTE

The IDL bus signals, L1TXD and L1RXD, require pull-up resistors in order to ensure proper operation with transceivers.

In addition to the 144-kbps ISDN 2B + D channels, IDL provides channels for maintenance and auxiliary bandwidth. The IDL bus has five channels:

B1	64-kbps Bearer Channel
B2	64-kbps Bearer Channel
D	16-kbps Signaling Channel
M	8-kbps Maintenance Channel (not required by IDL)
A	8-kbps Auxiliary Channel (not required by IDL)

The IMP supports all five channels of the IDL bus. The following table shows where each channel can be routed. The two B channels can be concatenated and routed to the same SCC channel.

IDL Channel	Serial Controllers
D	SCC1, SCC2, SCC3
B1	SCC1, SCC2, SCC3
B2	SCC1, SCC2, SCC3
M	SMC1
A	SMC2

The IMP supports the request-grant method for contention detection on the D channel. When the IMP has data to transmit on the D channel, it asserts L1RQ. The physical layer device monitors the physical layer bus for activity on the D channel and indicates that the channel is free by asserting L1GR. The IMP samples the L1GR signal when L1SY1 is asserted. If L1GR is high (active), the IMP transmits the first zero of the opening flag in the first bit of the D channel. If a collision is detected on the D channel, the physical layer device negates L1GR. The IMP then stops its transmission and retransmits the frame when L1GR is asserted again. This is handled automatically for the first two buffers of the frame.

The IDL interface supports the CCITT I.460 recommendation for data rate adaptation. The IDL interface can access each bit of the B channel as an 8-kbps channel. A serial interface mask register (SIMASK) for the B channels specifies which bits are supported by the IDL interface. The receiver will support only the bits enabled by SIMASK. The transmitter will transmit only the bits enabled by the mask register and will three-state L1TXD otherwise.

Refer to Figure 4-6 for an example of supporting two bits in the B1 channel and three bits in the B2 channel.

4.4.2 GCI Interface

The normal mode of the GCI (also known as ISDN-Oriented Modular rev 2.2 (IOM2)) ISDN bus is fully supported by the IMP. The IMP also supports channel 0 of the Special Circuit Interface T (SCIT) interface, and in channel 2 of SCIT, supports the D channel access control for S/T interface terminals, using the command/indication (C/I) field. The IMP does not support the Telecom IC (TIC) bus.

The GCI bus consists of four lines: two data lines, a clock, and a frame synchronization line. Usually an 8-kHz frame structure defines the various channels within the 256-kbps data rate as indicated in Figure 4-8. However, the interface can also be used in a multiplexed frame structure on which up to eight physical layer devices multiplex their GCI channels. L1SY1 must provide the channel SYNC. In this mode, the data rate would be 2048 kbps.

The GCI clock rate is twice the data rate. The clock rate for the IMP must not exceed the ratio of 1:2.5 serial clock to parallel clock. Thus, for a 16.67-MHz system clock, the serial clock rate must not exceed 6.67 MHz.

The IMP also supports another line for D-channel access control—the L1GR line. This signal is not part of the GCI interface definition and may be used in proprietary interfaces.

NOTE

When the L1GR line is not used, it should be pulled high. The IMP has two data strobe lines (SDS1 and SDS2) for selecting either or both of the B1 and B2 channels and the data rate clock (L1CLK). These signals are used for interfacing devices that do not support the GCI bus. They are configured with the SIMASK register and are active only for bits that are not masked.

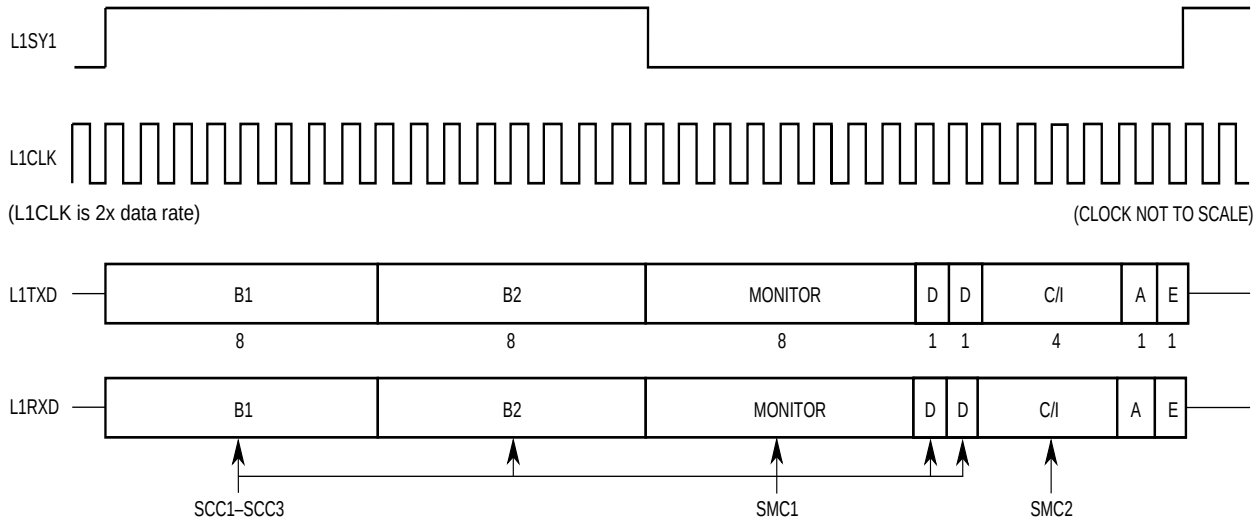


Figure 4-8. GCI Bus Signals

The GCI signals are as follows:

L1CLK	GCI clock; input to the IMP.
L1TXD	GCI transmit data; open drain output.
L1RXD	GCI receive data; input to the IMP.
L1SY1	GCI SYNC signal; input to the IMP.
L1GR	Grant permission to transmit on the D channel; input to the IMP.
SDS1	Serial data strobe 1; output from the IMP.
SDS2	Serial data strobe 2; output from the IMP.
GCIDCL	GCI interface data clock; output from the IMP.

NOTE

The GCI bus signals, L1TXD and L1RXD, require pull-up resistors in order to ensure proper operation with transceivers.

The GCI bus has five channels:

B1	64-kbps Bearer Channel (8 bits)
B2	64-kbps Bearer Channel (8 bits)
M	64-kbps Monitor Channel (8 bits)
D	16-kbps Signaling Channel (2 bits)
C/I, A, E	48-kbps Command/Indication Channel (6 bits)

In addition to the 144-kbps ISDN 2B + D channels, GCI provides two channels for maintenance and control functions.

The monitor channel is used to transfer data between layer-1 devices and the control unit (i.e., the M68000 core). The command/indication channel is used to control activation/deactivation procedures or for the switching of test loops by the control unit.

The IMP supports all five channels of the GCI channel 0. The following table shows where each channel can be routed. The two B channels can be concatenated and routed to the same SCC channel.

GCI Channel 0	Serial Controllers
D	SCC1, SCC2, SCC3
B1	SCC1, SCC2, SCC3
B2	SCC1, SCC2, SCC3
M	SMC1
C/I	SMC2

The GCI interface supports the CCITT I.460 recommendation for data rate adaptation. The GCI interface can access each bit of the B channel as an 8-kbps channel. The mask register (SIMASK) for the B channels specifies which bits are supported by the GCI interface. The receiver will receive only the bits that are enabled by SIMASK; the transmitter will transmit only the bits that are enabled by SIMASK and will not drive the L1TXD pin otherwise (L1TXD in GCI mode is an open-drain output).

The IMP supports contention detection on the D channel. When the IMP has data to transmit on the D channel, it checks bit 4 of the SCIT C/I channel 2. The physical layer device monitors the physical layer bus for activity on the D channel and indicates with this bit that the channel is free. If a collision is detected on the D channel, the physical layer device sets bit 4 of C/I channel 2 to logic high. The IMP then aborts its transmission and retransmits the frame when this bit is asserted again. This procedure is handled automatically for the first two buffers of a frame. The L1GR line may also be used for access to the S interface D channel. This signal is checked by the IMP, and the physical layer device should indicate that the S interface D channel is free by asserting L1GR.

In the deactivated state, the clock pulse is disabled, and the data line is a logic one. The layer-1 device activates the IMP by enabling the clock pulses and by an indication in the channel 0 C/I channel. The IMP will then report to the M68000 core by a maskable interrupt that a valid indication is in the SMC2 receive buffer descriptor.

When the M68000 core activates the line, it sets SETZ in the serial interface mode (SIMODE) register, causing the data output from L1TXD to become a logic zero. Code 0 (command timing TIM) will be transmitted on channel 0 C/I channel to the layer-1 device until the SETZ is reset. The physical layer device will resume transmitting the clock pulses and will give an indication in the channel 0 C/I channel. The M68000 core should reset SETZ to enable data output.

4.4.3 PCM Highway Mode

In PCM highway mode, one, two, or all three SCCs can be multiplexed together to support various time-division multiplexed interfaces. PCM highway supports the standard T1 and CEPT interfaces as well as user-defined interfaces. In this mode, the NMSI1 pins have new names and functions (see Table 4-2).

Table 4-2. PCM Highway Mode Pin Functions

Signal	Definition	Function
L1RXD	Receive Data	Input
L1TXD	Transmit Data	Output
L1CLK	Receive and Transmit Clock	Input
L1SY0	Sync Signal 0	Input
L1SY1	Sync Signal 1	Input
$\overline{\text{RTS1}}$, $\overline{\text{RTS2}}$, $\overline{\text{RTS3}}$	Three Request-to-Send Signals	Outputs

L1CLK is always an input to the MC68302 in PCM highway mode and is used as both a receive and transmit clock. Thus, data is transmitted and received simultaneously in PCM highway mode. (If receive data needs to be clocked into the MC68302 at a different time or speed than transmit data is being clocked out, then NMSI mode should be used instead of PCM highway.)

The two sync signals, L1SY0 and L1SY1, are also inputs to the MC68302. They select one of three PCM channels to which data is routed or select no channel (see Table 4-3).

Table 4-3. PCM Channel Selection

L1SY1	L1SY0	Selection
0	0	No Channel Selected
0	1	PCM Channel 1 Selected
1	0	PCM Channel 2 Selected
1	1	PCM Channel 3 Selected

A PCM channel is not an SCC channel. A PCM channel is an intermediate internal channel that can be routed to any SCC, as selected in the SIMODE register. This extra layer of indirection keeps the hardware (which must generate L1SY1 and L1SY0 signals externally) from having to be modified if a change in the SCC data routing is required.

The routing of each channel is determined in the SIMODE register by the DRB-DRA bits for channel 1, the B1RB–B1RA bits for channel 2, and the B2RB–B2RA bits for channel 3. Once the routing of a PCM channel is selected, data is transmitted from the selected SCC transmitter over the physical interface using the L1CLK pin. At the same time, data is received from the physical interface and routed to the selected SCC receiver. When no sync is asserted, the L1TXD pin is three-stated, and the L1RXD pin is ignored.

Two different methods exist for using the L1SY1–L1SY0 pins: one-clock-prior mode and envelope mode (see Figure 4-9). In one-clock-prior mode, the sync signals should go active for a single clock period prior to an 8-bit time slot. In envelope mode, the sync signals should go active on the first bit of the time slot and stay active the entire time slot. The envelope mode is more general, allowing a time slot to be from one to N bits long.

An example of the use of the L1SY1 and L1SY0 sync signals in the envelope mode is shown in Figure 4-10. The three PCM channels defined in the figure show some of the flexibility available in the PCM highway envelope mode. As shown, PCM channel time slots do not

have to be contiguous in the PCM highway, but rather can be separated by other time slots. Also, PCM channel time slots need not be an even multiple of eight bits in envelope mode. Although not shown in the figure, it is also possible to route multiple PCM channels to a single SCC, causing the SCC to process one higher speed data stream.

The PCM highway interface also supports the $\overline{\text{RTS}}$ signals. They will be asserted (just like in NMSI mode) when an SCC desires to transmit over the PCM highway and will stay asserted until the entire frame is transmitted (regardless of how many time slots that takes). The $\overline{\text{RTS}}$ signal that asserts corresponds to the SCC that desires to transmit. The $\overline{\text{RTS}}$ signals may be useful in debugging but are not required for proper PCM highway operation. If the $\overline{\text{RTS}}$ signals are not needed, they can be ignored or reassigned as parallel I/O.

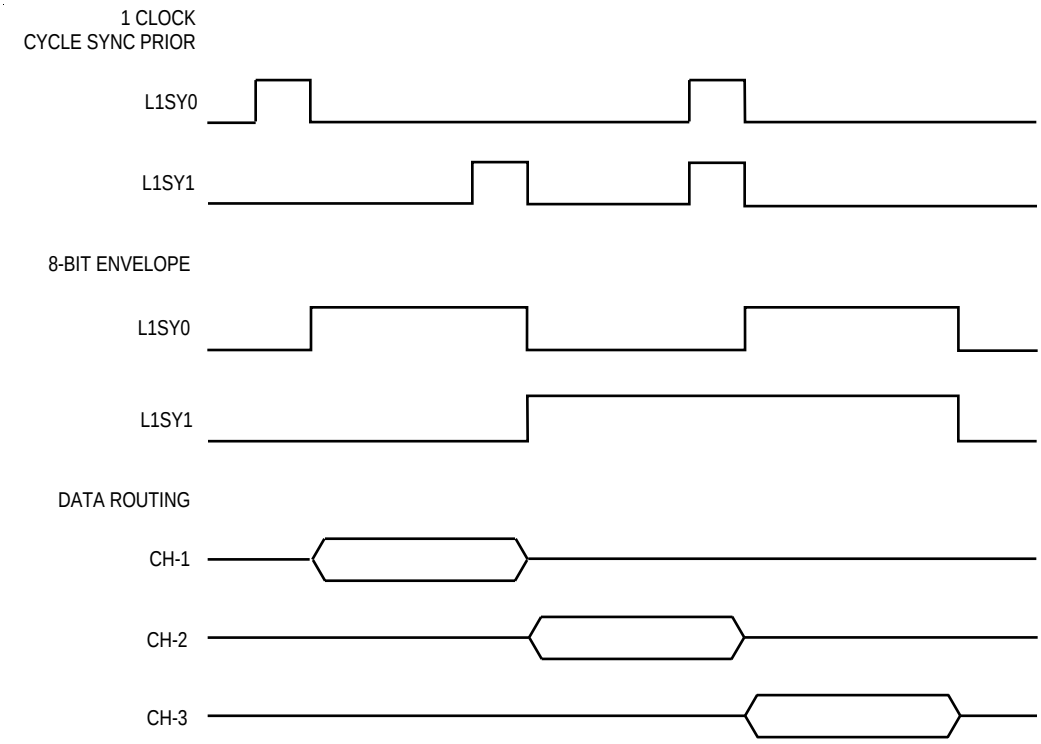
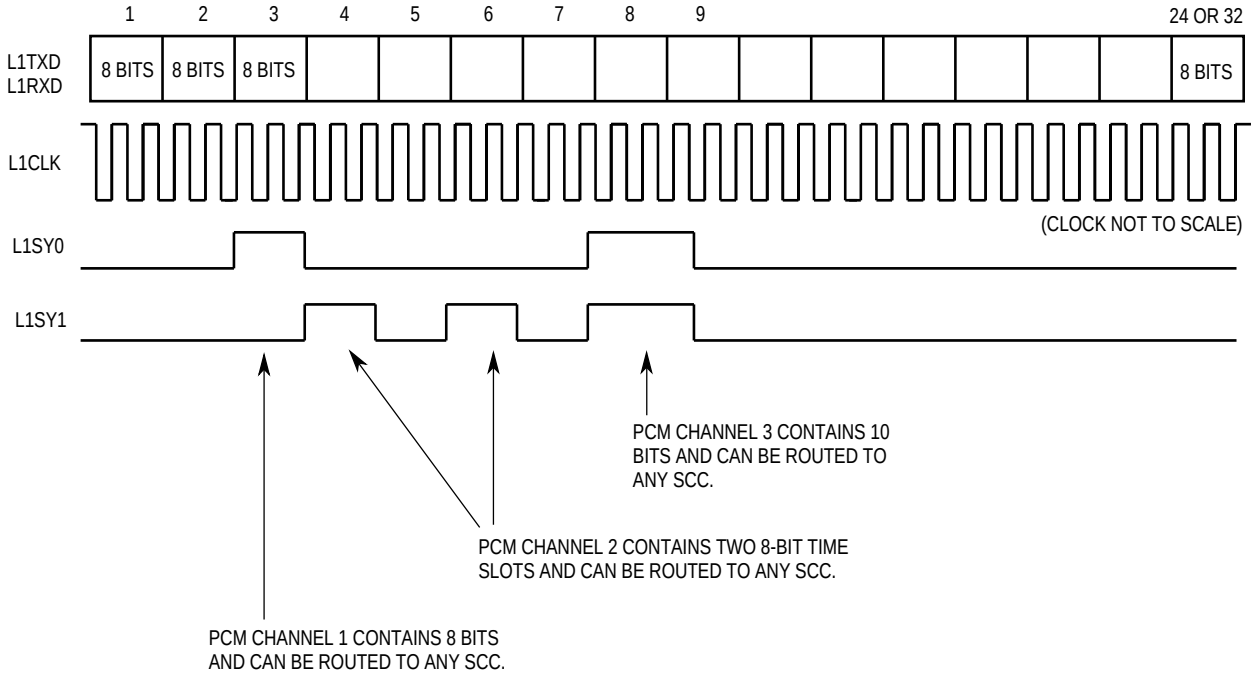


Figure 4-9. Two PCM Sync Methods



NOTE: Whenever the syncs are active, data from that SCC is transmitted and received using L1CLK edges.

Figure 4-10. PCM Channel Assignment on a T1/CEPT Line

4.4.4 Nonmultiplexed Serial Interface (NMSI)

The IMP supports the NMSI with modem signals. In this case, the serial interface connects the seven serial lines of the NMSI1/ISDN interface (RXD1, TXD1, RCLK1, TCLK1, CD1, CTS1, and RTS1) directly to the SCC1 controller. NMSI pins associated with SCC2 and SCC3 can be used as desired or left as general-purpose I/O port pins. See 3.3 Parallel I/O Ports for an example. $\overline{\text{RTS}}$ is an output of the transmitter, while $\overline{\text{CTS}}$ and $\overline{\text{CD}}$ are inputs to the transmitter and receiver, respectively. See 4.5.3 SCC Mode Register (SCM) and 4.4 Serial Channels Physical Interface for additional information.

$\overline{\text{CTS}}$ and $\overline{\text{CD}}$ may be programmed to control transmission and reception automatically or to just generate interrupts.

4.4.5 Serial Interface Registers

There are two serial interface registers: SIMODE and SIMASK. The SIMODE register is a 16-bit register used to define the serial interface operation modes. The SIMASK register is a 16-bit register used to determine which bits are active in the B1 and B2 channels of ISDN.

4.4.5.1 Serial Interface Mode Register (SIMODE)

If the IDL or GCI mode is used, this register allows the user to support any or all of the ISDN channels independently. Any extra SCC channel can then be used for other purposes in

NMSI mode. The SIMODE register is a memory-mapped read-write register cleared by reset.

15	14	13	12	11	10	9	8
SETZ	SYNC/SCIT	SDIAG1	SDIAG0	SDC2	SDC1	B2RB	B2RA

7	6	5	4	3	2	1	0
B1RB	B1RA	DRB	DRA	MSC3	MSC2	MS1	MS0

SETZ—Set L1TXD to zero (valid only for the GCI interface)

0 = Normal operation
1 = L1TXD output set to a logic zero (used in GCI activation, refer to 4.4.2 GCI Interface)

SYNC/SCIT—SYNC Mode/SCIT Select Support

SYNC is valid only in PCM mode.

0 = One pulse wide prior to the 8-bit data
1 = N pulses wide and envelopes the N-bit data

The SCIT (Special Circuit Interface T) interface mode is valid only in GCI mode.

0 = SCIT support disabled
1 = SCIT D-channel collision enabled. Bit 4 of channel 2 C/I used by the IMP for receiving indication on the availability of the S interface D channel.

SDIAG1–SDIAG0—Serial Interface Diagnostic Mode (NMSI1 Pins Only)

00 = Normal operation
01 = Automatic echo
The channel automatically retransmits the received data on a bit-by-bit basis. The receiver operates normally, but the transmitter can only retransmit received data. In this mode, L1GR is ignored.
10 = Internal loopback
The transmitter output (L1TXD) is internally connected to the receiver input (L1RXD). The receiver and the transmitter operate normally. Transmitted data appears on the L1TXD pin, and any external data received on L1RXD pin is ignored. In this mode, L1RQ is asserted normally, and L1GR is ignored.
11 = Loopback control
In this mode, the transmitter output (TXD1/L1TXD) is internally connected to the receiver input (RXD1/L1RXD). The TXD1/L1TXD, TXD2, TXD3, $\overline{\text{RTS1}}$, $\overline{\text{RTS2}}$, and $\overline{\text{RTS3}}$ pins will be high, but L1TXD will be three-stated in IDL and PCM modes. This mode may be used to accomplish multiplex mode loopback testing without affecting the multiplexed layer 1 interface. It also prevents an SCC's individual loopback (configured in the SCM) from affecting the pins of its associated NMSI interface.

SDC2—Serial Data Strobe Control 2

0 = SDS2 signal is asserted during the B2 channel
1 = SDS1 signal is asserted during the B2 channel

SDC1—Serial Data Strobe Control 1

0 = SDS1 signal is asserted during the B1 channel
1 = SDS2 signal is asserted during the B1 channel

B2RB, B2RA—B2 Channel Route in IDL/GCI Mode or CH-3 Route in PCM Mode

00 = Channel not supported
01 = Route channel to SCC1
10 = Route channel to SCC2 (if MSC2 is cleared)
11 = Route channel to SCC3 (if MSC3 is cleared)

B1RB, B1RA—B1 Channel Route in IDL/GCI Mode or CH-2 Route in PCM Mode

00 = Channel not supported
01 = Route channel to SCC1
10 = Route channel to SCC2 (if MSC2 is cleared)
11 = Route channel to SCC3 (if MSC3 is cleared)

DRB, DRA—D-Channel Route in IDL/GCI Mode or CH-1 Route in PCM Mode

00 = Channel not supported
01 = Route channel to SCC1
10 = Route channel to SCC2 (if MSC2 is cleared)
11 = Route channel to SCC3 (if MSC3 is cleared)

MSC3—SCC3 Connection

0 = SCC3 is connected to the multiplexed serial interface (PCM, IDL, or GCI) chosen in MS1–MS0. NMSI3 pins are all available for other purposes.
1 = SCC3 is not connected to a multiplexed serial interface but is connected directly to the NMSI3 pins or SCP pins or is not used. The choice of general-purpose I/O port pins versus SCC3 functions is made in the port A control register. The choice of SCP pins versus SCC3 functions is made in the SPMODE register.

MSC2—SCC2 Connection

0 = SCC2 is connected to the multiplexed serial interface (PCM, IDL, or GCI) chosen in MS1–MS0. NMSI2 pins are all available for other purposes.
1 = SCC2 is not connected to a multiplexed serial interface but is either connected directly to the NMSI2 pins or not used. The choice of general-purpose I/O port pins versus SCC2 functions is made in the port A control register.

MS1—MS0—Mode Supported

00 = NMSI Mode
When working in NMSI mode, SCC1 is connected directly to the seven NMSI1 pins (RXD1, TXD1, RCLK1, TCLK1, $\overline{CD1}$, $\overline{CTS1}$, and $\overline{RTS1}$). SCC2 functions can be routed to port A as NMSI functions or configured instead as PA6–PA0. Four of the SCC3 functions can be routed to port A or retained as PA11–PA8. The other

three SCC3 functions ($\overline{CTS3}$, $\overline{RTS3}$, and $\overline{CD3}$) can be routed to replace the three SCP pins or else not used.
In NMSI mode, the MSC2 and MSC3 bits are ignored. The choice of general-purpose I/O port pins versus SCC2 and SCC3 functions is made in the port A control register. See 3.3 Parallel I/O Ports for an example and more information. The choice of SCP pins versus three SCC3 functions is made in the SPMODE register in the SCP. See 4.6 Serial Communication Port (SCP) for more details.

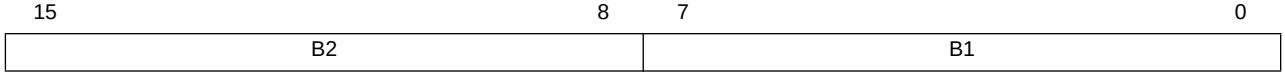
01 = PCM Mode
When working in PCM mode, each of the three multiplexed channels CH-1, CH-2, and CH-3 can be routed independently to each of the three SCCs. This connection is determined by the DRB, DRA, B1RB, B1RA, B2RB, and B2RA bits. SCC2 and SCC3 can be connected directly to their respective NMSI pins (if they are not needed for the PCM channels) as determined by the MSC3–MSC2 bits. In the NMSI case, the choice still exists for port/SCP functions versus SCC functions as described in case 00. The MSC3–MSC2 bits override the PCM routing for a specific SCC.

10 = IDL Mode
When working in IDL/GCI mode, each ISDN channel (D, B1, and B2) can be routed independently to each of the three SCCs. This connection is determined by the DRB, DRA, B1RB, B1RA, B2RB, and B2RA bits. SCC2 and SCC3 can be connected directly to their respective NMSI pins (if they are not needed for ISDN channels) determined by the MSC3–MSC2 bits. In the NMSI case, the choice still exists for port/SCP functions versus SCC functions as described in case 00. Note that the MSC3–MSC2 bits override the ISDN connection for a specific SCC.

11 = GCI Interface
Refer to the IDL mode description.

4.4.5.2 Serial Interface Mask Register (SIMASK)

The SIMASK register, a memory-mapped read-write register, is set to all ones by reset. SIMASK is used in IDL and GCI to determine which bits are active in the B1 and B2 channels. Any combination of bits may be chosen. A bit set to zero is not used by the IMP. A bit set to one signifies that the corresponding B channel bit is used for transmission and reception on the B channel. Note that the serial data strobes, SD1 and SD2, are asserted for the entire 8-bit time slot independent of the setting of the bits in the SIMASK register.



NOTE

Bit 0 of this register is the first bit transmitted or received on the IDL/GCI B1 channel.

4.5 SERIAL COMMUNICATION CONTROLLERS (SCCS)

The IMP contains three independent SCCs, each of which can implement different protocols. This configuration provides the user with options for controlling up to three independent full-duplex lines implementing bridges or gateway functions or multiplexing up to three SCCs onto the same physical layer interface to implement a 2B + D ISDN basic rate channel or

three channels of a PCM highway. Each protocol-type implementation uses identical buffer structures to simplify programming.

The following protocols are supported: HDLC/SDLC, BISYNC, synchronous and asynchronous DDCMP, UART, several transparent modes, and V.110 rate adaption support. Each protocol can be implemented with IDL, GCI, PCM, or NMSI physical layer interfaces (see 4.4 Serial Channels Physical Interface) and can be configured to operate in either echo or loopback mode. Echo mode provides a return signal from an SCC by retransmitting the received signal. Loopback mode is a local feedback connection allowing an SCC to receive the signal it is transmitting. (Echo and loopback mode for multiplexed interfaces are discussed in 4.4 Serial Channels Physical Interface).

The receive and transmit section of each SCC is supported with one of the six dedicated SDMA channels (see 4.2 SDMA Channels). These channels transfer data between the SCCs and either external RAM or on-chip dual-port RAM. This function is transparent to the user, being enabled and controlled according to the configuration of each SCC channel. Each SCC can be clocked by either an external source (with the clock pins RCLK or TCLK) or by an internal source through a baud rate generator for each SCC channel. The baud rate generator can derive its clock from the main IMP clock or from a separate input clock. The SCC transmitter and receiver sections are independent and may be clocked at different rates.

The SCCs exhibit two types of performance limitations. The first type is a hardware clocking limit, which is the same for each SCC. The SCC clocks must not exceed a ratio of 1:2.5 serial clock (RCLK or TCLK) to parallel clock (EXTAL). Thus, for a 16.67-MHz system clock frequency, the serial clock must not exceed 6.67 MHz. The second type concerns the system data rate. The SDMA channels and CP main controller must have enough time to service the SCCs, thus preventing FIFO underruns and overruns in the SCCs. This requirement depends on a number of factors discussed in more detail in Appendix A SCC Performance.

Each SCC supports the standard seven-line modem interface (also referred to as NMSI) with the signals RXD, TXD, RCLK, TCLK, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$. Other modem signals (such as DSR and DTR) may be supported through the parallel I/O pins. A block diagram of the SCC is depicted in Figure 4-11.

To provide extra modem serial output lines, the user must define I/O port A or B pins as outputs in the port A/B data direction register and write to the port A/B data register to cause the state of the pin to change. Extra serial input lines with interrupts may be supported by defining the port B pins as inputs in the port B data direction register. When a change in the state of the pin occurs, the interrupt handler may assert or negate the extra outputs to support the hand-shaking protocol. (See 3.3 Parallel I/O Ports for related details.)

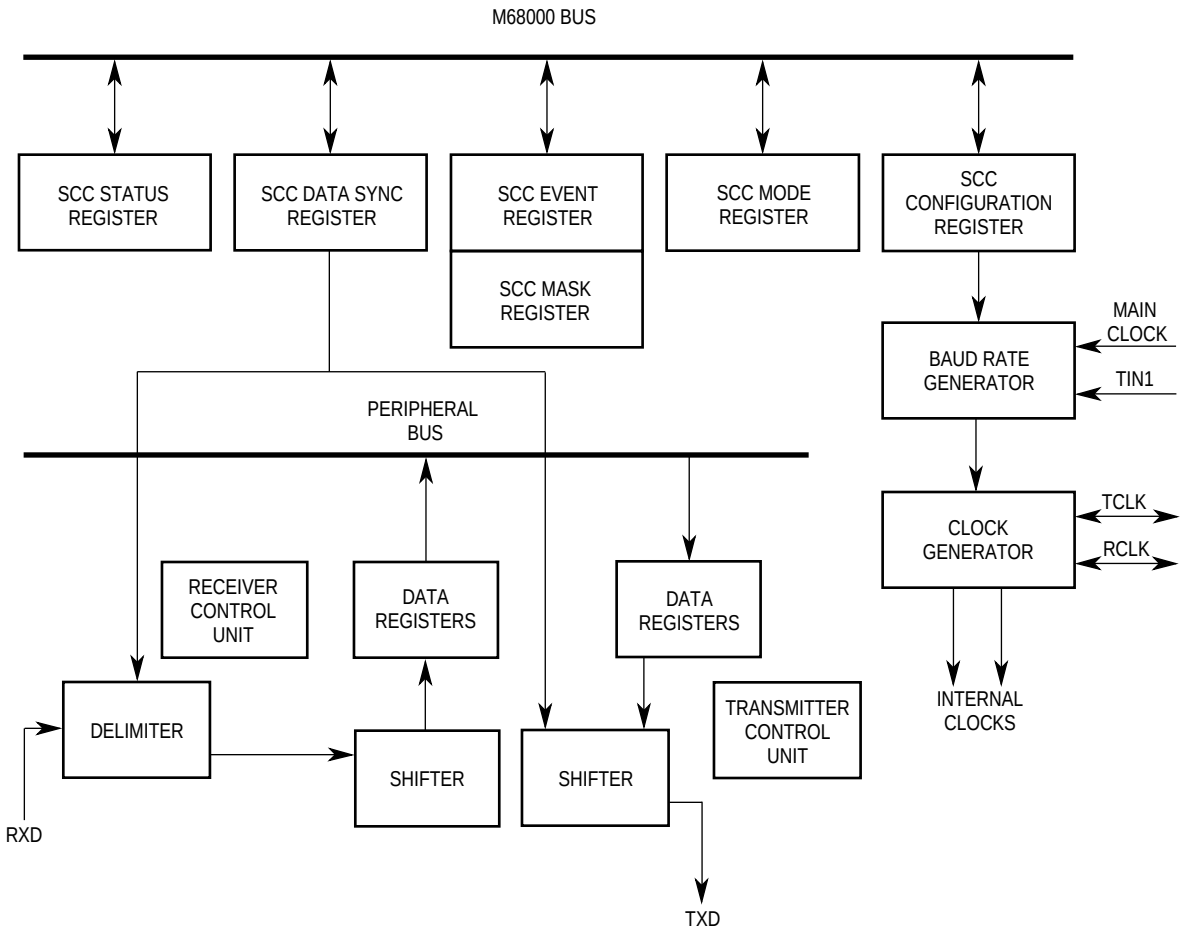


Figure 4-11. SCC Block Diagram

4.5.1 SCC Features

Each SCC channel has the following features:

- HDLC/SDLC, BISYNC, DDCMP, UART, Transparent, or V.110 Protocols
- Programmable Baud Rate Generator Driven by Main Clock or an External Clock
- Data Clocked by the Baud Rate Generator or Directly by an External Pin
- Supports Modem Signals (RXD, TXD, RCLK, TCLK, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$, and $\overline{\text{CD}}$)
- Full-Duplex Operation
- Echo Mode
- Local Loopback Mode
- Baud Rate Generator Outputs Available Externally

4.5.2 SCC Configuration Register (SCON)

Each SCC controller has a configuration register that controls its operation and selects its clock source and baud rate. Figure 4-12 shows one of the three SCC baud rate generators.

Each SCON is a 16-bit, memory-mapped, read-write register. The SCONs are set to $0004 by reset, resulting in the baud rate generator output clock rate being set to the main clock rate divided by 3. The baud rate generator output clock is always available externally, as shown in Table 5-8.

NOTE

The BRG output are 180 degrees out of phase to the TCLK and RCLK signals used by the SCC and output on the RCLK and TCLK pins.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WOMS	EXTC	TCS	RCS	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0	DIV4

WOMS—Wired-OR

When WOMS is set, the TXD driver is programmed to function as an open-drain output and may be externally wired together with other TXD pins in an appropriate bus configuration. In this case, an external pullup resistor is required. When WOMS is cleared, the TXD pin operates normally with an active internal pullup.

NOTE

This bit is valid only in NMSI mode.

EXTC—External Clock

The EXTC bit selects whether the baud rate generator input clock source is the internal main clock (EXTC = 0) or external clock (EXTC = 1). If EXTC = 1, the external clock is taken from the TIN1 pin. Note that the single TIN1 pin can be used to supply a clock for all three baud rate generators.

TCS—Transmit Clock Source

The TCS bit selects either the baud rate generator output (TCS = 0) or the TCLK pin (TCS = 1) for the transmitter clock. If TCS = 0, then the baud rate generator output is driven onto the TCLK pin. This bit should be programmed to one if a multiplexed mode is chosen for the SCC.

After system reset, SCC hardware causes TCLK to default to an input and stay an input until a zero is written to TCS. For SCC2 and SCC3, TCLK can be derived directly from the RCLK pin as shown in Table 3-6.

RCS—Receive Clock Source

The RCS bit selects either the baud rate generator output (RCS = 0) or the RCLK pin (RCS = 1) for the receiver clock. If RCS = 0, then the baud rate generator output is driven onto the RCLK pin. This bit should be programmed to one if a multiplexed mode is chosen for the SCC.

After system reset, SCC hardware causes the RCLK to default to an input and stay an input until a zero is written to RCS.

CD10–CD0—Clock Divider

The clock divider bits and the prescaler determine the baud rate generator output clock rate. CD10–CD0 are used to preset an 11-bit counter that is decremented at the prescaler output rate. The counter is not otherwise accessible to the user. When the counter reaches zero, it is reloaded with the clock divider bits. Thus, a value of $7FF in CD10–CD0 produces the minimum clock rate (divide by 2048); a value of $000 produces the maximum clock rate (divide by 1).

NOTE

Because of SCC clocking restrictions, the maximum baud rate that may be used to clock an SCC is divide by 3.

When dividing by an odd number, the counter ensures a 50% duty cycle by asserting the terminal count once on a clock high and next on a clock low. The terminal count signals the counter expiration and toggles the clock.

DIV4—SCC Clock Prescaler Divide by 4

The SCC clock prescaler bit selects a divide-by-1 (DIV4 = 0) or divide-by-4 (DIV4 = 1) prescaler for the clock divider input. The divide-by-4 option is useful in generating very slow baud rates.

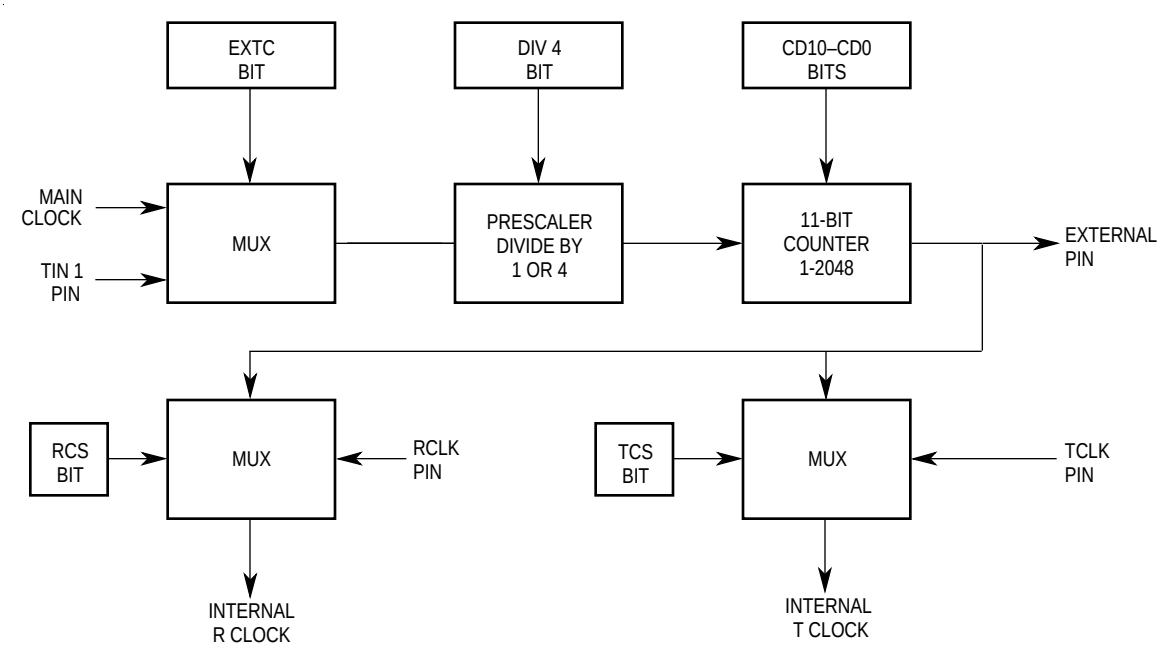


Figure 4-12. SCC Baud Rate Generator

4.5.2.1 Asynchronous Baud Rate Generator Examples

The UART circuitry always uses a clock that is 16x the baud rate. The ratio of the 16x UART clock to the system parallel clock must not exceed 1:2.5. For an internally supplied clock, an integer divider value must be used; therefore, the divider must be 3 or greater. Thus, using a clock divider value of 3 (programmed as 2 in the SCON) and a 16.67-MHz crystal gives a UART clock rate of 5.56 MHz and a baud rate of 347 kbaud. Assuming again a 16.67-MHz

crystal, an externally supplied UART clock on the TCLK or RCLK pins can be as high as 6.67 MHz, giving a maximum baud rate of 417 kbaud.

The baud rate using the baud rate generator is (System Clock or TIN1 clock)/(1 or 4)/(Clock Divider + 1)/16. The baud rate using the baud rate generator with an externally supplied clock to the TCLK or RCLK pins is always (TCLK or RCLK)/16.

Table 4-4 shows examples of typical bit rates of asynchronous communication and how to obtain them with the baud rate generator using an internally supplied clock.

Table 4-4. Typical Bit Rates of Asynchronous Communication

Baud Rates	15.36			16.0			16.667		
	DIV4	DIV	Actual Frequency	DIV4	DIV	Actual Frequency	DIV4	DIV	Actual Frequency
150	1	1599	150	1	1666	149.97	1	1735	150.01
300	1	799	300	1	832	300.12	1	867	300.02
600	0	1599	600	0	1666	599.88	0	1735	600.05
1200	0	799	1200	0	832	1200.48	0	867	1200.1
2400	0	399	2400	0	416	2398.08	0	433	2400.2
4800	0	199	4800	0	207	4807.69	0	216	4800.4
9600	0	99	9600	0	103	9615.34	0	108	9556.76
19200	0	49	19200	0	51	19230.8	0	53	19290.5
38400	0	24	38400	0	25	38461.53	0	26	38581.0

4.5.2.2 Synchronous Baud Rate Generator Examples

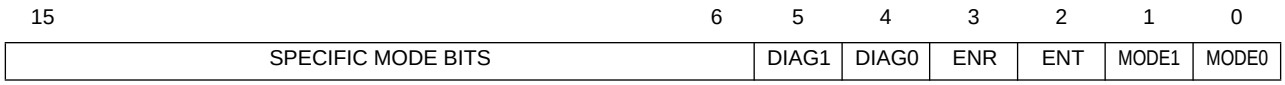
For synchronous communication (HDLC/SDLC, BISYNC, DDCMP, Transparent, and V.110), the internal clock is identical to the baud rate output. To obtain the desired rate, the user selects the appropriate system clock according to the following equation:

Baud rate = (System Clock or TIN1 Clock)/(Clock Divider + 1)/(1 or 4) according to the DIV4 bit

For example, to get the data rate of 64 kbps, the system clock can be 15.36 MHz, DIV4 = 0, and the Clock Divider = 239. Of course, a 64 kbps rate provided externally on the TCLK or RCLK pins could also be used.

4.5.3 SCC Mode Register (SCM)

Each SCC has a mode register. The functions of bits 5–0 are common to each protocol. The function of the specific mode bits varies according to the protocol selected by the MODE1–MODE0 bits. They are described in the relevant sections for each protocol type. Each SCM is a 16-bit, memory-mapped, read-write register. The SCMs are cleared by reset.



DIAG1–DIAG0—Diagnostic Mode

00 = Normal operation ($\overline{CTS}$, $\overline{CD}$ lines under automatic control)
In this mode, the CTS and CD lines are monitored by the SCC controller. The SCC controller uses these lines to automatically enable/disable reception and transmission.

If $\overline{RTS}$ is programmed to be asserted by the SCC, it will be asserted once buffered data is loaded into the transmit FIFO and a falling TCLK edge occurs. The following table shows the transmit data delays.

Table 4-5. Transmit Data Delay (TCLK Periods)

Protocol Type	From RTS Low	From CTS Low
Asynchronous Protocols (16x clock) Synchronous Protocols (1x clock)	0 1	48 3.5

NOTES:
1. $\overline{RTS}$ low values assume $\overline{CTS}$ is already asserted when $\overline{RTS}$ is asserted.
2. $\overline{CTS}$ low values assume $\overline{CTS}$ met the asynchronous setup time; otherwise, an additional clock may be added.

$\overline{RTS}$ is negated by the SCC one clock after the last bit in the frame. Figure 4-13 shows a diagram of synchronous mode timing from $\overline{RTS}$ low. Figure 4-14 shows a diagram of synchronous mode timing delays from $\overline{CTS}$ low.

The SCC samples $\overline{CTS}$ on the every rising edge of the TCLK. If $\overline{CTS}$ is negated when $\overline{RTS}$ is asserted, a CTS lost error occurs. If a synchronous protocol is used, the transmit data will be aborted after four additional bits are transmitted. If an asynchronous protocol is used, the transmit data will be aborted after three additional bits are transmitted. See the transmit error section of each protocol for further details and steps to be taken following a CTS lost error.

The SCC latches its first bit of valid receive data on the same clock edge (rising RCLK) that samples $\overline{CD}$ as low. The only exception is when the EXSYN bit is set in the SCC mode register for the BISYNC and Transparent protocols.

If $\overline{CD}$ is negated during frame reception, a CD lost error occurs and the SCC will quit receiving data within four additional bit times. At this point, any residue of bits less than 8 bits (or 16 bits in HDLC or transparent modes) will be discarded and not written to memory. Thus, the last bit written to memory will be within plus or minus four bit times from the point at which $\overline{CD}$ was negated.

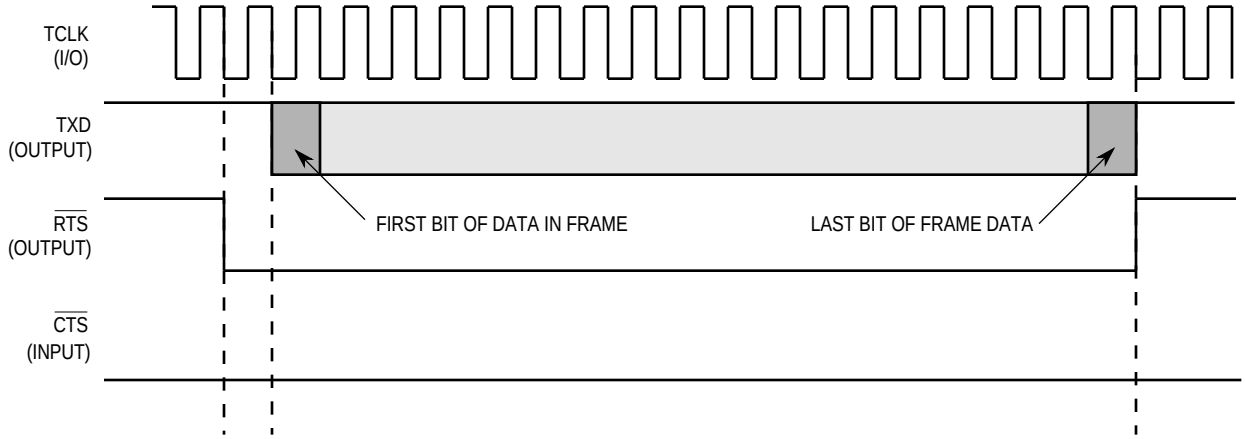
NOTE

The CTS lost error and CD lost error (with $\overline{CTS}$ and $\overline{CD}$ under automatic control) is not intended to implement a flow control method in the UART protocol. The software operation of the DIAG1–DIAG0 bits should be chosen if UART flow control is desired, with transmission being temporarily suspended by the FRZ bit in the UART event register. CTS lost and CD lost, as defined here, are intended to implement the aborting of transmission and reception as defined in many synchronous protocols.

01 = Loopback mode

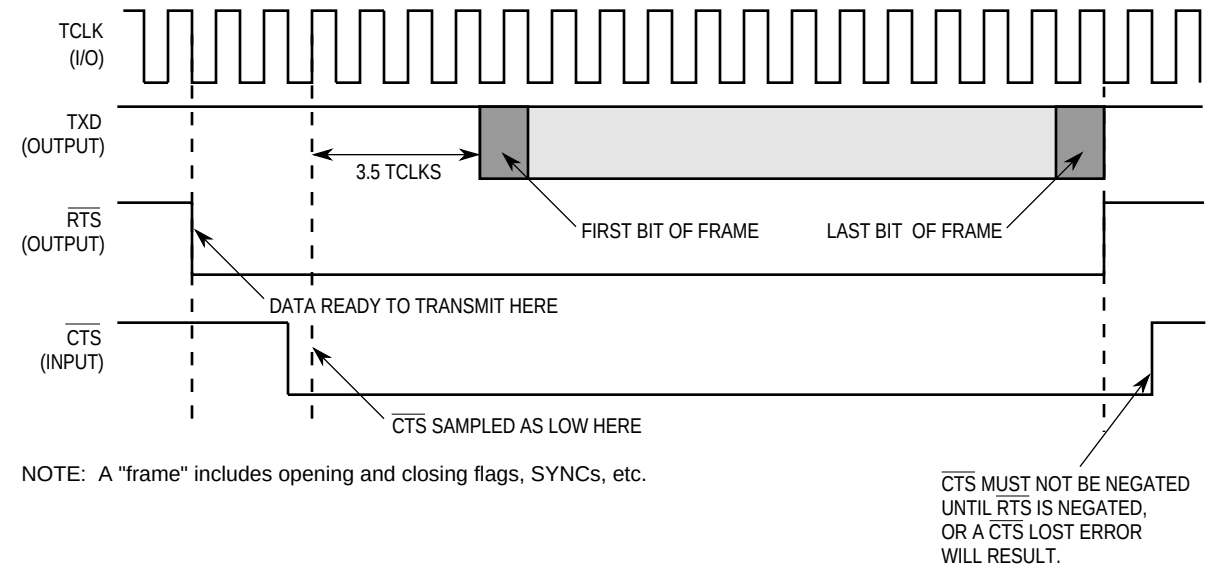
In this mode, the transmitter output is internally connected to the receiver input while the receiver and the transmitter operate normally. The value on the RXD pin is ignored. For the NMSI2 and NMSI3 pins, the TXD pin may be programmed to either show the transmitted data or not show the data by programming port A par-

allel I/O lines in the PACNT register. To cause the TXD and $\overline{RTS}$ pins to simply remain high in NMSI1, NMSI2, and NMSI3 modes, use this loopback mode in conjunction with setting the SDIAG1–SDIAG0 bits in the SIMODE register to loopback control.



NOTE: A "frame" includes opening and closing flags in HDLC and SYNCs in BISYNC and DDCMP.

Figure 4-13. Output Delays from RTS Low, Synchronous Protocol



NOTE: A "frame" includes opening and closing flags, SYNCs, etc.

Figure 4-14. Output Delays from $\overline{CTS}$ Low, Synchronous Protocol

If an internal loopback is desired when this SCC is configured to a multiplexed physical interface, then only the SDIAG1–SDIAG0 bits need be set.
When using loopback mode, the clock source for the transmitter and the receiver (as set in the TCS and RCS bits in the SCON register), must be the same. Thus,

for an internal clock, TCS and RCS may both be zero, or, for an external clock, they may both be one. The other two combinations are not allowed in this mode.

NOTE

If external loopback is desired (i.e., external to the MC68302), then the DIAG1–DIAG0 bits should be set for either normal or software operation, and an external connection should be made between the TXD and RXD pins. Clocks may be generated internally, externally, or an internally generated TCLK may be externally connected to RCLK. If software operation is used, the $\overline{\text{RTS}}$, $\overline{\text{CD}}$, and $\overline{\text{CTS}}$ pins need not be externally connected. If normal operation is used, the $\overline{\text{RTS}}$ pin may be externally connected to the $\overline{\text{CD}}$ pin, and the $\overline{\text{CTS}}$ pin may be grounded.

NOTE

Do not use this mode for loopback operation of IDL in the Serial Interface. Instead program the diag bits to Normal Operation, and (1) assert the L1GR pin externally from the S/T chip, or (2) configure the SDIAG1-0 bits in the SIMODE to Internal Loopback or Loopback Control.

10 = Automatic echo

In this mode, the channel automatically retransmits the received data on a bit-by-bit basis. The receiver operates normally, but the transmitter simply retransmits the received data. The $\overline{\text{CD}}$ pin must be asserted for the receiver to receive data, and the $\overline{\text{CTS}}$ line is ignored. The data is echoed out the TXD pin with a few nanosecond delay from RXD. No transmit clock is required, and the ENT bit in the SCC mode register does not have to be set.

NOTE

The echo function may also be accomplished in software by receiving buffers from an SCC, linking them to transmit buffer descriptors, and then transmitting them back out of that SCC.

11 = Software operation (CTS, CD lines under software control)

In this mode, the CTS and CD lines are just inputs to the SCC event (SCCE)and status (SCCS) registers. The SCC controller does not use these lines to enable/disable reception and transmission, but leaves low (i.e., active) in this mode. Transmission delays from RTS low are zero TCLKs (asynchronous protocols) or one TCLK (synchronous protocols).

NOTE

The MC68302 provides several tools for enabling and disabling transmission and/or reception. Choosing the right tool is application and situation dependent. For the receiver, the tools are 1) the empty bit in the receive buffer descriptor, 2) the ENR bit, and 3) the ENTER HUNT MODE command. For the transmitter, the

tools are 1) the ready bit in the transmit buffer descriptor, 2) the ENT bit, 3) the STOP TRANSMIT command, 4) the RESTART TRANSMIT command, and 5) the FRZ bit in the SCM (UART mode only).

ENR—Enable Receiver

When ENR is set, the receiver is enabled. When it is cleared, the receiver is disabled, and any data in the receive FIFO is lost. If ENR is cleared during data reception, the receiver aborts the current character. ENR may be set or cleared regardless of whether serial clocks are present. To restart reception, the ENTER HUNT MODE command should be issued before ENR is set again.

ENT—Enable Transmitter

When ENT is set, the transmitter is enabled; when ENT is cleared, the transmitter is disabled. If ENT is cleared, the transmitter will abort any data transmission, clear the transmit data FIFO and shift register, and force the TXD line high (idle). Data already in the transmit shift register will not be transmitted. ENT may be set or cleared regardless of whether serial clocks are present.

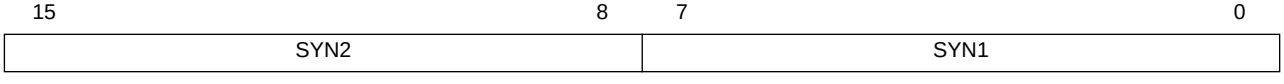
The STOP TRANSMIT command additionally aborts the current frame and would normally be given to the channel before clearing ENT. The command does not clear ENT automatically. In a similar manner, to restart transmission, the user should issue the RESTART TRANSMIT command and then set ENT. The command register is described in 4.3 Command Set. The specific actions taken with each command vary somewhat according to protocol and are discussed in each protocol section.

MODE1–MODE0—Channel Mode

00 = HDLC
01 = Asynchronous (UART and DDCMP)
10 = Synchronous DDCMP and V.110
11 = BISYNC and Promiscuous Transparent

4.5.4 SCC Data Synchronization Register (DSR)

Each DSR is a 16-bit, memory-mapped, read-write register. DSR specifies the pattern used in the frame synchronization procedure of the SCC in the synchronous protocols. In the UART protocol it is used to configure fractional stop bit transmission. After reset, the DSR defaults to $7E7E (two FLAGs); thus, no additional programming is necessary for the HDLC protocol. For BISYNC, DDCMP, and V.110, the contents of the DSR should be written before the channel is enabled. Note that for the DDCMP, SYN1 must equal SYN2 must equal DSYN1 for proper operation.



NOTE

The DSR register has no relationship to the RS-232 signal “data set ready,” which is also abbreviated DSR.

4.5.5 Buffer Descriptors Table

Data associated with each SCC channel is stored in buffers. Each buffer is referenced by a buffer descriptor (BD). BDs are located in each channel's BD table (located in dual-port RAM). There are two such tables for each SCC channel: one is used for data received from the serial line; the other is used to transmit data. The actual buffers may reside in either external memory or internal memory (dual-port RAM). For internal memory data buffers, the data buffer pointer is in the low-order data pointer word and is an offset from the device base address to any available area in the dual-port RAM. (Data buffers may reside in the parameter RAM of an SCC if it is not enabled).

The BD table allows the user to define up to eight buffers for the transmit channel and up to eight buffers for the receive channel (Figure 4-15). Each BD table forms a circular queue. The format of the BDs is the same for each SCC mode of operation (HDLC, UART, DDCMP, BISYNC, V.110, and transparent) and for both transmit or receive. Only the first field (containing status and control bits) differs for each protocol. The BD format is shown in Figure 4-16.

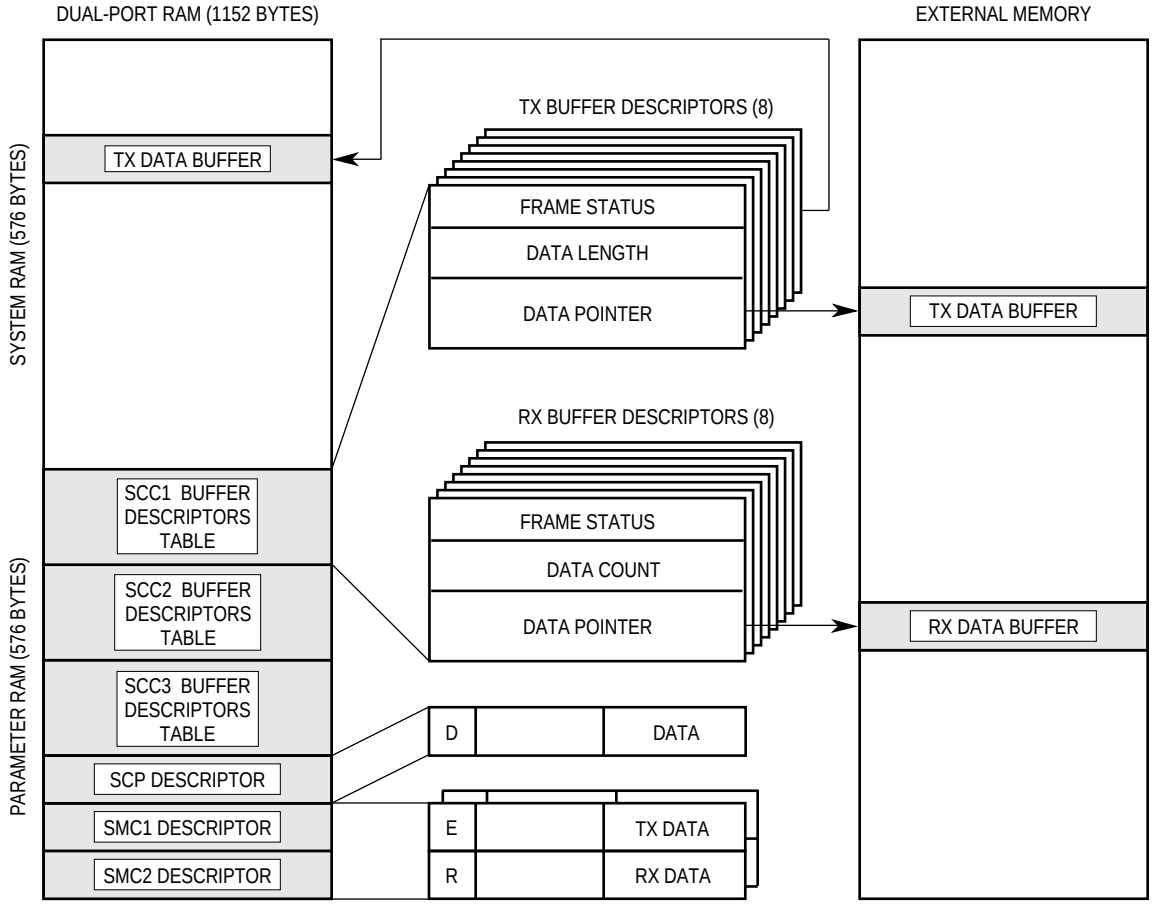


Figure 4-15. Memory Structure

	15	0
OFFSET + 0	STATUS AND CONTROL	
OFFSET + 2	DATA LENGTH	
OFFSET + 4	HIGH-ORDER DATA BUFFER POINTER (only lower 8 bits used, upper 8 bits must be 0)	
OFFSET + 6	LOW-ORDER DATA BUFFER POINTER	

Figure 4-16. SCC Buffer Descriptor Format

For frame-oriented protocols (HDLC, BISYNC, DDCMP, V.110), a frame may reside in as many buffers as are necessary (transmit or receive). Each buffer has a maximum length of 64K–1 bytes. The CP does not assume that all buffers of a single frame are currently linked to the BD table, but does assume that the unlinked buffers will be provided by the processor in time to be either transmitted or received. Failure to do so will result in a TXE error being reported by the CP.

For example, assume the first six buffers of the transmit BD table have been transmitted and await processing by the M68000 core (with all eight buffers used in the circular queue), and a three-buffer frame awaits transmission. The first two buffers may be linked to the remaining two entries in the table as long as the user links the final buffer into the first entry in the BD table before the IMP attempts its transmission. If the final buffer is not linked in time to the BD table by the time the CP attempts its transmission, the CP will report an underrun error.

Buffers allocated to an SCC channel may be located in either internal or external memory. Memory allocation occurs for each BD individually. If internal memory is selected, the CP uses only the lower 11 address bits (A10–A0) as an offset to the internal dual-port RAM. Accesses to the internal memory by the CP are one clock cycle long and occur without arbitration. If external memory is selected, the pointers to the data buffers are used by the CP as 24 bits of address.

Extra caution should be used if function codes are included in the decoding of the external buffer address (e.g., in the on-chip chip select logic). The function code of this SCC channel must be set before external buffers can be accessed; it can then be changed only when the user is sure that the CP is not currently accessing external buffers for that channel. There are six separate function code registers located in the parameter RAM for the three SCC channels: three for receive data buffers (RFCR) and three for transmit data buffers (TFCR).

NOTE

The RFCR and TFCR function codes should never be initialized to “111.”

The CP processes the transmit BDs in a straightforward fashion. Once the transmit side of an SCC is enabled, it starts with the first BD in that SCC's transmit BD table, periodically checking a bit to see if that BD is "ready". Once it is ready, it will process that BD, reading a word at a time from its associated buffer, doing certain required protocol processing on the data, and moving resultant data to the SCC transmit FIFO. When the first buffer has been processed, the CP moves on to the next BD, again waiting for that BD's “ready” bit to be set. Thus, the CP does no look-ahead BD processing, nor does it skip over BDs that are not ready. When the CP sees the “wrap” bit set in a BD, it goes back to the beginning of the BD

table, after processing of this BD is complete. After using a BD, the CP sets the “ready” bit to not-ready; thus, the CP will never use a BD twice until the BD has been confirmed by the M68000 core.

The CP uses the receive BDs in a similar fashion. Once the receive side of an SCC is enabled, it starts with the first BD in that SCC's receive BD table. Once data arrives from the serial line into the SCC, the CP performs certain required protocol processing on the data and moves the resultant data (either bytes or words at a time depending on the protocol) to the buffer pointed to by the first BD. Use of a BD is complete when there is no more room left in the buffer or when certain events occur, such as detection of an error or an end-of-frame. Whatever the reason, the buffer is then said to be “closed,” and additional data will be stored using the next BD. Whenever the CP needs to begin using a BD because new data is arriving, it will check the “empty” bit of that BD. If the current BD is not empty, it will report a” busy” error. However, it will not move from the current BD until it becomes empty. When the CP sees the “wrap” bit set in a BD, it goes back to the beginning of the BD table, after use of this BD is complete. After using a BD, the CP sets the “empty” bit to not-empty; thus, the CP will never use a BD twice until the BD has been “processed” by the M68000 core.

In general, each SCC has eight transmit BDs and eight receive BDs. However, it is possible in one special case to assign up to 16 receive BDs at the expense of all transmit BDs. Since the transmit BDs directly follow the receive BDs in the memory map for each SCC, if an SCC is configured exclusively for half-duplex reception, it is possible to have up to 16 receive BDs available for that SCC.

If the DRAM refresh unit is used, SCC2 has six transmit BDs rather than the normal eight. SCC3 normally only has four transmit BDs. However, it is actually possible to regain additional Tx BDs for SCC3 as follows. The Tx BD table may be extended by two BDs to six BDs if the SMCs are not used. Additionally, all eight Tx BDs for SCC3 may be used if the following is considered: 1) the SCP and SMCs must not be used; 2) various words within the last two BDs will be changed by the CP during the initialization routine following any reset; and 3) the BERR channel number value will be written into the last BD after any SDMA bus error (see 4.5.8.4 Bus Error on SDMA Access), but this is not a major concern since the CP must be reset after any SDMA bus error.

4.5.6 SCC Parameter RAM Memory Map

Each SCC maintains a section in the dual-port RAM called the parameter RAM. Each SCC parameter RAM area begins at offset $80 from each SCC base area ($400, $500, or $600) and continues through offset $BF. Refer to Table 2-8 for the placement of the three SCC parameter RAM areas. Part of each SCC parameter RAM (offset $80–$9A), which is identical for each protocol chosen, is shown in Table 4-6. Offsets $9C–$BF comprise the protocol-specific portion of the SCC parameter RAM and are discussed relative to the particular protocol chosen.

Table 4-6. SCC Parameter RAM Memory Map

Address	Name	Width	Description
SCC Base + 80 #	RFCR	Byte	Rx Function Code
SCC Base + 81 #	TFCR	Byte	Tx Function Code
SCC Base + 82 #	MRBLR	Word	Maximum Rx Buffer Length
SCC Base + 84 ##		Word	Rx Internal State
SCC Base + 86 ##		Byte	Reserved
SCC Base + 87 ##	RBD#	Byte	Rx Internal Buffer Number
SCC Base + 88		2 Words	Rx Internal Data Pointer
SCC Base + 8C		Word	Rx Internal Byte Count
SCC Base + 8E		Word	Rx Temp
SCC Base + 90 ##		Word	Tx Internal State
SCC Base + 92 ##		Byte	Reserved
SCC Base + 93 ##	TBD#	Byte	Tx Internal Buffer Number
SCC Base + 94		2 Words	Tx Internal Data Pointer
SCC Base + 98		Word	Tx Internal Byte Count
SCC Base + 9A		Word	Tx Temp
SCC Base + 9C SCC Base + BF			First Word of Protocol-Specific Area Last Word of Protocol-Specific Area

Initialized by the user (M68000 core).

Modified by the CP following a CP or system reset.

Certain parameter RAM values need to be initialized by the user before the SCC is enabled. Those values not so designated are initialized/written by the CP. Once initialized, most parameter RAM values will not need to be accessed in user software since most of the activity is centered around the transmit and receive buffer descriptors, not the parameter RAM. However, if the parameter RAM is accessed by the user, the following should be noted. The parameter RAM can be read at any time. The parameter RAM values related to the SCC transmitted can only be written 1) whenever the ENT bit in the SCM is zero or 2) after a STOP TRANSMIT command and before a RESTART TRANSMIT command. The parameter RAM values related to the SCC receiver can only be written 1) whenever the ENR bit in the SCM is zero or 2) if the receiver has previously been enabled, after the ENTER HUNT MODE command and before the ENR bit is set. See 4.5.10 Disabling the SCCs for a discussion of when the SCC registers may be changed.

The registers (see Table 4-6) that typically need to be accessed by the user are described in the following paragraphs.

4.5.6.1 Data Buffer Function Code Register (TFCR, RFCR)

This register defines the address space of the receive (RFCR) and transmit (TFCR) data buffers. These registers must be initialized if the SCC is used.

NOTE

The value of the function code register for any channel may be equal to that of any other, but do not initialize FC2–FC0 with the value “111” which causes a conflict with the interrupt acknowledge cycle to occur.

7	6	5	4	3	2	1	0
0	FC2	FC1	FC0	0	0	0	0

4.5.6.2 Maximum Receive Buffer Length Register (MRBLR)

Each SCC has one MRBLR that is used to define the receive buffer length for that SCC. The MRBLR defines the maximum number of bytes that the IMP will write to a receive buffer on that SCC before moving to the next buffer. The IMP may write fewer bytes to the buffer than MRBLR if a condition such as an error or end of frame occurs, but it will never write more bytes than the MRBLR value. Thus, buffers supplied by the user for use by the IMP should always be of size MRBLR (or greater) in length.

The transmit buffers for an SCC are not affected in any way by the value programmed into MRBLR. Transmit buffers may be individually chosen to have varying lengths, as needed. The number of bytes to be transmitted is chosen by programming the data length field in the Tx BD.

NOTE

MRBLR was not intended to be changed dynamically while an SCC is operating. However, if it is modified in a single bus cycle with one 16-bit move (NOT two 8-bit back-to-back bus cycles), then a dynamic change in receive buffer length can be successfully achieved, which occurs when the CP moves control to the next Rx BD in the table. Thus, a change to MRBLR will not have an immediate effect. To guarantee the exact Rx BD on which the change will occur, the user should change MRBLR only while the SCC receiver is disabled (see 4.5.6 SCC Parameter RAM Memory Map).

NOTE

The MRBLR value should be greater than zero in all modes. In the HDLC and transparent modes, the MRBLR should have an even value.

4.5.6.3 Receiver Buffer Descriptor Number (RBD#)

The RBD# for each SCC channel defines the next BD to which the receiver will move data when it is in the IDLE state or defines the current BD during frame processing. The RBD# is the BD offset from the SCC base in the Rx BD table. For Rx BD 0, RBD# = $00; for Rx BD 1, RBD# = $08, etc. Upon reset, the CP main controller sets this register to zero. The user can change this register only after the ENR bit is clear and after the ENTER HUNT MODE command has been issued. In most applications, this parameter will never need to be modified by the user.

4.5.6.4 Transmit Buffer Descriptor Number (TBD#)

The TBD# for each SCC channel defines the next BD from which the transmitter will move data when it is in the IDLE state or defines the current BD during frame transmission. The TBD# is the BD offset from the SCC base in the Tx BD table. For Tx BD 0, TBD# = $40; for Tx BD 1, TBD# = $48, etc. Upon reset, the CP main controller sets this register to $40. The user can change this register only after the STOP TRANSMIT command has been issued. In most applications, this parameter will never need to be modified by the user.

4.5.6.5 Other General Parameters

Additional parameters are listed in Table 4-2. These parameters do not need to be accessed by the user in normal operation, and are listed only because they may provide helpful information for experienced users and for debugging.

The Rx and Tx internal data pointers are updated by the SDMA channels to show the next address in the buffer to be accessed.

The Tx byte count is a down-count value that is initialized with the Tx BD data length and decremented with every byte read by the SDMA channels. The Rx byte count is a down-count value that is initialized with the MRBLR value and decremented with every byte written by the SDMA channels.

NOTE

The Rx byte count, Rx internal data pointer, and RBD# can be used to extract data out of a receive buffer before the buffer is completely full. However, the use of this technique is not recommended unless no other solution to the application requirement can be found! The IMP was specifically designed to eliminate the need for this technique by allowing a programmable receive buffer size for each SCC, by closing buffers immediately upon an error, and by closing a receive buffer after a user-programmable line idle period in the case of UART mode. Having considered these capabilities, a user desiring to extract data from a partially full data buffer should note the following cautions:

1. The Rx byte count and Rx internal data pointer may not be valid before the first byte has been written to the buffer or after the last byte has been written to the buffer.

2. The parameters, Rx byte count, Rx internal data pointer, and RBD#, are not updated simultaneously.

3. The RBD# and the empty bit of the Rx BD are not updated simultaneously.

The Rx internal state, Tx internal state, Rx temp, Tx temp, and reserved areas are for RISC use only.

4.5.7 SCC Initialization

The SCCs require a number of registers and parameters to be configured after a power-on reset. The following is a proper sequence for initializing the SCCs, regardless of the protocol used.

1. If SCC2 or SCC3 is used, write the parallel port A and B control registers (PACNT and PBCNT) to configure pins as parallel I/O lines or peripheral functions as needed (see 3.3 Parallel I/O Ports).
2. Write SIMODE to configure the serial channels physical interface for the three SCCs

(i.e., NMSI, PCM, GCI, IDL modes). If IDL or GCI is chosen in SIMODE, write SIMASK in the serial channels physical interface (see 4.4.5 Serial Interface Registers).

3. Write SCON (see 4.5.2 SCC Configuration Register (SCON)).
4. Write SCM (SCC Mode) but do not set the ENT or ENR bits yet (see 4.5.3 SCC Mode Register (SCM)).
5. Write DSR as required if a protocol other than HDLC is used (see specific protocol section).
6. Initialize the required values in the general-purpose parameter RAM (see 4.5.6 SCC Parameter RAM Memory Map).
7. Initialize the required values in the protocol-specific parameter RAM (see specific protocol section).
8. Clear out any current events in SCCE, if desired (see specific protocol section).
9. Write SCCM to enable the interrupts in SCCE that should reach the interrupt controller (see specific protocol section).
10. Write IMR in the interrupt controller to enable the SCC interrupt to the interrupt controller (see 3.2.5.3 Interrupt Mask Register (IMR)).
11. Set the ENR and/or ENT bits in SCM (see 4.4.3 PCM Highway Mode).

The buffer descriptors may have their ready/empty bits set at any time. Notice that the command register (CR) does not need to be accessed following power-on reset. An SCC should be disabled and re-enabled (see 4.5.10 Disabling the SCCs) after any dynamic change in its parallel I/O ports or serial channels physical interface configuration. A full reset using the RST bit in the CR is a comprehensive reset that may also be used.

4.5.8 Interrupt Mechanism

Interrupt handling for each of the SCC channels is configured on a global per-channel basis in the interrupt pending register (IPR), the interrupt mask register (IMR), and the interrupt in-service register (ISR). Within each of these registers, one bit is used to either mask or report the presence of a pending or in-service interrupt in an SCC channel. However, an SCC interrupt may be caused by a number of events. To allow interrupt handling for SCC-specific events, further registers are provided within the SCCs.

Up to eight events can cause the SCC to interrupt the processor. The events differ in accordance with the SCC protocol chosen. The events are handled independently for each channel by the SCC event register (SCCE) and the SCC mask register (SCCM). All unmasked event bits must be cleared in order for the corresponding IPR bit to be cleared. The interrupt handler typically reads the event register, and then immediately clears those bits that it will deal with during the interrupt handler.

4.5.8.1 SCC Event Register (SCCE)

This 8-bit register is used to report events recognized by any of the SCCs. On recognition of an event, the SCC will set its corresponding bit in the SCC event register (regardless of the corresponding mask bit in the SCC mask register). The SCC event register is a memory-mapped register that may be read at any time. A bit is cleared by writing a one (writing a zero does not affect a bit's value).

NOTE

Bit manipulation instructions such as BSET should not be used to clear bits in the event register because any bits that were set will be written back as ones (thus clearing all pending interrupts) as well as the desired bit.

More than one bit may be cleared at a time. This register is cleared at reset (total system reset, CP reset, or the M68000 RESET instruction).

4.5.8.2 SCC Mask Register (SCCM)

This 8-bit read-write register allows enabling or disabling interrupt generation by the CP for specific events in each SCC channel. An interrupt will only be generated if the SCC interrupts for this channel are enabled in the IMR in the interrupt controller.

If a bit in the SCC mask register is zero, the CP will not proceed with its usual interrupt handling whenever that event occurs. Any time a bit in the SCC mask register is set, a one in the corresponding bit in the SCC event register will cause the SCC event bit in the IPR to be set.

The bit locations in the SCC mask register are identical to those in the SCC event register. SCCM is cleared upon reset.

4.5.8.3 SCC Status Register (SCCs)

Each SCCS reflects line status for that SCC. It is used primarily in the NMSI physical interface mode to read the current status of the $\overline{\text{CTS}}$ pin, the $\overline{\text{CD}}$ pin, and idle status of the RXD pin. This 8-bit read-only register may be read at any time.

The $\overline{\text{CTS}}$ status indication in the SCCS is not valid until after the SCC transmitter is enabled (ENT bit is set). After this, the $\overline{\text{CTS}}$ indication will only be updated in the SCCS when any change in its condition is sampled by a rising edge of TCLK. The $\overline{\text{CD}}$ and ID status indications are not valid until the SCC receiver is enabled (ENR bit is set). After this, the CD and ID indications will only be updated in the SCCS when any change in their condition is sampled by a rising edge of RCLK.

NOTE

Since the RISC controller is involved in the update process, a slight delay between the external line condition change and the update of the SCCS is induced.

Beyond what the SCCS provides, in the BDs for each protocol, indications are given as to whether the status of these signals has changed during the reception/transmission of a given buffer. Furthermore, in the event registers (SCCE) for each protocol, a maskable interrupt bit is provided to allow the detection of any change in signal status.

NOTE

After power-on reset, when the SCC is enabled for the first time, the SCCE register will show that a change of status occurred, re-

gardless of what happens externally. This signifies that the corresponding SCCS bit is now valid.

7	3	2	1	0
RESERVED		ID	CD	CTS

Bits 7–3—Reserved for future use.

ID—Idle Status on the Receiver Line

This bit is meaningful only if the SCC is programmed to HDLC or UART mode. In HDLC mode, this bit is a one after 15 continuous ones are received on the line. This bit will be zero after a single zero occurs on the line. If flags, rather than idles, are received between frames, the ID bit will remain zero between frames.

In UART mode, this bit is a one after one idle character (9 to 13 bits) is received and is a zero after a single zero occurs on the line (e.g., a start bit).

If the DIAG1–DIAG0 bits in the SCM are programmed to normal mode, then the $\overline{CD}$ signal is an enable signal for ID status. In this case, if $\overline{CD}$ is not asserted, the ID bit will always be one, regardless of the activity on the line.

If the DIAG1–DIAG0 bits in the SCM are programmed to software operation mode, then the ID bit will always reflect line activity, regardless of the state of the $\overline{CD}$ pin.

The ID bit is valid in both the multiplexed and nonmultiplexed modes, once the ENR bit is set.

$\overline{CD}$—Carrier Detect Status on the Channel Pin

This bit has the same polarity as the external pin. In the multiplexed modes, it is always zero. $\overline{CD}$ is undefined until ENR is set.

$\overline{CTS}$ —Clear-to-Send Status on the Channel Pin.

This bit has the same polarity as the external pin. In the PCM highway mode, it is always zero. In the GCI and IDL mode, if the SCC is connected to the D channel, then this bit is valid; otherwise, it is always zero. $\overline{CTS}$ is undefined until the ENT bit is set.

When the $\overline{CTS}$ and $\overline{CD}$ lines are programmed to software control in the SCC mode register, these lines do not affect the SCC and can be used for other purposes such as a data set ready (DSR), a data terminal ready (DTR) line, or an interrupt source in the SCCE register according to the behavior just described.

4.5.8.4 Bus Error on SDMA Access

When a bus error occurs on an access by the SDMA channel, the CP generates a unique interrupt (see 3.2 Interrupt Controller). The interrupt service routine should read the bus error channel number from the parameter RAM at BASE + 67C as follows:

0—SCC1 Tx Channel

1—SCC1 Rx Channel or DRAM Refresh Cycle

2—SCC2 Tx Channel

3—SCC2 Rx Channel

4—SCC3 Tx Channel

5—SCC3 Rx Channel

Next, the pointer that caused the bus error can be determined by reading the Rx or Tx internal data pointer from the parameter's memory map of the particular SCC. Following this bus error, the CP must be reset with a hardware reset or the setting of the RST bit in the command register.

An SDMA retry cycle is not indicated with any status information or interrupts.

4.5.9 SCC Transparent Mode

The SCC supports several transparent receive and transmit modes, which vary according to the protocol being implemented. As used here, transparent means data transparency and is not the same as the totally transparent (promiscuous) mode described later in 4.5.16 Transparent Controller. The transparent modes for each protocol are as follows:

UART Mode

If the normal mode is selected (UM1–UM0 = 00 in the UART mode register) and the control characters table is empty, then the UART will transfer all received characters to memory except break and idle characters.

HDLC Mode

When the HDLC mask register = $0000, the HDLC controller will transfer all received frames to the receive buffers, including address, control, data, and CRC. The HDLC controller still performs the standard HDLC functions of zero insertion/deletion and flag recognition.

BISYNC Mode

The BISYNC mode may be used to transparently receive data that is delimited by SYNCs. To do this, the BISYNC control characters table should be empty, and SYNC/DLE stripping should be disabled. Thereafter, all data following the SYNCs will be received into the receive buffers.

There are two possible ways of recognizing SYNCs. Either the EXSYN bit in the BISYNC mode register is cleared and a SYNC is defined by the SYN1–SYN2 characters in DSR, or the EXSYN bit is set and a SYNC is determined by an external SYNC pulse.

When the BISYNC control characters table is empty, the SYNC and DLE stripping is disabled, and the BISYNC controller is in normal nontransparent mode (RTR = 0 in BISYNC mode register). In this case, the configuration is as follows:

- If EXSYN in the BISYNC mode register is cleared, then the BISYNC controller transfers all characters that follow the SYN1–SYN2 sequence to the receive buffers.
- If EXSYN in the BISYNC mode register is set, then the BISYNC controller transfers all characters that follow the external SYNC pulse to the receive buffers.

NOTE

The BISYNC controller can reverse the bit order in both modes.

Totally Transparent (Promiscuous) Mode

The MC68302 can both receive and transmit the entire serial bit stream transparently. See 4.5.16 Transparent Controller for details.

4.5.10 Disabling the SCCs

If an SCC transmitter or receiver is not needed for a period of time or a mode change is required, then it may be disabled and re-enabled later. In this case, a sequence of operations is followed.

For the SCC transmitter, the sequence is as follows:

STOP TRANSMIT Command

Wait for the FIFO to empty

Clear ENT

-
- (The SCC transmitter is now disabled)
-

RESTART TRANSMIT Command

Set ENT

For the SCC receiver, the sequence is as follows:

Clear ENR

-
- (The SCC receiver is now disabled)
-

ENTER HUNT MODE Command

Set ENR

This sequence assures that any buffers in use will be properly closed and that new data will be transferred to/from a new buffer.

While an SCC is disabled (and only while an SCC is disabled) the SCON and SCM registers may be modified. Thus, once disabled, changes such as the SCC protocol, diagnostic mode, or baud rate may be made. Such parameters cannot be modified “on-the-fly.” The DSR should also only be modified while an SCC is disabled, although an exception exists to this in the UART mode concerning the transmission of partial stop bits.

The TBD# and RBD# values in the parameter RAM are not reset by the disabling process; thus, the very next BDs will be used when the SCC is re-enabled. A full software reset of the entire CP including the three SCCs is accomplished in the command register (CR). To reset an SCC to its initial state, the RX internal state, the TX internal state, the TBD#, and the RBD# can be written to their values after reset. The user can read these values for each SCC after a reset.

The SCC should be disabled and re-enabled if any change is made to the SCC's parallel I/O or serial channels physical interface configuration. The SCC does not need to be disabled if only a change to a parameter RAM value is made. See 4.5.6 SCC Parameter RAM Memory Map for a discussion of when parameter RAM values may be modified.

To save power, the SCCs may simply be disabled. Clearing the enable transmitter (ENT) bit in the SCC mode register causes the SCC transmitter to consume the least possible power; clearing the ENR bit causes a similar action for the SCC receiver.

The above statement on saving power is independent of a decision to use the low-power modes (see 3.8 System Control). If a low-power mode is desired, the SCC may be disabled before entering the low-power mode, or it may be left enabled so that an SCC interrupt may bring the IMP out of the low-power mode. One common use of the low-power mode is to disable the transmitter but leave the receiver enabled (i.e., in the hunt mode) so that an arriving frame destined for this station will cause an interrupt, waking the IMP from its low-power mode.

The low-power mode affects the M68000 core, not the SCCs. Since the SCCs are usually clocked at a far lower rate than the M68000 core, significant power savings may still be achieved with the SCCs fully enabled and the M68000 core in the low-power mode.

4.5.11 UART Controller

Many applications need a simple method of communicating low-speed data between equipment. The universal asynchronous receiver transmitter (UART) protocol is the *de-facto* standard for such communications. The term asynchronous is used because it is not necessary to send clocking information with the data that is sent. UART links are typically 38400 baud or less in speed and are character oriented (i.e., the smallest unit of data that can be correctly received or transmitted is a character). Typical applications of asynchronous links are connections between terminals and computer equipment. Even in applications where synchronous communication is required, the UART is often used for a local debugging port to run board debugger software. The character format of the UART protocol is shown in Figure 4-17.

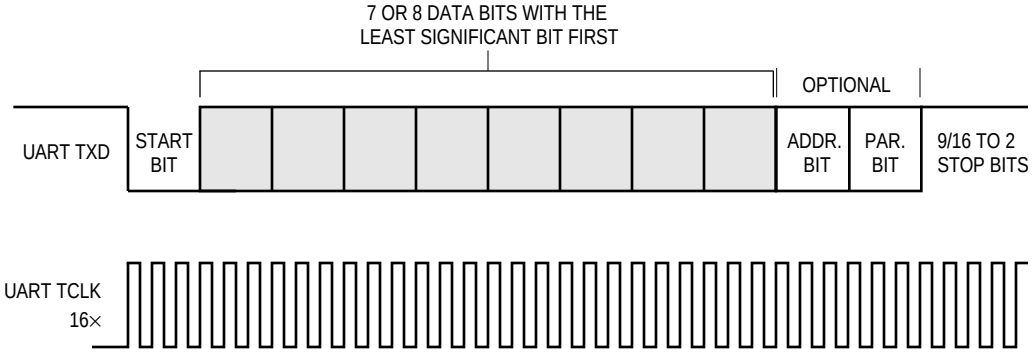


Figure 4-17. UART Frame Format

Since the transmitter and receiver work asynchronously, there is no need to connect transmit and receive clocks. Instead, the receiver over-samples the incoming data stream by a factor of 16 and uses some of these samples to determine the bit value. Traditionally, the middle three of the 16 samples are used. Two UARTs can communicate using a system like this if parameters such as the parity scheme and character length are the same for both transmitter and receiver.

When data is not transmitted in the UART protocol, a continuous stream of ones is transmitted. This is called the idle condition. Since the start bit is always a zero, the receiver can detect when real data is once again present on the line. The UART also specifies an all-zeros character, called a break, which is used to abort a character transfer sequence.

Many different protocols have been defined that use asynchronous characters, but the most popular of these is the RS-232 standard. RS-232 specifies standard baud rates, handshaking protocols, and mechanical/electrical details. Another popular standard using the same character format is RS-485, which defines a balanced line system allowing longer cables than RS-232 links. Synchronous protocols like HDLC or DDCMP are sometimes defined to run over asynchronous links. Other protocols like PROFIBUS (see Appendix C RISC Microcode from RAM) extend the UART protocol to include LAN-oriented features such as token passing.

All the standards provide handshaking signals, but some systems require just three physical lines: transmit data, receive data, and ground.

Many proprietary standards have been built around the asynchronous character frame, and some even implement a multidrop configuration. In multidrop systems, more than two stations may be present on a network, with each station having a specific address. Frames composed of many characters may be broadcast, with the first character acting as a destination address. To allow this procedure, the UART frame is extended by one bit to distinguish between an address character and the normal data characters.

By appropriately setting the SCC mode register, any of the SCC channels may be configured to function as a UART. The UART controller provides standard serial I/O using asynchronous character-oriented (start-stop) protocols. The UART may be used to communicate with other existing UART devices. Also, in conjunction with another SCC channel, it may be used in either ISDN terminal adaptor or X.25 packet assembly and disassembly (PAD) applications.

The UART provides a port for serial communication to other microprocessors, terminals, etc., either locally or through modems. It includes facilities for communication using standard asynchronous bit rates and protocols. The UART supports a multidrop mode for master/slave operation with wakeup capability on either an idle line or an address bit.

The UART uses a seven-pin interface in NMSI mode. It transmits data from memory (internal or external) to the TXD line and receives data from the RXD line into memory. The seven dedicated serial interface pins are transmit data (TXD), receive data (RXD), receive clock (RCLK), transmit clock (TCLK), carrier detect ($\overline{CD}$), clear to send ($\overline{CTS}$), and request to send

($\overline{\text{RTS}}$). Other modem lines such as data set ready (DSR) and data terminal ready (DTR) can be supported through the parallel I/O pins.

The UART consists of separate transmit and receive sections whose operations are asynchronous with the M68000 core and may be either synchronous or asynchronous with respect to each other. Each clock can be supplied either from the baud rate generator or from the external pins.

The UART key features are as follows:

- Flexible Message-Oriented Data Buffers
- Multidrop Operation
- Receiver Wakeup on IDLE Line or Address Mode
- Eight Control Character Comparison Registers
- Two Address Comparison Registers
- Four 16-Bit Error Counters
- Programmable Data Length (7 or 8 Bits)
- Programmable 1 or 2 Stop Bits with Fractional Stop Bits
- Even/Odd/Force/No Parity Generation
- Even/Odd/No Parity Check
- Frame Error, Noise Error, Break, and IDLE Detection
- Transmits Preamble and Break Sequences
- Freeze Transmission Option
- Maintenance of Four 16-Bit Error Counters
- Provides Asynchronous Link for DDCMP Use
- Flow Control Character Transmission Supported

4.5.11.1 Normal Asynchronous Mode

In the normal asynchronous mode, the receive shift register receives the incoming data on the RXD pin. The length and the format of the serial word in bits are defined by the control bits in the UART mode register. The order of reception is as follows:

Start Bit
Seven or Eight Data Bits with the Least Significant Bit First
Address/Data Bit (Optional)
Parity Bit (Optional)
Stop Bits

The receiver samples each bit of the incoming data three times around its center. The value of the bit is determined by the majority of those samples. If all the samples do not agree, a noise indication counter is incremented. When a complete character has been clocked in, the contents of the shift register are transferred to the UART receive data register. If there is an error in this character, then the appropriate error bits will be set by the IMP.

The UART may receive fractional stop bits. The next character's start bit may begin anytime after the 11th internal clock of the previous character's first stop bit (the UART uses a 16X clock).

The UART transmit shift register transmits the outgoing data on the TXD pin as shown in Figure 4-17. Data is clocked synchronously with the transmit clock, which may have either an internal or external source. The order of bit transmission is as stated for reception.

Only the data portion of the UART frame is actually stored in the data buffers. The start and stop bits are always generated and stripped by the UART controller. The parity bit may also be generated in the case of transmission, and checked during reception. Although parity is not stored in the data buffer, its value may be inferred by the reporting mechanism in the data buffer (i.e., characters with parity errors are identified). Similarly, the optional address bit is not stored in the transmit or receive data buffer, but is implied from the buffer descriptor itself. Parity is generated and checked for the address bit, when present.

4.5.11.2 Asynchronous DDCMP MODE

The IMP also allows the DDCMP protocol to be run over an asynchronous connection, using the UART. The description of this operation is contained in 4.5.14 DDCMP Controller. This operation uses the DDCMP buffer structures and the DDCMP-specific parameter RAM; however, the SCC mode register must be configured as a UART. The proper programming of the UART mode register to obtain asynchronous DDCMP is covered in 4.5.11.13 UART Mode Register.

4.5.11.3 UART Memory Map

When configured to operate in UART mode, the IMP overlays the structure (see Table 4-6) onto the protocol-specific area of that SCC's parameter RAM. Refer to 2.8 MC68302 Memory Map for the placement of the three SCC parameter RAM areas and to Table 4-5 for the other parameter RAM values.

Table 4-7. UART Specific Parameter RAM

Address	Name	Width	Description
SCC Base + 9C # SCC Base + 9E SCC Base + A0 #	MAX_IDL IDLC BRKCR	Word Word Word	Maximum IDLE Characters (Receive) Temporary Receive IDLE Counter Break Count Register (Transmit)
SCC Base + A2 # SCC Base + A4 # SCC Base + A6 # SCC Base + A8 #	PAREC FRMEC NOSEC BRKEC	Word Word Word Word	Receive Parity Error Counter Receive Framing Error Counter Receive Noise Counter Receive Break Condition Counter
SCC Base + AA # SCC Base + AC #	UADDR1 UADDR2	Word Word	UART ADDRESS Character 1 UART ADDRESS Character 2
SCC Base + AE SCC Base + B0 # SCC Base + B2 # SCC Base + B4 # SCC Base + B6 # SCC Base + B8 # SCC Base + BA # SCC Base + BC # SCC Base + BE #	RCCR CHARACTER1 CHARACTER2 CHARACTER3 CHARACTER4 CHARACTER5 CHARACTER6 CHARACTER7 CHARACTER8	Word Word Word Word Word Word Word Word Word	Receive Control Character Register CONTROL Character 1 CONTROL Character 2 CONTROL Character 3 CONTROL Character 4 CONTROL Character 5 CONTROL Character 6 CONTROL Character 7 CONTROL Character 8

Initialized by the user (M68000 core).

MAX_IDL

The UART controller watches the receive line, regardless of whether or not actual data is being received. If the line is idle, the UART controller counts how many idle characters have been received. An idle character is defined as 9 to 13 consecutive ones. For a given application, the number of bits in the idle character is calculated as follows:

1 + data length (either 7 or 8) + (1 if address bit used) + (1 if parity bit used) + number of stop bits (either 1 or 2)

MAX_IDL is programmed with a value from 1 (MAX_IDL = 1) to 65536 (MAX_IDL = 0).

Once a character of data is received on the line, the UART controller begins counting any idle characters received. If a MAX_IDL number of idle characters is received before the next data character is received, an idle timeout occurs, and the buffer is closed. This, in turn, can produce an interrupt request to the M68000 core to receive the data from the buffer. MAX_IDL then provides a convenient way to demarcate frames in the UART mode (see also 4.5.11.11 UART Error-Handling Procedure.

NOTE

Program MAX_IDL to $0001 for the minimum timeout value; program MAX_IDL to $0000 for the maximum timeout value.

IDLC

This value is used by the RISC to store the current idle counter value in the MAX_IDL timeout process. IDLC is a down counter. It does not need to be initialized or accessed by the user.

BRKCR

The UART controller will send a break character sequence whenever a STOP TRANSMIT command is given. The number of break characters sent by the UART controller is determined by the value in BRKCR. The length of one break character is 9 to 13 zeros depending on the configuration. The same equation applies for BRKCR as that used for MAX_IDL. See 4.5.11.8 Send Break for more details. BRKCR is programmed with a value from 0 (BRKCR = 0) to 65535 (BRKCR = 65535).

PAREC, FRMEC, NOSEC, BRKEC

These counters are initialized by the user. When the associated condition occurs, they will be incremented by the RISC controller. See 4.5.11.11 UART Error-Handling Procedure for more details.

UADDR1, UADDR2

In the multidrop mode, the UART controller can provide automatic address recognition of two addresses. In this case, the lower order byte of UADDR1 and UADDR2 are programmed by the user with the two desired addresses. See 4.5.11.6 UART Address Recognition for more details.

RCCR, CHARACTER

The UART controller can automatically recognize special characters and generate interrupts. It also allows a convenient method for inserting flow control characters into the transmit stream. See 4.5.11.7 UART Control Characters and Flow Control for more details.

If neither of these capabilities are desired, initialize CHARACTER1 to $8000 and CHARACTER8 to $0000 to disable both functions.

4.5.11.4 UART Programming Model

An SCC configured as a UART uses the same data structure as the other protocols. The UART data structure supports multibuffer operation. The UART may also be programmed to perform address comparison whereby messages not destined for a given programmable address are discarded. Also, the user can program the UART to accept or reject control characters. If a control character is rejected, an interrupt may be generated. The UART enables the user to transmit break and preamble sequences. Overrun, parity, noise, and framing errors are reported using the buffer descriptor (BD) table and/or error counters. An indication of the status of the line (idle) is reported through the status register, and a maskable interrupt is generated upon a status change.

In its simplest form, the UART can function in a character-oriented environment. Each character is transmitted with accompanying stop bits and parity (as configured by the user) and is received into separate one-byte buffers. Reception of each buffer may generate a maskable interrupt.

Many applications may want to take advantage of the message-oriented capabilities supported by the UART using linked buffers to receive or transmit data. In this case, data is handled in a message-oriented environment; users can work on entire messages rather than operating on a character-by-character basis. A message may span several linked buffers. For example, rather than being interrupted after the reception of each character, a terminal driver may want to wait until an end-of-line character has been typed by a user before handling the input data.

As another example, when transmitting ASCII files, the data may be transferred as messages ending on the end-of-line character. Each message could be both transmitted and received as a circular list of buffers without any intervention from the M68000 core. This technique achieves both ease in programming and significant savings in processor overhead.

On the receive side, the user may define up to eight control characters. Each control character may be configured to designate the end of a message (such as end of line) or to generate a maskable interrupt without being stored in the data buffer. This latter option is useful when flow-control characters such as XON or XOFF need to alert the M68000 core, yet do not belong to the message being received. Flow-control characters may also be transmitted at any time.

In the message-oriented environment, the data stream is divided into buffers. However, the physical format of each character (stop bits, parity, etc.) is not altered.

4.5.11.5 UART Command Set

These commands are issued to the command register described in 4.3 Command Set**.**

STOP TRANSMIT Command

After a hardware or software reset and the enabling of the channel by writing the SCC mode register, the channel is in the transmit enable mode and starts polling the first BD in the table approximately every eight transmit clocks.

The channel STOP TRANSMIT command disables the transmission of characters on the transmit channel. If this command is received by the UART controller during message transmission, transmission of that message is aborted. The UART completes transmission of any data already transferred to the UART FIFO (up to three characters) and then stops transmitting data. The TBD# is not advanced.

The UART transmitter will transmit a programmable number of break sequences and then start to transmit idles. The number of break sequences (which may be zero) should be written to the break count register (BRKCR) before this command is given to the UART controller.

The STOP TRANSMIT command must be issued before the SCC mode register is used to disable the transmitter if the transmitter will be reenabled at a later time.

RESTART TRANSMIT Command

The channel RESTART TRANSMIT command re-enables the transmission of characters on the transmit channel. This command is expected by the UART in three situations: after issuing a STOP TRANSMIT command, after issuing a STOP TRANSMIT and then disabling the channel using the SCC mode register, or after transmitter errors (CTS lost). The UART controller will resume transmission from the current transmitter BD number (TBD#) in the channel's Tx BD table.

If the transmitter is being re-enabled, the RESTART TRANSMIT command must be used and should be followed by the enabling of the transmitter in the SCC mode register.

ENTER HUNT MODE Command

After a hardware or software reset and the enabling of the channel by its SCC mode register, the channel is in the receive enable mode and will use the first BD in the table.

The ENTER HUNT MODE command is used to force the UART controller to abort reception of the current message, generate an RX interrupt (if enabled) as the buffer is closed, and enter the hunt mode. The UART controller will resume reception using the next BD once an address character or a single idle character is received. In multidrop hunt mode, the UART controller continually scans the input data stream for the address character. While not in multidrop mode, the UART controller will wait for a single IDLE character. In the UART mode, none of the data received in the FIFO is lost when ENTER HUNT MODE command is issued; however, this command does reset the receive FIFO in other protocols, e.g., HDLC.

If an enabled receiver has been disabled by clearing ENR in the SCC mode register, the ENTER HUNT MODE command must be given to the channel before setting ENR again. Reception will then begin with the next BD.

4.5.11.6 UART Address Recognition

In multidrop systems, more than two stations may be present on a network, with each having a specific address. Figure 4-18 shows two examples of such a configuration. Frames comprised of many characters may be broadcast, with the first character acting as a destination address. To achieve this, the UART frame is extended by one bit, called the address bit, to distinguish between an address character and the normal data characters. The UART can be configured to operate in a multidrop environment in which two modes are supported:

Automatic Multidrop Mode—The IMP automatically checks the incoming address character and accepts the data following it only if the address matches one of two 8-bit preset values. In this mode, UM1–UM0 = 11 in the UART mode register.

Nonautomatic Multidrop Mode—The IMP receives all characters. An address character is always written to a new buffer (it may be followed by data characters in the same buffer). In this mode, UM1–UM0 = 01 in the UART mode register.

Each UART controller has two 8-bit address registers (UADDR1 and UADDR2) for address recognition. In the automatic mode, the incoming address is checked against the lower order byte of the UART address registers. Upon an address match, the address match (M) bit in the BD is set/cleared to indicate which address character was matched. The data following it is written to the same data buffer.

NOTE

For 7-bit characters, the eighth bit (bit 7) in UADDR1 and UADDR2 should be zero.

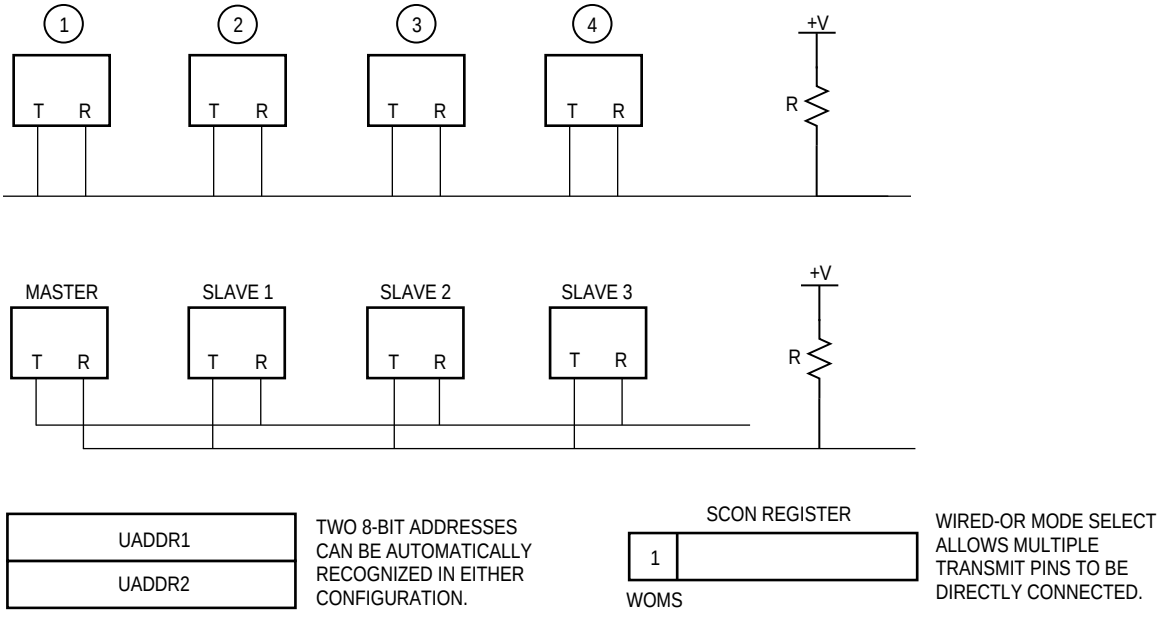


Figure 4-18. Two Configurations of UART Multidrop Operation

4.5.11.7 UART Control Characters and Flow Control

The UART has the capability to recognize special control characters. These characters may be used when the UART functions in a message-oriented environment. Up to eight control characters may be defined by the user in the control characters table. Each of these characters may be either stored (written to the receive buffer, after which the current buffer is closed and a new receive buffer taken) or rejected. If rejected, the character is written to the received control character register (RCCR) in internal RAM, and a maskable interrupt is generated. This method is useful for notifying the user of the arrival of control characters (e.g., XOFF) that are not part of the received messages.

The UART uses a table of 16-bit entries to support control-character recognition. Each entry consists of the control character, an end-of-table bit, and a reject character bit. The control characters table is shown in Figure 4-19.

NOTE

To disable all functions of the control characters and flow control table, initialize CHARACTER1 to $8000 and CHARACTER8 to $0000.

RCCR—Received Control Character Register

Upon a control character match for which the reject bit is set, the UART will write the control character into the RCCR and generate a maskable interrupt. The M68000 core must process the interrupt and read the RCCR before a second control character arrives. Failure to do so will result in the UART overwriting the first control character.

	15	14	13	12	11	10	9	8	7 … 0
OFFSET + 0									RCCR
OFFSET + 2	E	R							CHARACTER1
OFFSET + 4	E	R							CHARACTER2
OFFSET + 6	E	R							CHARACTER3
•									
•									
•									
OFFSET + 10	E	R	REA	I	CT	0	0	A	CHARACTER8

Figure 4-19. UART Control Characters Table

CHARACTER7–CHARACTER1—Control Character Value

These fields define control characters that should be compared to the incoming character. For 7-bit characters, the eighth bit (bit 7) should be zero.

E—End of Table

0 = This entry is valid. The lower eight bits will be checked against the incoming character.
1 = The entry is not valid. No valid entries lie beyond this entry.

NOTE

In tables with eight receive control characters, E is always zero.

R—Reject Character

0 = The character is not rejected but is written into the receive buffer. The buffer is then closed, and a new receive buffer is used if there is more data in the message. A maskable interrupt is generated in the RX bit of the UART event register.
1 = If this character is recognized, it will not be written to the receive buffer. Instead, it is written to the RCCR, and a maskable interrupt is generated in the CCR bit in the UART event register. The current buffer is not closed when a control character is received with R set.

Transmission of out-of-sequence characters is also supported and is normally used for the transmission of flow control characters such as XON or XOFF. This is performed using the last (eighth) entry in the UART control characters table. The UART will poll this character whenever the transmitter is enabled for UART operation: during freeze, during buffer transmission, and when no buffer is ready for transmission. The character is transmitted at a higher priority than the other characters in the transmit buffer (if any), but does not pre-empt characters already in the transmit FIFO.

CHARACTER8—Control Character Value

The eighth entry in the UART control characters table is defined as follows:

E—Empty

Must be one to use this entry as a flow control transmission character. To use this entry instead as a receive control characters entry, this E bit (and all other E bits in the table) should be zero.

R—Reject

Must be zero to use this entry as a flow control transmission character. For a receive control characters entry, it maintains its functionality as previously defined.

REA—Ready

This bit is set by the M68000 core when the character is ready for transmission and will remain one while the character is being transmitted. The CP clears this bit after transmission.

I—Interrupt

If set, the M68000 core will be interrupted when this character has been transmitted. (The TX bit will be set in the UART event register.)

CT—Clear-to-Send Lost

This status bit indicates that the $\overline{CTS}$ signal was negated during transmission of this character. If this occurs, the CTS bit in the UART event register will also be set.

NOTE

If the $\overline{CTS}$ signal was negated during transmission, and the CP transmits this character in the middle of buffer transmission, the $\overline{CTS}$ signal could actually have been negated either during this character's transmission (i.e., CHARACTER8) or during a buffer character's transmission. In this case, the CP sets the CT bit both here and in the Tx BD status word.

A—Address

When working in a multidrop configuration, the user should include the address bit in this position.

CHARACTER8—Flow Control Character Value

Any 7- or 8-bit character value may be transmitted. This value may be modified only while the REA bit is cleared. A 7-bit character should comprise bits 6–0.

4.5.11.8 Send Break

A break is an all-zeros character without stop bits—i.e., 9 to 13 continuous zeros. A break is sent by issuing the STOP TRANSMIT command. The UART completes transmission of any outstanding data in the FIFO and then sends 9 to 13 zeros (depending on the UM1–UM0, SL, PEN, and CL bits in the UART mode register). The UART transmits a programmable number of break characters according to the value of the break count register (BRKCR), and then reverts to idle or sends data if the RESTART TRANSMIT command was given before completion. Upon transmission of the entire set of break characters, the transmitter sends at least one high bit before transmitting any data to guarantee recognition of a valid start bit.

4.5.11.9 Send Preamble (IDLE)

A preamble sequence gives the programmer a convenient way of ensuring that the line goes idle before starting a new message. The preamble sequence length is 9 to 13 consecutive ones (depending on the UM1–UM0, SL, PEN, and CL bits in the UART mode register). If the preamble bit in a BD is set, the SCC will send a preamble sequence before transmitting that data buffer.

4.5.11.10 Wakeup Timer

By issuing the ENTER HUNT MODE command, the user can temporarily disable the UART receiver. It will remain inactive until an idle or address character is recognized (depending on the setting of UM1–UM0).

If the UART is still in the process of receiving a message that the user has already decided to discard, the message may be aborted by issuing the ENTER HUNT MODE command. The UART receiver will be re-enabled when the message is finished by detecting one idle

character of 9 to 13 consecutive ones (if UM1–UM0 = 00) or by the address bit of the next message (if UM0 = 1).

When the receiver is in sleep mode and a break sequence is received, the receiver will increment the BRKEC counter and generate the BRK interrupt (if enabled).

4.5.11.11 UART Error-Handling Procedure

The UART controller reports character reception and transmission error conditions through the channel BDs, the error counters, and the UART event register (SCCE). The modem interface lines can also be monitored directly by the SCC status register.

Transmission Error

Clear to Send Lost During Character Transmission. When this error occurs and the channel is not programmed to control this line with software, the channel terminates buffer transmission, closes the buffer, sets the CTS lost (CT) bit in the BD, and generates the TX interrupt (if enabled). The channel will resume transmission after the reception of the RESTART TRANSMIT command.

Reception Errors

1. Overrun Error. The UART controller maintains an internal three-byte FIFO for receiving data. The CP begins programming the SDMA channel (if the data buffer is in external memory) when the first byte is received into the FIFO. When a receiver FIFO overrun occurs, the channel writes the received character into the internal FIFO over the previously received character (the previous character and its status bits are lost). Then the channel writes the received character to the buffer, closes the buffer, sets overrun (OV) in the BD, and generates the RX interrupt (if enabled). In automatic multidrop mode, the receiver enters hunt mode immediately.
2. Carrier Detect Lost During Character Reception. When this error occurs and the channel is not programmed to control this line with software, the channel terminates character reception, closes the buffer, sets the carrier detect lost (CD) bit in the BD, and generates the RX interrupt (if enabled). This error's priority is the highest; the last character in the buffer is lost and other errors are not checked. In automatic multidrop mode, the receiver enters hunt mode immediately.
3. Framing Error. Framing error is reported by the UART controller when no stop bit is detected in a received data string. When this error occurs, the channel writes the received character to the buffer, closes the buffer, sets framing error (FR) in the BD, and generates the RX interrupt (if enabled). The channel also increments the framing error counter (FRMEC). When this error occurs, parity is not checked for this character. In automatic multidrop mode, the receiver enters hunt mode immediately.
4. Parity Error. When the parity error occurs, the channel writes the received character to the buffer, closes the buffer, sets parity error (PR) in the BD, and generates the RX interrupt (if enabled). The channel also increments the parity error counter (PAREC). In automatic multidrop mode, the receiver enters hunt mode immediately.
5. Noise Error. Noise error is detected by the UART controller when the three samples taken on every bit are not identical. When this error occurs, the channel writes the received character to the buffer and proceeds normally but increments the noise error

counter (NOSEC).

6. IDLE Sequence. Receive IDLE (preamble) is detected by the UART controller when a character with 9 to 13 consecutive ones (depending on the UM1–UM0, SL, PEN, and CL bits in the UART mode register) is received. When an IDLE sequence is received, the channel starts to count the number of IDLE sequences received. If it reaches the MAX_IDL value, the buffer is closed and an RX interrupt is generated (if enabled). The counter is reset every time a character is received.
7. BREAK Sequence. A BREAK sequence is detected by the UART receiver when a character with zero value and framing error is received. When a BREAK sequence is received, the channel will increment the BRKEC counter, close the buffer, set the BR bit (if a buffer was currently open), and generate a BRK interrupt (if enabled). Also, if the channel was in the middle of buffer processing, the buffer is closed and an RX is generated (if enabled). A long break sequence only increments the counter once.

Error Counters

The UART maintains four 16-bit (modulo–2**16) error counters for the receive portion of each UART controller. They can be initialized by the user when the channel is disabled. The counters are as follows:

PAREC—Parity Error Counter
FRMEC—Framing Error Counter
NOSEC—Noise Error Counter
BRKEC—BREAK Error Counter

4.5.11.12 Fractional Stop Bits

The UART transmitter can be programmed to transmit fractional stop bits. Three bits in the SCC data synchronization register (DSR) are used to program the length of the last stop bit transmitted. These DSR bits may be modified at any time. If two stop bits are transmitted, only the second one is affected. Idle characters are always transmitted as full-length characters. In UART mode, bits 14–12 in the DSR are now decoded as follows:

14–12 of DSR			
111	Last Transmit Stop Bit	16/16	(the default value after reset)
110	Last Transmit Stop Bit	15/16	
. . .			
001	Last Transmit Stop Bit	10/16	
000	Last Transmit Stop Bit	9/16	

The setting of the DSR in combination with the setting of the CL bit in the UART mode register causes the number of stop bits transmitted to be either 9/16 to 1 or 1-9/16 to 2 stop bits.

The UART receiver can always receive fractional stop bits. The next character's start bit may begin anytime after the 11th internal clock of the previous character's first stop bit (the UART uses a 16x clock).

4.5.11.13 UART Mode Register.

Each SCC mode register is a 16-bit, memory- mapped, read-write register that controls the SCC operation. The term UART mode register refers to the protocol-specific bits (15–6) of the SCC mode register when that SCC is configured as a UART. The read-write UART mode register is cleared by reset.

15	14	13	12	11	10	9	8	7	6	5 … 0
TPM1	TPM0	RPM	PEN	UM1	UM0	FRZ	CL	RTSM	SL	COMMON SCC MODE BITS

TPM1–TPM0—Transmitter Parity Mode

TMP1—TMP0 select the type of parity to be performed.

00 = Odd parity; always send an odd number of ones.
01 = Force low parity; always send a zero in the parity bit position.
10 = Even parity; always send an even number of ones.
11 = Force high parity; always send a one in the parity bit position.

RPM—Receiver Parity Mode

0 = Odd parity
1 = Even parity

When odd parity is selected, the receiver will count the number of ones in the data word. If the total number of ones is not an odd number, the parity bit is set to one to produce an odd number of ones. If the receiver counts an even number of ones, an error in transmission has occurred. Similarly, for even parity, an even number of ones must result from the calculation performed at both ends of the line.

PEN—Parity Enable

0 = No parity
1 = Parity is enabled for the transmitter and receiver as determined by the parity mode bits.

UM1–UM0—UART Mode 1–0

00 = Normal UART operation. Multidrop mode is disabled for point-to-point operation and an idle-line wakeup is selected. In the idle-line wakeup mode, the UART receiver is re-enabled by an idle string of 9 to 13 consecutive ones (depending on character length and parity mode).
01 = In the multidrop mode, an additional address/data bit is transmitted with each character. The multidrop asynchronous modes are compatible with the Motorola MC68681 DUART, the Motorola MC68HC11 SCI interface, and the Motorola DSP56000 SCI interface. UM0 is also used to select the wakeup mode before enabling the receiver or issuing the ENTER HUNT MODE command.
Multidrop mode is enabled and an address bit wakeup is selected. In the address bit wakeup mode, the UART receiver is re-enabled when the last data bit (the 8th or 9th) in a character is one. This configuration means that the received character is an address, which should be processed by all inactive processors. The IMP re-

ceives the address character and writes it to a new buffer. No address recognition is performed.

10 = The DDCMP protocol is implemented over the asynchronous channel.

11 = Multidrop mode is enabled as in the 01 case, and the IMP automatically checks the address of the incoming address character and either accepts or discards the data following the address.

FRZ—Freeze Transmission

This bit allows the user to halt the UART transmitter and to continue transmission from the next character in the buffer at a later time.

0 = Normal operation (or resume transmission after FRZ is set).

1 = The UART completes transmission of any data already transferred to the UART FIFO (up to three characters) and then stops transmitting data. The UART continues to receive normally.

CL—Character Length

0 = 7-bit character length. On receive, bit 7 in memory is written as zero. On transmit, bit 7 in memory is a don't care.

1 = 8-bit character length

RTSM—RTS Mode

0 = $\overline{\text{RTS}}$ is asserted whenever the transmitter is enabled and there are characters to transmit. $\overline{\text{RTS}}$ is negated after the last stop bit of a transmitted character when both the shift register and the transmit FIFO are empty. RTS is also negated at the end of a buffer to guarantee accurate reporting of the CTS bit in the BD.

1 = $\overline{\text{RTS}}$ is asserted whenever the transmitter is enabled (the ENT bit is set).

SL—Stop Length

This bit selects the number of the stop bits transmitted by the UART. The receiver is always enabled for one stop bit. Fractional stop bits are configured in the DSR (see 4.5.11.12 Fractional Stop Bits).

0 = One stop bit

1 = Two stop bits

COMMON SCC MODE BITS—see 4.5.3 SCC Mode Register (SCM) for a description of the DIAG1, DIAG0, ENR, ENT, MODE1, and MODE0 bits.

4.5.11.14 UART Receive Buffer Descriptor (Rx BD)

The CP reports information about each buffer of received data by its BDs. The Rx BD is shown in Figure 4-20. The CP closes the current buffer, generates a maskable interrupt, and starts to receive data in the next buffer due to any of the following events:

1. Reception of a user-defined control character (when reject (R) bit = 0)
2. Detection of an error during message processing
3. Detection of a full receive buffer
4. Reception of a programmable number of consecutive IDLE characters

5. Reception of an address character when working in multidrop mode

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET + 0	E	X	W	I	C	A	M	ID	—	—	BR	FR	PR	—	OV	CD
OFFSET + 2	DATA LENGTH															
OFFSET + 4	RX BUFFER POINTER (24-bits used, upper 8 bits must be 0)															
OFFSET +6																

Figure 4-20. UART Receive Buffer Descriptor

The first word of the Rx BD contains the control and status bits.

NOTE

In the nonautomatic multidrop mode (UM1–UM0 = 01), the address character will be written into the next buffer for comparison by the user software.

An example of the UART receive process is shown in Figure 4-21. This figure shows the resulting state of the Rx BDs after receipt of 10 characters, an idle period, and five characters—one with a framing error. The example assumes that MRBLR = 8 in the SCC parameter RAM.

E—Empty

0 = The data buffer associated with this BD has been filled with received data, or data reception has been aborted due to an error condition. The M68000 core is free to examine or write to any fields of the BD.

1 = The data buffer associated with the BD is empty. This bit is used to signify that the BD and its associated buffer are available to the CP. After it sets this bit, the M68000 core should not write to any fields of this BD when this bit is set. Note that the empty bit will remain set while the CP is currently filling the buffer with received data.

X—External Buffer

0 = The buffer associated with this BD is in internal dual-port RAM.

1 = The buffer associated with this BD is in external memory.

W—Wrap (Final BD in Table)

0 = This is not the last BD in the Rx BD table.

1 = This is the last BD in the Rx BD table. After this buffer has been used, the CP will receive incoming data into the first BD in the table, allowing the user to use fewer than eight BDs to conserve internal RAM.

NOTE

The user is required to set the wrap bit in one of the first eight BDs; otherwise, errant behavior may occur.

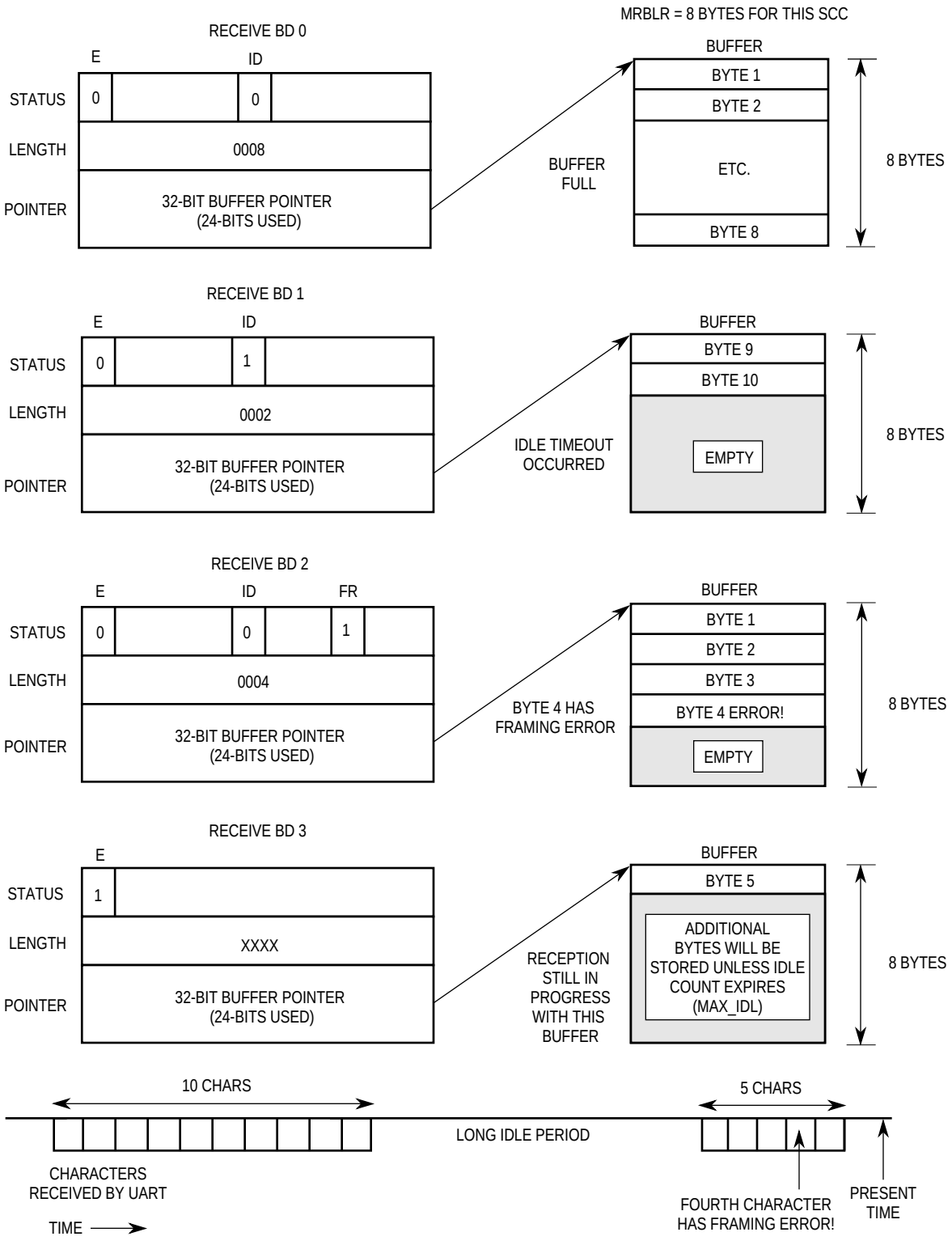


Figure 4-21. UART Rx BD Example

I—Interrupt

0 = No interrupt is generated after this buffer has been filled.
1 = The RX bit in the UART event register will be set when this buffer has been completely filled by the CP, indicating the need for the M68000 core to process the buffer. The RX bit can cause an interrupt.

The following bits contain status information written by the CP after it has finished receiving data in the associated data buffer.

C—Control Character

0 = This buffer does not contain a control character.
1 = This buffer contains a user-defined control character in the last byte location.

A—Address

0 = The buffer contains data only.
1 = When working in nonautomatic multidrop mode (UM1–UM0 = 01), this bit indicates that the first byte of this buffer contains an address byte. The address comparison should be implemented in software. In automatic multidrop mode, this bit indicates that the BD contains a message received immediately following an address recognized in UADDR1 or UADDR2. This address is not written into the receive buffer.

M—Address Match

This bit is meaningful only if the A bit (bit 10) is set and UM1–UM0 = 11 in the UART mode register. Following an address match, this bit defines which address character matched the user-defined address character, enabling the UART to receive the data.

0 = The address-matched user-defined UADDR2
1 = The address-matched user-defined UADDR1

ID—Buffer Closed on Reception of Idles

The buffer was closed due to the reception of the programmable number of consecutive IDLE sequences (defined in MAX_IDL).

Bits 7–6, 2—Reserved for future use.

BR—Break Received

A break sequence was received while receiving data into this buffer.

FR—Framing Error

A character with a framing error was received and is located in the last byte of this buffer. A framing error is detected by the UART controller when no stop bit is detected in the receive data string.

PR—Parity Error

A character with a parity error was received and is located in the last byte of this buffer.

OV—Overrun

A receiver overrun occurred during message reception.

CD—Carrier Detect Lost

The carrier detect signal was negated during message reception.

Data Length

Data length contains the number of octets written by the CP into this BD's data buffer. It is written by the CP once as the BD is closed.

NOTE

The actual amount of memory allocated for this buffer should be greater than or equal to the contents of maximum receive buffer length register (MRBLR).

Rx Buffer Pointer

The receive buffer pointer, which always points to the first location of the associated data buffer, may be even or odd. The buffer may reside in either internal or external memory.

NOTE

For correct operation of the function codes, the upper 8 bits of the pointer must be initialized to zero.

4.5.11.15 UART Transmit Buffer Descriptor (Tx BD)

Data is presented to the CP for transmission on an SCC channel by arranging it in buffers referenced by the channel's Tx BD table. The CP confirms transmission (or indicates error conditions) through the BDs to inform the M68000 core that the buffers have been serviced. The Tx BD shown in Figure 4-22.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET + 0	R	X	W	I	CR	A	P	—	—	—	—	—	—	—	—	CT
OFFSET + 2	DATA LENGTH															
OFFSET + 4 OFFSET +6	TX BUFFER POINTER (24-bits used, upper 8 bits must be 0)															

Figure 4-22. UART Transmit Buffer Descriptor

The first word of the Tx BD contains status and control bits. The following bits are prepared by the user before transmission and set by the CP after the buffer has been transmitted.

R—Ready

0 = This buffer is not currently ready for transmission. The user is free to manipulate the BD (or its associated buffer). The CP clears this bit after the buffer has been transmitted or after an error condition has been encountered.

1 = The data buffer, which has been prepared for transmission by the user, has not been transmitted or is currently transmitting. No fields of this BD may be written by the user once this bit is set.

X—External Buffer

0 = The buffer associated with this BD is in internal dual-port RAM.
1 = The buffer associated with this BD is in external memory.

W—Wrap (Final BD in Table)

0 = This is not the last BD in the Tx BD table.
1 = This is the last BD in the Tx BD table. After this buffer has been used, the CP will transmit data from the first BD in the table.

NOTE

The user is required to set the wrap bit in one of the first eight BDs; otherwise, errant behavior may occur.

I—Interrupt

0 = No interrupt is generated after this buffer has been serviced.
1 = The TX bit in the UART event register will be set when this buffer has been serviced by the CP, which can cause an interrupt.

Bits 8–1—Reserved for future use.

CR—Clear-to-Send Report

This bit allows a choice of no delay between buffers transmitted in UART mode, versus a more accurate CTS lost error reporting and two bits of idle between buffers.

0 = The buffer following this buffer will be transmitted with no delay (assuming it is ready), but the CT bit may not be set in the correct Tx BD, or may not be set at all in a CTS lost condition. The user is advised to monitor the CTS bit in the UART event register for an indication of CTS lost, in addition to the CT bits in the Tx BDs. The CTS bit will always be set properly.
1 = Normal CTS lost (CT bit) error reporting, and two bits of idle occur between back-to-back buffers.

If the DIAG1–DIAG0 bits in the SCM are set to software operation (rather than normal operation), then this bit only affects the delay between buffers, not the CTS reporting, and would normally be set to zero.

A—Address

This bit is valid only in multidrop mode (UM0 = 1).
0 = This buffer contains data only.
1 = Set by the M68000 core, this bit indicates that this buffer contains address character(s). All the buffer's data will be transmitted as address characters.

P—Preamble

0 = No preamble sequence is sent.
1 = The UART sends one preamble sequence (9 to 13 ones) before sending the data.

The following bits are written by the CP after it has finished transmitting the associated data buffer.

CT—CTS Lost

0 = The $\overline{\text{CTS}}$ signal remained active during transmission.
1 = The $\overline{\text{CTS}}$ signal was negated during transmission.

Data Length

The data length is the number of octets that the CP should transmit from this BD's data buffer. It is never modified by the CP. This value should be normally greater than zero. The data length may be equal to zero with the P bit set, and only a preamble will be sent.

Tx Buffer Pointer

The transmit buffer pointer, which always points to the first location of the associated data buffer, may be even or odd. The buffer may reside in either internal or external memory.

NOTE

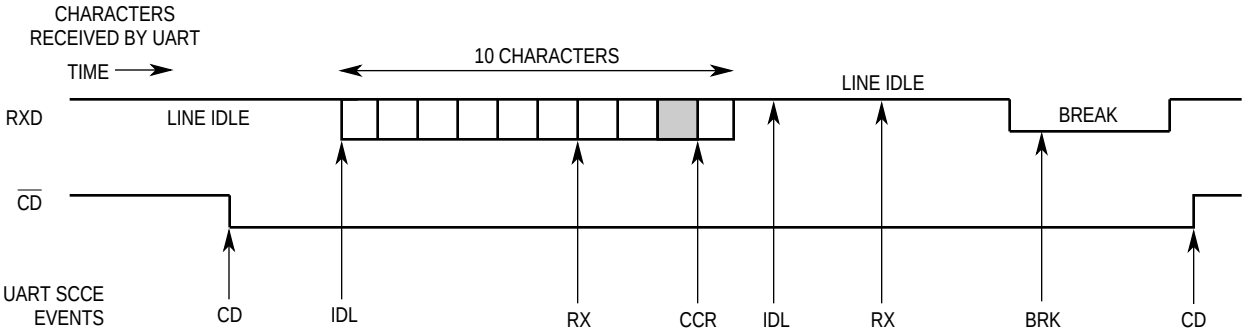
For correct operation of the function codes, the upper 8 bits of the pointer must be initialized to zero.

4.5.11.16 UART Event Register

The SCC event register (SCCE) is called the UART event register when the SCC is operating as a UART. It is an 8-bit register used to report events recognized by the UART channel and generate interrupts. On recognition of an event, the UART controller will set the corresponding bit in the UART event register. Interrupts generated by this register may be masked in the UART mask register.

The UART event register is a memory-mapped register that may be read at any time. A bit is cleared by writing a one (writing a zero does not affect a bit's value). More than one bit may be cleared at a time. All unmasked bits must be cleared before the CP will clear the internal interrupt request. This register is cleared at reset.

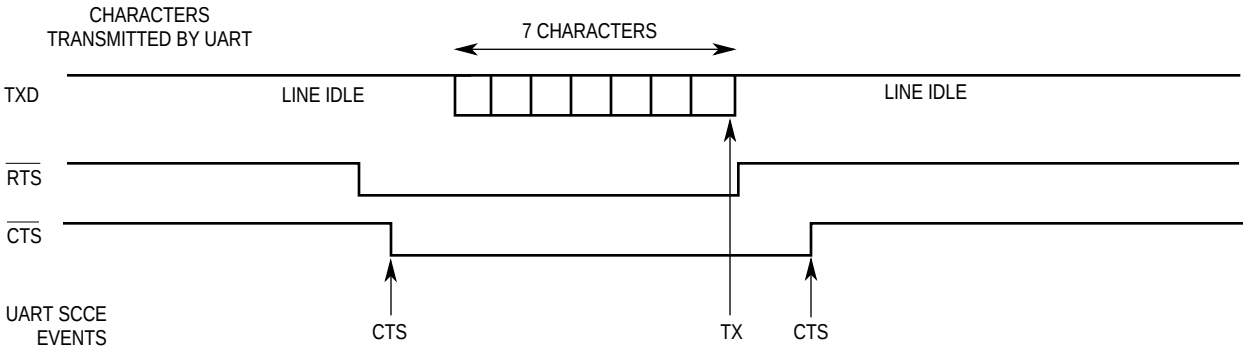
An example of the timing of various events in the UART event register is shown in Figure 4-23.



NOTES:
1. The first RX event assumes receive buffers are six bytes each.
2. The second IDL event occurs after 9 to 13 ones received in a row.
3. The second RX event position is programmable based on the max_IDL value.
4. The BRK event occurs after the first break character is received.

LEGEND:

Is a receive control character defined not to be stored in the receive buffer.



NOTE: TX event assumes all seven characters were put into a single buffer.

Figure 4-23. UART Interrupt Events Example

7	6	5	4	3	2	1	0
CTS	CD	IDL	BRK	CCR	BSY	TX	RX

CTS—Clear-To-End Status Changed

A change in the status of the $\overline{\text{CTS}}$ line was detected on the UART channel. The SCC status register may be read to determine the current status.

CD—Carrier Detect Status Changed

A change in the status of the $\overline{\text{CD}}$ line was detected on the UART channel. The SCC status register may be read to determine the current status.

IDL—IDLE Sequence Status Changed

A change in the status of the receive serial line was detected on the UART channel. The SCC status register may be read to determine the current status.

BRK—Break Character Received

A break character was received.

CCR—Control Character Received

A control character was received (with reject (R) character = 1) and stored in the receive control character register (RCCR).

BSY—Busy Condition

A character was received and discarded due to lack of buffers. The receiver automatically enters hunt mode immediately if in the multidrop mode. The latest that an Rx BD can be made empty (have its empty bit set) and still avoid the busy condition is the middle of the stop bit of the first character to be stored in that buffer.

TX—Tx Buffer

A buffer has been transmitted over the UART channel. If CR = 1 in the Tx BD, this bit is set no sooner than when the last data bit of the last character in the buffer begins to be transmitted. If CR = 0, this bit is set after the last character was written to the transmit FIFO.

RX—Rx Buffer

A buffer has been received over the UART channel. This event occurs no sooner than the middle of the first stop bit of the character that causes the buffer to be closed.

4.5.11.17 UART MASK Register

The SCC mask register (SCCM) is referred to as the UART mask register when the SCC is operating as a UART. It is an 8-bit read-write register with the same bit formats as the UART event register. If a bit in the UART mask register is a one, the corresponding interrupt in the event register will be enabled. If the bit is zero, the corresponding interrupt in the event register will be masked. This register is cleared upon reset.

4.5.11.18 S-Records Programming Example

In the following paragraphs, an example of a downloading application is given that utilizes an SCC channel as a UART controller. The application performs downloads and uploads of S records between a host computer and an intelligent peripheral through a serial asynchronous line.

The S records are strings of ASCII characters that begin with `S' and end in an end-of-line character. This characteristic will be used to impose a message structure on the communication between the devices. Note that each device may also transmit XON and XOFF characters for flow control, which do not form part of the program being uploaded or downloaded.

The UART mode register should be set as required, with the freeze (FRZ) bit cleared and the enable transmitter/receiver (ENT, ENR) bits set. Receive buffers should be linked to the receive buffer table with the interrupt (I) bit set. For simplicity, assume that the line is not multidrop (no addresses are transmitted) and that each S record will fit into a single data buffer.

Three characters should first be entered into the UART control character table:

1. End of Line—The empty (E) bit is cleared; the reject (R) bit is cleared. When an end-of-line character is received, the current buffer is closed (the next BD taken by the IMP) and made available to the M68000 core for processing. This buffer contains an entire S record, which the processor can now check and copy to memory or disk as required.
2. XOFF—E should be cleared and R should be set. Whenever the M68000 core receives a control character received interrupt and the receive control character register contains XOFF, the software should immediately stop transmitting to the other station by setting the FRZ bit in the UART mode register. This prevents data from being lost by the other station when it runs out of receive buffers.
3. XON—XON should be received after XOFF. E should be cleared and R should be set. The FRZ bit on the transmitter should now be cleared. The IMP automatically resumes transmission of the serial line at the point at which it was previously stopped. Like XOFF, the XON character is not stored in the receive buffer.

To receive the S records, the M68000 core must only wait for the RX interrupt, indicating the reception of a complete S-record buffer. Transmission requires assembling S records into data buffers and linking them to the transmit buffer table (transmission may be temporarily halted by reception of an XOFF character). This scheme minimizes the number of interrupts received by the M68000 core (one per S record) and relieves it from the task of continually scanning for control characters.

4.5.12 HDLC Controller

Layer 2 of the seven-layer OSI model is the data link layer. One of the most common layer 2 protocols is HDLC. Many other common layer 2 protocols are heavily based on HDLC, particularly its framing structure: namely, SDLC, SS#7, LAPB, and LAPD. The framing structure of HDLC is shown in Figure 4-24.

OPENING FLAG	ADDRESS	CONTROL	INFORMATION (OPTIONAL)	CRC	CLOSING FLAG
8 BITS	16 BITS	8 BITS	8N BITS	16 BITS	8 BITS

Figure 4-24. Typical HDLC Frame

HDLC uses a zero insertion/deletion process (commonly known as bit-stuffing) to ensure that the bit pattern of the delimiter flag does not occur in the fields between flags. The HDLC frame is synchronous and therefore relies on the physical layer to provide a method of clocking and synchronizing the transmitter and receiver.

Since the layer 2 frame can be transmitted over a point-to-point link, a broadcast network, or packet and circuit-switched systems, an address field is needed to carry the frame's destination address. The length of this field is commonly 0, 8, or 16 bits, depending on the data link layer protocol. For instance, SDLC and LAPB use an 8-bit address. SS#7 has no address field at all because it is always used in point-to-point signaling links. LAPD further divides its 16-bit address into different fields to specify various access points within one piece of equipment. It also defines a broadcast address. Some HDLC-type protocols also allow for extended addressing beyond 16-bits.

The 8- or 16-bit control field provides a flow control number and defines the frame type (control or data). The exact use and structure of this field depends upon the protocol using the frame.

Data is transmitted in the data field, which can vary in length depending upon the protocol using the frame. Layer 3 frames are carried in the data field.

Error control is implemented by appending a cyclic redundancy check (CRC) to the frame, which is 16-bits long in most protocols, but may be 32-bits long in some.

When the MODE1–MODE0 bits of an SCC mode register (SCM) select the HDLC mode, then that SCC functions as an HDLC controller. The HDLC controller handles the basic functions of the HDLC/SDLC protocol on either the D channel, a B channel, or from a multiplexed serial interface (IDL, GCI (IOM-2), or PCM highway). When the HDLC controller is used to support the B or D channel of the ISDN, the SCC outputs are internally connected to the physical layer serial interface.

NOTE

SDLC is fully supported, but the SDLC loop mode (ring configuration) is not supported.

When an SCC in HDLC mode is used with a nonmultiplexed modem interface, then the SCC outputs are connected directly to the external pins. In this case, the serial interface uses seven dedicated pins: transmit data (TXD), receive data (RXD), receive clock (RCLK), transmit clock (TCLK), carrier detect ($\overline{CD}$), clear to send ($\overline{CTS}$), and request to send ($\overline{RTS}$). Other modem signals may be supported through the parallel I/O pins.

The HDLC controller consists of separate transmit and receive sections whose operations are asynchronous with the M68000 core and may be either synchronous or asynchronous with respect to the other SCCs. Up to eight frames may be transmitted or received without M68000 core intervention. When the HDLC controller is connected to one of the multiplexed physical interface options (IDL, GCI, or PCM highway), the receive and transmit clocks are identical and are supplied externally by the physical layer. In non-ISDN applications, each clock can be supplied either from the baud rate generator or externally. The baud rate generator is discussed more fully in 4.5.2 SCC Configuration Register (SCON).

The HDLC controller key features are as follows:

- Flexible Data Buffers with Multiple Buffers per Frame Allowed
- Separate Interrupts for Frames and Buffers (Receive and Transmit)
- Four Address Comparison Registers with Mask
- Maintenance of Five 16-Bit Error Counters
- Flag/Abort/Idle Generation/Detection
- Zero Insertion/Deletion
- NRZ/NRZI Data Encoding
- 16-Bit or 32-Bit CRC-CCITT Generation/Checking

- Detection of Non-Octet Aligned Frames
- Detection of Frames That Are Too Long
- Programmable Flags (0–15) between Successive Frames
- Automatic Retransmission in Case of Collision

4.5.12.1 HDLC Channel Frame Transmission Processing

The HDLC transmitter is designed to work with almost no intervention from the M68000 core. When the M68000 core enables one of the transmitters, it will start transmitting flags or idles as programmed in the HDLC mode register. The HDLC controller will poll the first buffer descriptor (BD) in the transmit channel's BD table. When there is a frame to transmit, the HDLC controller will fetch the data from memory and start transmitting the frame (after first transmitting the user-specified minimum number of flags between frames). When the end of the current BD has been reached and the last buffer in the frame bit is set, the cyclic redundancy check (CRC), if selected, and the closing flag are appended.

Following the transmission of the closing flag, the HDLC controller writes the frame status bits into the BD and clears the ready bit. When the end of the current BD has been reached, and the last bit is not set (working in multibuffer mode), only the ready bit is cleared. In either mode, an interrupt is issued according to the interrupt bit in the BD. The HDLC controller will then proceed to the next BD in the table. In this way, the user may be interrupted after each buffer, after a specific buffer has been transmitted, or after each frame.

To rearrange the transmit queue before the IMP has completed transmission of all buffers, issue the STOP TRANSMIT command. This technique can be useful for transmitting expedited data before previously linked buffers or for error situations. When receiving the STOP TRANSMIT command, the HDLC controller will abort the current frame being transmitted and start transmitting idles or flags. When the HDLC controller is given the RESTART TRANSMIT command, it resumes transmission.

4.5.12.2 HDLC Channel Frame Reception Processing

The HDLC receiver is also designed to work with almost no intervention from the M68000 core. The HDLC receiver can perform address recognition, CRC checking, and maximum frame length checking. The received frame (all fields between the opening and closing flags) is made available to the user for performing any HDLC-based protocol.

When the M68000 core enables one of the receivers, the receiver waits for an opening flag character. When the receiver detects the first byte of the frame, the HDLC controller will compare the frame address against the user-programmable addresses. The user has four 16-bit address registers and an address mask available for address matching. The HDLC controller will compare the received address field to the user-defined values after masking with the address mask. The HDLC controller can also detect broadcast (all ones) addressed frames, if one address register is written with all ones.

If a match is detected, the HDLC controller will fetch the next BD and, if empty, will start to transfer the incoming frame to the BD's associated data buffer starting with the first address byte. When the data buffer has been filled, the HDLC controller clears the empty bit in the BD and generates an interrupt if the interrupt bit in the BD is set. If the incoming frame ex-

ceeds the length of the data buffer, the HDLC controller will fetch the next BD in the table and, if it is empty, will continue to transfer the rest of the frame to this BD's associated data buffer.

During this process, the HDLC controller will check for a frame that is too long. When the frame ends, the CRC field is checked against the recalculated value and is written to the data buffer starting with the first address byte. The data length written to the last BD in the HDLC frame is the length of the entire frame. This enables HDLC protocols that “lose” frames to correctly recognize the frame-too-long condition. The HDLC controller then sets the last buffer in frame bit, writes the frame status bits into the BD, and clears the empty bit. The HDLC controller next generates a maskable interrupt, indicating that a frame has been received and is in memory. The HDLC controller then waits for a new frame. Back-to-back frames may be received with only a single shared flag between frames. Also, flags that share a zero will be recognized as two consecutive flags.

4.5.12.3 HDLC Memory Map

When configured to operate in HDLC mode, the IMP overlays the structure shown in Table 4-7 onto the protocol-specific area of that SCC parameter RAM. Refer to 2.8 MC68302 Memory Map for the placement of the three SCC parameter RAM areas and to Table 4-2 for the other parameter RAM values.

Table 4-8. HDLC-Specific Parameter RAM

Address	Name	Width	Description
SCC Base + 9C SCC Base + 9E SCC Base + A0 # SCC Base + A2 # SCC Base + A4 SCC Base + A6	RCRC_L RCRC_H C_MASK_L C_MASK_H TCRC_L TCRC_H	Word Word Word Word Word Word	Temp Receive CRC Low Temp Receive CRC High Constant ($F0B8 16-Bit CRC, $DEBB 32-Bit CRC) Constant ($XXXX 16-Bit CRC, $20E3 32-Bit CRC) Temp Transmit CRC Low Temp Transmit CRC High
SCC Base + A8 # SCC Base + AA # SCC Base + AC # SCC Base + AE # SCC Base + B0 #	DISFC CRCEC ABTSC NMARC RETRC	Word Word Word Word Word	Discard Frame Counter CRC Error Counter Abort Sequence Counter Nonmatching Address Received Counter Frame Retransmission Counter
SCC Base + B2 # SCC Base + B4	MFLR MAX_cnt	Word Word	Max Frame Length Register Max_Length Counter
SCC Base + B6 # SCC Base + B8 # SCC Base + BA # SCC Base + BC # SCC Base + BE #	HMASK HADDR1 HADDR2 HADDR3 HADDR4	Word Word Word Word Word	User-Defined Frame Address Mask User-Defined Frame Address User-Defined Frame Address User-Defined Frame Address User-Defined Frame Address

Initialized by the user (M68000 core).

NOTE

An incorrect initialization of C_MASK may be used to “force” receive CRC errors for software testing purposes. The transmit CRC will not be affected.

4.5.12.4 HDLC Programming Model

The M68000 core configures each SCC to operate in one of four protocols by the MODE1–MODE0 bits in the SCC mode register (SCM). MODE1–MODE0 = 00 selects HDLC mode.

The HDLC controller uses the same data structure as the UART, BISYNC, and DDCMP controllers. This data structure supports multibuffer operation and address comparisons.

The receive errors (overrun, nonoctet aligned frame, $\overline{CD}$ lost, aborted frame, and CRC error) are reported through the receive BD. The transmit errors (underrun and $\overline{CTS}$ lost) are reported through the transmit BD. An indication about the status of the lines (idle, $\overline{CD}$, and $\overline{CTS}$) is reported through the SCC status register (SCCS), and a maskable interrupt is generated upon a status change in any one of those lines.

4.5.12.5 HDLC Command Set

The following commands are issued to the command register.

STOP TRANSMIT Command

After a hardware or software reset and the enabling of the channel in the SCC mode register, the channel is in the transmit enable mode and starts polling the first BD in the table approximately every eight or sixteen transmit clocks as determined by the FLG bit in the HDLC mode register.

The channel STOP TRANSMIT command disables the transmission of frames on the transmit channel. If this command is received by the HDLC controller during frame transmission, transmission of that frame is aborted after the contents of the FIFO are transmitted (up to four words). The TBD# is not advanced. No new BD is accessed, and no new frames are transmitted for this channel. The transmitter will transmit an abort sequence (if the command was given during frame transmission) and then begin to transmit flags or idles as indicated by the HDLC mode register. The abort sequence on transmit is a zero followed by seven ones (01111111).

This command is useful for performing frame retransmission. The M68000 core may issue the STOP TRANSMIT command, reorganize the transmit BD table, and issue the RESTART TRANSMIT command. The STOP TRANSMIT command may also be used in the X.25 protocol to send a reject frame or a link reset command.

The STOP TRANSMIT command must be issued before the SCC mode register is used to disable the transmitter if the transmitter is to be re-enabled at a later time.

RESTART TRANSMIT Command

The RESTART TRANSMIT command re-enables the transmission of characters on the transmit channel. This command is expected by the HDLC controller after a STOP TRANSMIT command, after a STOP TRANSMIT command and disabling the channel in its SCC mode register, or after transmitter error (underrun or $\overline{CTS}$ lost when no automatic frame retransmission is performed). The HDLC controller will resume transmission from the current transmitter BD (TBD#) in the channel's transmit BD table.

If the transmitter is being re-enabled, the RESTART TRANSMIT command must be used and should be followed by the enabling of the transmitter in the SCC mode register.

ENTER HUNT MODE Command

After a hardware or software reset and the enabling of the channel by its SCC mode register, the channel is in the receive enable mode and will use the first BD in the table.

The ENTER HUNT MODE command is generally used to force the HDLC receiver to abort reception of the current frame, generate an RXB interrupt (if enabled) as the buffer is closed, and enter the hunt mode. In the hunt mode, the HDLC controller continually scans the input data stream for the flag sequence. After receiving the command, the current receive buffer is closed, and the CRC is reset. Further frame reception will use the next BD.

If an enabled receiver has been disabled by clearing ENR in the SCC mode register), the ENTER HUNT MODE command must be given to the channel before setting ENR again. Subsequent frames will then be received, starting with the next BD.

4.5.12.6 HDLC Address Recognition

Each HDLC controller has five 16-bit registers for address recognition: one mask register and four address registers (HMASK, HADDR1, HADDR2, HADDR3, and HADDR4). The HDLC controller reads the frame's address from the HDLC receiver, checks it against the four address register values, and then masks the result with the user-defined HMASK. A one in HMASK represents a bit position for which address comparison should occur; a zero represents a masked bit position. Upon an address match, the address and the data following are written into the data buffers. When the addresses are not matched and the frame is error free, the nonmatching address received counter (NMARC) is incremented.

NOTE

For 8-bit addresses, mask out the eight high-order bits in the HMASK register.

Examples of 16- and 8-bit HDLC address recognition are shown in Figure 4-25.

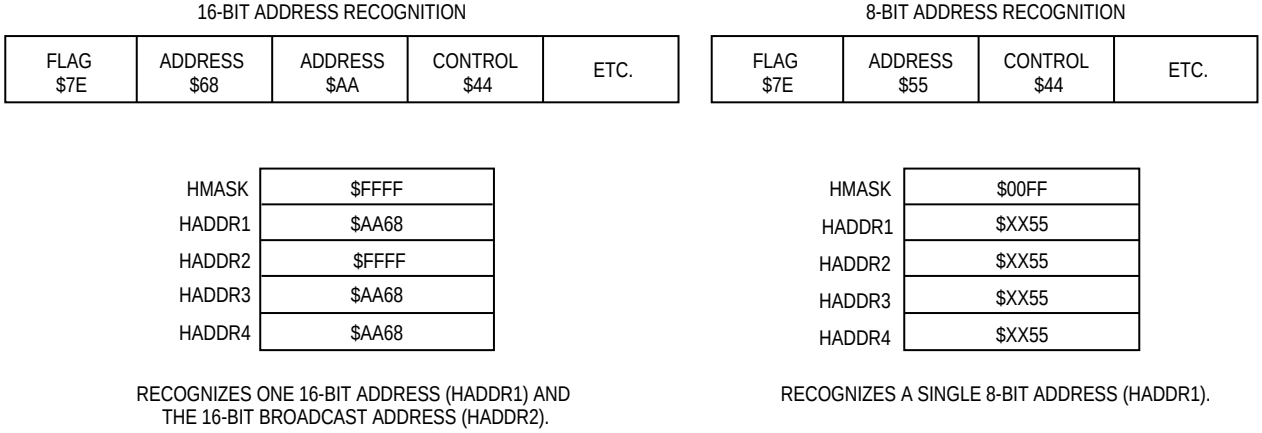


Figure 4-25. HDLC Address Recognition Examples

4.5.12.7 HDLC Maximum Frame Length Register (MFLR)

The HDLC controller checks the length of an incoming HDLC frame against the user-defined value given in this 16-bit register. If this limit is exceeded, the remainder of the incoming HDLC frame is discarded, and the LG (Rx frame too long) bit is set in the last BD belonging to that frame. The HDLC controller waits to the end of the frame and reports the frame status

and the frame length in the last BD. MFLR is defined as all the in-frame bytes between the opening flag and the closing flag (address, control, data, and CRC). MAX_CNT is a temporary downcounter used to track the frame length.

4.5.12.8 HDLC Error-Handling Procedure

The HDLC controller reports frame reception and transmission error conditions using the channel BDs, the error counters, and the HDLC event register. The modem interface lines can also be directly monitored in the SCC status register.

Transmission Errors:

1. Transmitter Underrun. When this error occurs, the channel terminates buffer transmission, closes the buffer, sets the underrun (UN) bit in the BD, and generates the TXE interrupt (if enabled). The channel will resume transmission after the reception of the RESTART TRANSMIT command. The transmit FIFO size is four words.
2. Clear-To-Send Lost (Collision) During Frame Transmission. When this error occurs and the channel is not programmed to control this line with software, the channel terminates buffer transmission, closes the buffer, sets the CTS lost (CT) bit in the BD, and generates the TXE interrupt (if enabled). The channel will resume transmission after the RESTART TRANSMIT command is given.

NOTE

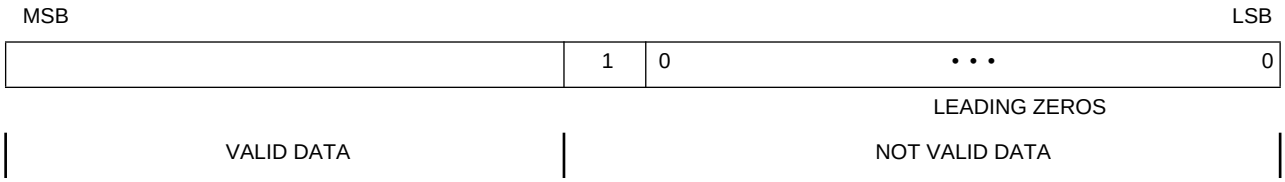
If this error occurs on the first or second buffer of the frame and the retransmit enable (RTE) bit in the HDLC mode register is set, the channel will retransmit the frame when the $\overline{\text{CTS}}$ line becomes active again. When using this feature, users should design transmit frames to fit within two buffers or less. When working in ISDN mode with D-channel collision possibility, to ensure the retransmission method functions properly, the first and second data buffers should contain more than 10 bytes of data if multiple buffers per frame are used. (Small frames consisting of a single buffer are not subject to this requirement). The channel will also increment the retransmission counter (RETRC).

Reception Errors:

1. Overrun Error. The HDLC controller maintains an internal three-word FIFO for receiving data. The CP begins programming the SDMA channel (if the data buffer is in external memory) and updating the CRC when the first word is received in the FIFO. When a receive FIFO overrun occurs, the channel writes the received data byte to the internal FIFO over the previously received byte. The previous data byte and the frame status are lost. Then the channel closes the buffer with the overrun (OV) bit in the BD set and generates the RXF interrupt (if enabled). The receiver then enters the hunt mode.
   Even if the overrun occurs during a frame whose address is not matched in the address recognition logic, a BD of length two will be opened to report the overrun, and the RXB interrupt will be generated (if enabled).
2. Carrier Detect Lost During Frame Reception. When this error occurs and the channel

is not programmed to control this line with software, the channel terminates frame reception, closes the buffer, sets the carrier detect lost (CD) bit in the BD, and generates the RXF interrupt (if enabled). This error has the highest priority. The rest of the frame is lost, and other errors are not checked in that frame. The receiver then enters the hunt mode.

3. Abort Sequence. An abort sequence is detected by the HDLC controller when seven or more consecutive ones are received while receiving a frame. When this error occurs, the channel closes the buffer by setting the Rx abort sequence (AB) bit in the BD and generates the RXF interrupt (if enabled). The channel also increments the abort sequence counter (ABTSC). The receiver then enters hunt mode immediately. The CRC and nonoctet error status conditions are not checked on aborted frames. The receiver then enters hunt mode.
4. Nonoctet Aligned Frame. When this error occurs, the channel writes the received data to the data buffer, closes the buffer, sets the Rx nonoctet aligned frame (NO) bit in the BD, and generates the RXF interrupt (if enabled). The CRC error status should be disregarded on nonoctet frames. After a nonoctet aligned frame is received, the receiver enters hunt mode. (An immediately following back-to-back frame will be received.) The nonoctet data may be derived from the last word in the data buffer as follows:



Consistent with other HDLC operation, the MSB is the first bit received in this word, and the low-order valid data bit is the last.

5. CRC Error. When this error occurs, the channel writes the received CRC to the data buffer, closes the buffer, sets the CR bit in the BD, and generates the RXF interrupt (if enabled). The channel also increments the CRC error counter (CRCEC). After receiving a frame with a CRC error, the received enters hunt mode. (An immediately following back-to-back frame will be received.) CRC checking cannot be disabled, but the CRC error may be ignored if checking is not required.

Error Counters

The CP maintains five 16-bit (modulo - 2**16) error counters for each HDLC controller. They can be initialized by the user when the channel is disabled. The counters are as follows:

DISFC—Discarded Frame Counter (error-free frames but no free buffers)
CRCEC—CRC Error Counter (includes frames not addressed to the user or frames received in the BSY condition, but does not include overrun errors)
ABTSC—Abort Sequence Counter
NMARC—Nonmatching Address Received Counter (error-free frames only)
RETRC—Frame Retransmission Counter (due to collision)

4.5.12.9 HDLC Mode Register

Each SCC mode register is a 16-bit, memory-mapped, read-write register that controls the SCC operation. The term HDLC mode register refers to the protocol-specific bits (15–6) of

the SCC mode register when that SCC is configured for HDLC. The read-write HDLC mode register is cleared by reset.

15	14	13	12	11	10	9	8	7	6	5 … 0
NOF3	NOF2	NOF1	NOF0	C32	FSE	—	RTE	FLG	ENC	COMMON SCC MODE BITS

NOF3–NOF0—Minimum Number of Flags between Frames or before Frames (0 to 15 Flags)

If NOF3–NOF0 = 0000, then no flags will be inserted between frames. Thus, the closing flag of one frame will be followed immediately by the opening flag of the next frame in the case of back-to-back frames.

C32—CRC16/CRC32

0 = 16-bit CCITT CRC ($X^{16} + X^{12} + X^5 + 1$)
1 = 32-bit CCITT CRC ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X^1 + 1$)

FSE—Flag Sharing Enable

0 = Normal operation
1 = If NOF3–NOF0 = 0000, then a single shared flag is transmitted between back- to-back frames. Other values of NOF3–NOF0 are decremented by one when FSE is set. This is useful in Signaling System #7 applications.

Bit 9—Reserved for future use.

RTE—Retransmit Enable

0 = No automatic retransmission will be performed.
1 = Automatic retransmit enabled

Automatic retransmission occurs if a $\overline{\text{CTS}}$ lost condition happens on the first or second buffer of the frame. See 4.5.12.8 HDLC Error-Handling Procedure.

FLG—Transmit Flags/Idles between Frames and Control the RTS Pin

0 = Send ones between frames; $\overline{\text{RTS}}$ is negated between frames. If NOF–NOF0 is greater than zero, $\overline{\text{RTS}}$ will be negated for a multiple of eight transmit clocks. The HDLC controller can transmit ones in both the NRZ and NRZI data encoding formats. The CP polls the Tx BD ready bit every 16 transmit clocks.
1 = Send flags between frames. $\overline{\text{RTS}}$ is always asserted. The CP polls the Tx BD ready bit every eight transmit clocks.

NOTE

This bit may be dynamically modified. If toggled from a one to a zero between frames, a maximum of two additional flags will be transmitted before the idle condition will begin. Toggling FLG will never result in partial flags being transmitted.

ENC—Data Encoding Format

0 = Non-return to zero (NRZ). A one is a high level; a zero is a low level.
1 = Non-return to zero inverted (NRZI). A one is represented by no change in the level; a zero is represented by a change in the level. The receiver decodes NRZI, but a clock must be supplied. The transmitter encodes NRZI. During an idle condition, with the FLG bit cleared, the line will be forced to a high state.

COMMON SCC MODE BITS—See 4.5.3 SCC Mode Register (SCM) for a description of the DIAG1, DIAG0, ENR, ENT, MODE1, and MODE0 bits.

4.5.12.10 HDLC Receive Buffer Descriptor (Rx BD)

The HDLC controller uses the Rx BD to report information about the received data for each buffer. The Rx BD is shown in Figure 4-26.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET + 0	E	X	W	I	L	F	—	—	—	—	LG	NO	AB	CR	OV	CD
OFFSET + 2	DATA LENGTH															
OFFSET + 4	RX BUFFER POINTER (24-bits used, upper 8 bits must be 0)															
OFFSET +6																

Figure 4-26. HDLC Receive Buffer Descriptor

An example of the HDLC receive process is shown in Figure 4-27. This shows the resulting state of the Rx BDs after receipt of a complete frame spanning two receive buffers and a second frame with an unexpected abort sequence. The example assumes that MRBLR = 8 in the SCC parameter RAM.

The first word of the Rx BD contains control and status bits. Bits 15–10 are written by the user before the buffer is linked to the Rx BD table, and bits 5–0 are set by the CP following frame reception. Bit 15 is set by the M68000 core when the buffer is available to the HDLC controller; it is cleared by the HDLC controller when the buffer is full.

E—Empty

0 = The data buffer associated with this BD has been filled with received data, or data reception has been aborted due to an error condition. The M68000 core is free to examine or write to any fields of the BD.
1 = The data buffer associated with the BD is empty. This bit signifies that the BD and its associated buffer are available to the HDLC controller. The M68000 core should not write to any fields of this BD after it sets this bit. The empty bit will remain set while the HDLC controller is currently filling the buffer with received data.

X—External Buffer

0 = The buffer associated with this BD is in internal dual-port RAM.
1 = The buffer associated with this BD is in external memory.

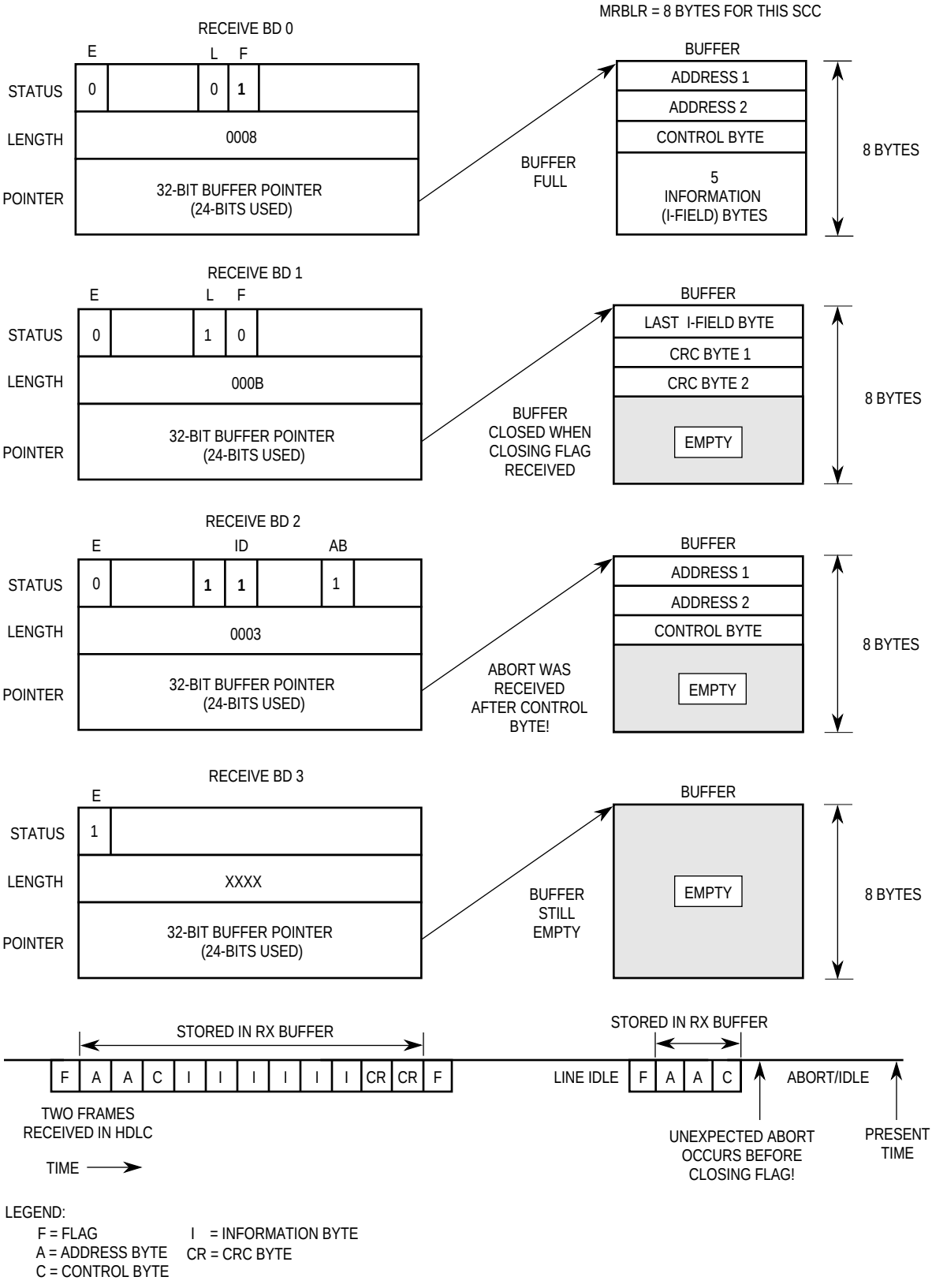


Figure 4-27. HDLC Receive BD Example

W—Wrap (Final BD in Table)

0 = This is not the last BD in the Rx BD table.
1 = This is the last BD in the Rx BD table. After this buffer has been used, the HDLC controller will receive incoming data into the first BD in the table.

NOTE

The user is required to set the wrap bit in one of the first eight BDs; otherwise, errant operation may occur.

I—Interrupt

0 = The RXB bit is not set after this buffer has been used, but RXF operation remains unaffected.
1 = The RXB or RXF bit in the HDLC event register will be set when this buffer has been used by the HDLC controller, which can cause an interrupt.

The following status bits are written by the HDLC controller after the received data has been placed into the associated data buffer.

L—Last in Frame

This bit is set by the HDLC controller when this buffer is the last in a frame. This implies the reception of a closing flag or reception of an error, in which case one or more of the CD, OV, AB, and LG bits are set. The HDLC controller will write the number of frame octets to the data length field.

0 = This buffer is not the last in a frame.
1 = This buffer is the last in a frame.

F—First in Frame

This bit is set by the HDLC controller when this buffer is the first in a frame.

0 = The buffer is not the first in a frame.
1 = The buffer is the first in a frame.

Bits 9–6—Reserved for future use.

LG—Rx Frame Length Violation.

A frame length greater than the maximum defined for this channel was recognized (only the maximum-allowed number of bytes (MFLR) is written to the data buffer). This event will not be reported until the Rx BD is closed and the RXF bit is set, after receipt of the closing flag. The actual number of bytes received between flags is written to the data length field of this BD.

NO—Rx Nonoctet Aligned Frame

A frame that contained a number of bits not exactly divisible by eight was received.

AB—Rx Abort Sequence

A minimum of seven consecutive ones was received during frame reception.

CR—Rx CRC Error

This frame contains a CRC error.

OV—Overrun

A receiver overrun occurred during frame reception.

CD—Carrier Detect Lost

The carrier detect signal was negated during frame reception. This bit is valid only when working in NMSI mode.

Data Length

The data length is the number of octets written to this BD's data buffer by the HDLC controller. It is written by the CP once as the BD is closed.

When this BD is the last BD in the frame (L = 1), the data length contains the total number of frame octets (including any previous linked receive data buffers and two or four bytes for the CRC) in the frame. This behavior is useful for determining the total number of octets received, even if MFLR was exceeded.

NOTE

The actual amount of memory allocated for this buffer should be even and greater than or equal to the contents of maximum receive buffer length register (MRBLR).

Rx Buffer Pointer

The receive buffer pointer, which always points to the first location of the associated data buffer, may reside in either internal or external memory.

NOTE

The Rx buffer pointer must be even, and the upper 8 bits must of the pointer must be zero for the function codes to operate correctly.

4.5.12.11 HDLC Transmit Buffer Descriptor (Tx BD)

Data is presented to the HDLC controller for transmission on an SCC channel by arranging it in buffers referenced by the channel's Tx BD table. The HDLC controller confirms transmission (or indicates error conditions) using the BDs to inform the M68000 core that the buffers have been serviced. The Tx BD is shown in Figure 4-28.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET + 0	R	X	W	I	L	TC	—	—	—	—	—	—	—	—	UN	CT
OFFSET + 2	DATA LENGTHTX BUFFER POINTER (24-bits used, upper 8 bits must be 0)															
OFFSET + 4																
OFFSET + 6																

Figure 4-28. HDLC Transmit Buffer Descriptor

The first word of the Tx BD contains status and control bits. Bits 15–10 are prepared by the user before transmission; bits 1–0 are set by the HDLC controller after the buffer has been transmitted. Bit 15 is set by the user when the buffer and BD have been prepared and is cleared by the HDLC controller after the frame has been transmitted.

R—Ready

0 = This buffer is not currently ready for transmission. The user is free to manipulate this BD (or its associated buffer). The HDLC controller clears this bit after the buffer has been fully transmitted or after an error condition has been encountered.
1 = The data buffer, which has been prepared for transmission by the user, has not yet transmitted. No fields of this BD may be written by the user once this bit is set.

X—External Buffer

0 = The buffer associated with this BD is in internal dual-port RAM.
1 = The buffer associated with this BD is in external memory.

W—Wrap (Final BD in Table)

0 = This is not the last BD in the Tx BD table.
1 = This is the last BD in the Tx BD table. After this buffer has been used, the HDLC controller will transmit data from the first BD in the table.

NOTE

The user is required to set the wrap bit in one of the first eight BDs; otherwise, errant behavior may occur.

I—Interrupt

0 = No interrupt is generated after this buffer has been serviced.
1 = Either TXB or TXE in the HDLC event register will be set when this buffer has been serviced by the HDLC controller, which can cause an interrupt.

L—Last

0 = This is not the last buffer in the frame.
1 = This is the last buffer in the current frame.

TC—Tx CRC

This bit is valid only when the last (L) bit is set.

0 = Transmit the closing flag after the last data byte. This setting can be used for testing purposes to send a “bad” CRC after the data.
1 = Transmit the CRC sequence after the last data byte.

Bits 9–2—Reserved for future use.

The following status bits are written by the HDLC controller after it has finished transmitting the associated data buffer.

UN—Underrun

The HDLC controller encountered a transmitter underrun condition while transmitting the associated data buffer.

CT—CTS Lost

CTS in NMSI mode or L1GR (layer-1 grant) in IDL/GCI mode was lost during frame transmission. If data from more than one buffer is currently in the FIFO when this error occurs, this bit will be set in the Tx BD that is currently open.

Data Length

The data length is the number of octets the HDLC controller should transmit from this BD's data buffer. It is never modified by the CP. The value of this field should be greater than zero.

Tx Buffer Pointer

The transmit buffer pointer, which contains the address of the associated data buffer, may be even or odd. The buffer may reside in either internal or external memory.

NOTE

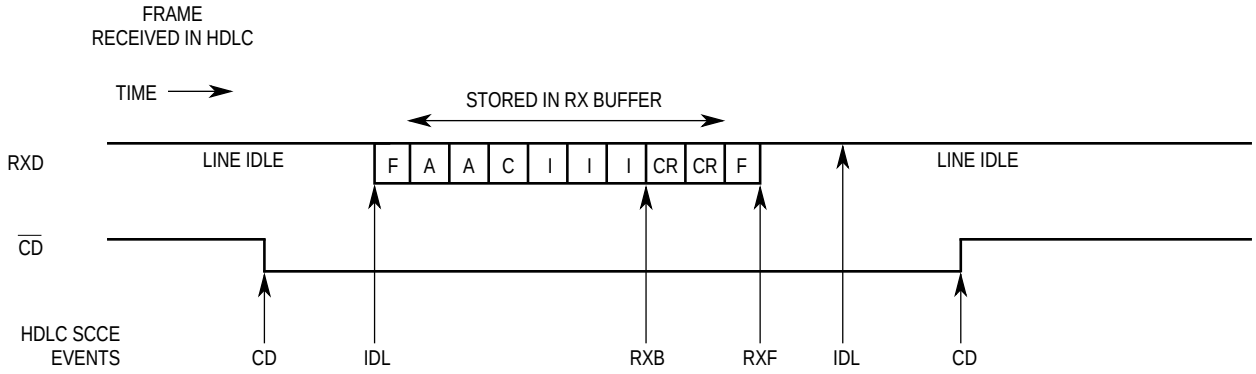
For correct operation of the function codes, the upper 8 bits of the pointer must be initialized to zero.

4.5.12.12 HDLC Event Register

The SCC event register (SCCE) is called the HDLC event register when the SCC is operating as an HDLC controller. It is an 8-bit register used to report events recognized by the HDLC channel and to generate interrupts. Upon recognition of an event, the HDLC controller sets its corresponding bit in the HDLC event register. Interrupts generated by this register may be masked in the HDLC mask register.

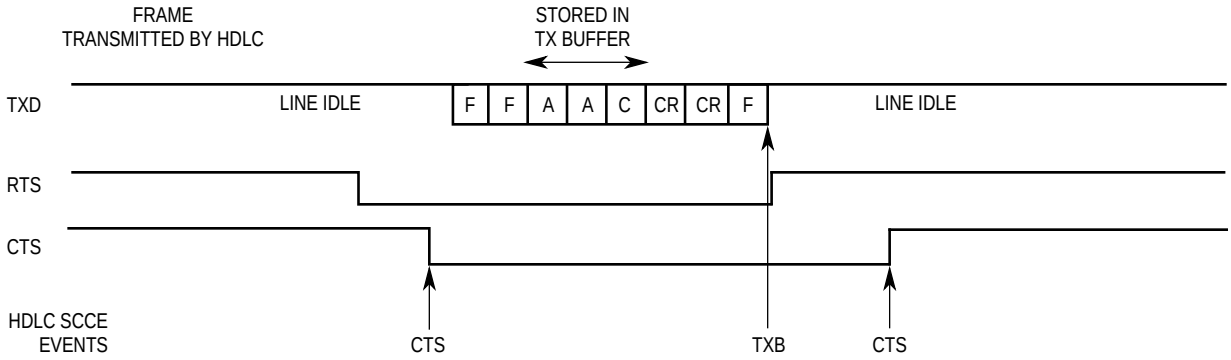
The HDLC event register is a memory-mapped register that may be read at any time. A bit is cleared by writing a one; writing a zero does not affect a bit's value. More than one bit may be cleared at a time. All unmasked bits must be cleared before the CP will clear the internal interrupt request. This register is cleared at reset.

An example of the timing of various events in the HDLC event register is shown in Figure 4-29.



NOTES:
1. RXB event assumes receive buffers are 6 bytes each.
2. The second IDL event occurs after 15 ones are received in a row.

LEGEND:
F = Flag A = Address byte C = Control byte I = Information byte CR = CRC byte



NOTE: TXB event shown assumes all three bytes were put into a single buffer.
Example shows one additional opening flag. This is programmable.

Figure 4-29. HDLC Interrupt Events Example

7	6	5	4	3	2	1	0
CTS	CD	IDL	TXE	RXF	BSY	TXB	RXB

CTS—Clear-To-Send Status Changed

A change in the status of the $\overline{CTS}$ line was detected on the HDLC channel. The SCC status register may be read to determine the current status.

CD—Carrier Detect Status Changed

A change in the status of the $\overline{CD}$ line was detected on the HDLC channel. The SCC status register may be read to determine the current status.

IDL—IDLE Sequence Status Changed

A change in the status of the serial line was detected on the HDLC channel. The SCC status register may be read to determine the current status.

TXE—Tx Error

An error ($\overline{\text{CTS}}$ lost or underrun) occurred on the transmitter channel.

RXF—Rx Frame

A complete frame has been received on the HDLC channel. This bit is set no sooner than two receive clocks after receipt of the last bit of the closing flag.

BSY—Busy Condition

A frame was received and discarded due to lack of buffers.

TXB—Tx Buffer

A buffer has been transmitted on the HDLC channel. This bit is set no sooner than when the second-to-last bit of the closing flag begins its transmission, if the buffer is the last in the frame. Otherwise, it is set after the last byte of the buffer has been written to the transmit FIFO.

RXB—Rx Buffer

A buffer has been received on the HDLC channel that was not a complete frame. This bit will only be set if the I bit in the Tx BD was set.

4.5.12.13 HDLC Mask Register

The SCC mask register (SCCM) is referred to as the HDLC mask register when the SCC is operating as an HDLC controller. It is an 8-bit read-write register that has the same bit formats as the HDLC event register. If a bit in the HDLC mask register is a one, the corresponding interrupt in the event register will be enabled. If the bit is zero, the corresponding interrupt in the event register will be masked. This register is cleared upon reset.

4.5.13 BISYNC Controller

The byte-oriented binary synchronous communication (BISYNC) protocol was originated by IBM for use in networking products. The three classes of BISYNC frames are transparent, non-transparent with header, and non-transparent without header (see Figure 4-30). The transparent mode in BISYNC allows full binary data to be transmitted, with any possible character pattern allowed. Each class of frame starts with a standard two octet synchronization pattern and ends with a block check code (BCC). The end of text character (ETX) is used to separate the text and BCC fields.

NON TRANSPARENT WITH HEADER

SYN1	SYN2	SOH	HEADER	STX	TEXT	ETX	BCC

NON TRANSPARENT WITHOUT HEADER

SYN1	SYN2	STX	TEXT	ETX	BCC

TRANSPARENT

SYN1	SYN2	DLE	STX	TRANSPARENT TEXT	DLE	ETX	BCC

Figure 4-30. Typical BISYNC Frames

The bulk of the frame is divided into fields whose meaning depends on the frame type. The BCC is either a 16-bit CRC (CRC-16) format if 8-bit characters are used or a longitudinal check (a sum check) in combination with vertical redundancy check (parity) if 7-bit characters are used. In transparent operation, to allow the BISYNC control characters to be present in the frame as valid text data, a special character (DLE) is defined, which informs the receiver that the character following the DLE is a text character, not a control character (from the control character table). If a DLE is transmitted as valid data, it must be preceded by a DLE character. This procedure is sometimes called byte-stuffing.

The physical layer of the BISYNC communications link must provide a means of synchronizing the receiver and transmitter, which is usually accomplished by sending at least one pair of synchronization characters prior to every frame.

BISYNC has the unusual property that a transmit underrun need not be an error. If an underrun occurs, the synchronization pattern is transmitted until data is once again ready to transmit. The receiver discards the additional synchronization characters as they are received, provided the V bit is set in the BISYNC-BISYNC SYNC register. In non-transparent operation, all synchronization characters (SYNCs) are discarded if the V bit is set in the BISYNC-BISYNC SYNC register. In transparent operation, all DLE-SYNC pairs are discarded. (Note that correct operation in this case assumes that, on the transmit side, the underrun does not occur between the DLE and its following character, a failure mode prevented in the MC68302.)

By appropriately setting the SCC mode register, any of the SCC channels may be configured to function as a BISYNC controller. The BISYNC controller handles the basic functions of the BISYNC protocol in normal mode and in transparent mode.

The SCC in BISYNC mode can work with IDL, GCI (IOM2), PCM highway, or NMSI interfaces. When the SCC in BISYNC mode is used with a modem interface (NMSI), the SCC outputs are connected directly to the external pins. The modem interface uses seven dedicated pins: transmit data (TXD), receive data (RXD) receive clock (RCLK), transmit clock (TCLK), carrier detect ($\overline{\text{CD}}$), clear to send ($\overline{\text{CTS}}$), and request to send ($\overline{\text{RTS}}$). Other modem lines can be supported using the parallel I/O pins.

The BISYNC controller consists of separate transmit and receive sections whose operations are asynchronous with the M68000 core and may be either synchronous or asynchronous with respect to the other SCCs. Each clock can be supplied from either the internal baud

rate generator or from external pins. More information on the baud rate generator is available in 4.5.2 SCC Configuration Register (SCON).

- Flexible Data Buffers
- Eight Control Character Recognition Registers
- Automatic SYNC1 and SYNC2 Detection
- SYNC/DLE Stripping and Insertion
- CRC16 and LRC Generation/Checking
- Parity (VRC) Generation/Checking
- Supports BISYNC Transparent Operation (Use of DLE Characters)
- Supports Promiscuous (Totally Transparent) Reception and Transmission
- Maintains Parity Error Counter
- External SYNC Support
- Reverse Data Mode
- Four Commands

4.5.13.1 Bisync Channel frame Transmission Processing

The BISYNC transmitter is designed to work with almost no intervention from the M68000 core. When the M68000 core enables the BISYNC transmitter, it will start transmitting SYN1–SYN2 pairs (located in the data synchronization register) or idle as programmed in the BISYNC mode register. The BISYNC controller polls the first buffer descriptor (BD) in the transmit channel's BD table. When there is a message to transmit, the BISYNC controller will fetch the data from memory and start transmitting the message (after first transmitting the SYN1–SYN2 pair).

When a BD's data has been completely transmitted, the last in message (L) bit is checked. If both the L bit and transmit BCS bit are set in that BD, the BISYNC controller will append the CRC16/LRC. Subsequently, the BISYNC controller writes the message status bits into the BD and clears the ready bit. It will then start transmitting SYN1–SYN2 pairs or IDLEs as programmed in the BISYNC mode register. When the end of the current BD has been reached and the last bit is not set (working in multibuffer mode), only the ready bit is cleared. In both cases, an interrupt is issued according to the interrupt (I) bit in the BD. By appropriately setting the I bit in each BD, interrupts can be generated after the transmission of each buffer, a specific buffer, or each block. The BISYNC controller will then proceed to the next BD in the table.

If no additional buffers have been presented to the BISYNC controller for transmission, an in-frame underrun is detected, and the BISYNC controller begins transmitting SYNCs. If the BISYNC controller was in transparent mode, the BISYNCs controller transmits DLE-SYNC pairs. This case is not an error. However, if an underrun occurs within a buffer, the BISYNC controller will transmit a SYN1–SYN2 pair followed by either SYNCs or idles according to the SYNF bit in the BISYNC mode register. This case is an underrun error and is described further in 4.5.13.8 BISYNC Error-Handling Procedure.

Characters are included in the block check sequence (BCS) calculation on a per-buffer basis. Each buffer can be independently programmed to be included or excluded from the BCS calculation, and any characters to be excluded from the BCS calculation must reside in a separate buffer. The BISYNC controller can reset the BCS generator before transmitting a specific buffer. When functioning in transparent mode, the BISYNC controller automatically inserts a DLE before transmitting a DLE character. In this case, only one DLE is used in the calculation of the BCS.

The IMP may also be used to transmit characters in a promiscuous (totally transparent) mode. See 4.5.16 Transparent Controller.

4.5.13.2 Bisync Channel Frame Reception Processing

Although the BISYNC receiver is designed to work with almost no intervention from the M68000 core, it allows user intervention on a per-byte basis if necessary. The BISYNC receiver can perform CRC16, longitudinal redundancy check (LRC), or vertical redundancy check (VRC) checking, SYNC stripping in normal mode, DLE-SYNC stripping and stripping of the first DLE in DLE-DLE pairs in transparent mode, and control character recognition. A control character is one belonging to the control characters shown in Figure 4-31.

When the M68000 core enables the BISYNC receiver, it will enter hunt mode. In this mode, as data is shifted into the receiver shift register one bit at a time, the contents of the register are compared to the contents of the SYN1–SYN2 fields in the data synchronization register. If the two are not equal, the next bit is shifted in, and the comparison is repeated. When the registers match, the hunt mode is terminated, and character assembly begins. The BISYNC controller is now character synchronized and will perform SYNC stripping and message reception. The BISYNC controller will revert to the hunt mode when it is issued the ENTER HUNT MODE command, upon recognition of some error condition, or upon reception of an appropriately defined control character.

When receiving data, the BISYNC controller updates the BCS bit (CR) in the BD for every byte transferred. When the data buffer has been filled, the BISYNC controller clears the empty (E) bit in the BD and generates an interrupt if the interrupt (I) bit in the BD is set. If the incoming data exceeds the length of the data buffer, the BISYNC controller will fetch the next BD in the table and, if it is empty, will continue to transfer data to this BD's associated data buffer.

When a BCS is received, it is checked and written to the data buffer. The BISYNC controller sets the last bit, writes the message status bits into the BD, and clears the empty bit. Then it generates a maskable interrupt, indicating that a block of data has been received and is in memory. Note that the SYNC in the nontransparent mode or DLE-SYNC pairs in the transparent mode (i.e., an underrun condition) are not included in the BCS calculations.

The IMP may also be used to receive characters in a promiscuous (totally transparent) mode. See 4.5.16 Transparent Controller.

4.5.13.3 Bisync Memory Map

When configured to operate in BISYNC mode, the IMP overlays the structure listed in Table 4-8 onto the protocol-specific area of that SCC parameter RAM. Refer to 2.8 MC68302

Memory Map for the placement of the three SCC parameter RAM areas and Table 4-5 for the other parameter RAM values.

Table 4-9. BISYNC Specific Parameter RAM

Address	Name	Width	Description
SCC Base + 9C	RCRC	Word	Temp Receive CRC
SCC Base + 9E	CRCC	Word	CRC Constant
SCC Base + A0 #	PRCRC	Word	Preset Receiver CRC 16/LRC
SCC Base + A2	TCRC	Word	Temp Transmit CRC
SCC Base + A4 #	PTCRC	Word	Preset Transmitter CRC 16/LRC
SCC Base + A6	RES	Word	Reserved
SCC Base + A8	RES	Word	Reserved
SCC Base + AA #	PAREC	Word	Receive Parity Error Counter
SCC Base + AC #	BSYNC	Word	BISYNC SYNC Character
SCC Base + AE #	BDLE	Word	BISYNC DLE Character
SCC Base + B0 #	CHARACTER1	Word	CONTROL Character 1
SCC Base + B2 #	CHARACTER2	Word	CONTROL Character 2
SCC Base + B4 #	CHARACTER3	Word	CONTROL Character 3
SCC Base + B6 #	CHARACTER4	Word	CONTROL Character 4
SCC Base + B8 #	CHARACTER5	Word	CONTROL Character 5
SCC Base + BA #	CHARACTER6	Word	CONTROL Character 6
SCC Base + BC #	CHARACTER7	Word	CONTROL Character 7
SCC Base + BE #	CHARACTER8	Word	CONTROL Character 8

Initialized by the user (M68000 core).

The M68000 core configures each SCC to operate in one of four protocols by the MODE1–MODE0 bits in the SCC mode register. MODE1–MODE0 = 11 selects the BISYNC mode of operation. The SYN1–SYN2 synchronization characters are programmed in the data synchronization register (see 4.5.4 SCC Data Synchronization Register (DSR)).

The BISYNC controller uses the same basic data structure as the other protocol controllers. Receive and transmit errors are reported through their respective BDs. The status of the line is reflected in the SCC status register, and a maskable interrupt is generated upon each status change.

There are two basic ways of handling the BISYNC channels. First, data may be inspected on a per-byte basis, with the BISYNC controller interrupting the M68000 core upon receipt of every byte of data. Second, the BISYNC controller may be operated so that software is only necessary for handling the first two to three bytes of data; subsequent data (until the end of the block) can be handled by the BISYNC controller without interrupting the M68000 core. See 4.5.13.14 Programming the BISYNC Controllers for more information.

4.5.13.4 BISYNC Command Set

The following commands are issued to the command register.

STOP TRANSMIT Command

After a hardware or software reset and the enabling of the channel using the SCC mode register, the channel is in the transmit enable mode and starts polling the first BD in the table approximately every eight transmit clocks.

The STOP TRANSMIT command aborts transmission after the contents of the FIFO are transmitted (up to three bytes) without waiting until the end of the buffer is reached. The TBD# is not advanced. SYNC characters consisting of SYNC-SYNC or DLE-SYNC pairs (according to the transmitter mode) will be continually transmitted until transmission is re-enabled by issuing the RESTART TRANSMIT command. The STOP TRANSMIT com-

mand may be used when it is necessary to abort transmission and transmit an EOT control sequence. The EOT sequence should be the first buffer presented to the BISYNC controller for transmission after re-enabling transmission.

The STOP TRANSMIT command must be issued before the SCC mode register is used to disable the transmitter if the transmitter is to be re-enabled at a later time.

NOTE

The BISYNC controller will remain in the transparent or normal mode after receiving the STOP TRANSMIT or RESTART TRANSMIT commands.

RESTART TRANSMIT Command

The RESTART TRANSMIT command is used to begin or resume transmission from the current Tx BD number (TBD#) in the channel's Tx BD table. When this command is received by the channel, it will start polling the ready bit in this BD. This command is expected by the BISYNC controller after a STOP TRANSMIT command, after the STOP TRANSMIT command and the disabling of the channel in its mode register, or after a transmitter error (underrun or CTS lost) occurs.

If the transmitter is being re-enabled, the RESTART TRANSMIT command must be used and should be followed by the enabling of the transmitter in the SCC mode register.

RESET BCS CALCULATION Command

The RESET BCS CALCULATION command resets the receive BCS accumulator immediately. For example, it may be used to reset the BCS after recognizing a control character, signifying that a new block is commencing (such as SOH).

ENTER HUNT MODE Command

After a hardware or software reset and the enabling of the channel in the SCC mode register, the channel is in the receive enable mode and will use the first BD in the table.

The ENTER HUNT MODE command is used to force the BISYNC controller to abort reception of the current block, generate an RX interrupt (if enabled) as the buffer is closed, and enter the hunt mode. In hunt mode, the BISYNC controller continually scans the input data stream for the SYN1–SYN2 sequence as programmed in the data synchronization register. After receiving the command, the current receive buffer is closed, and the BCS is reset. Message reception continues using the next BD.

If an enabled receiver has been disabled (by clearing ENR in the SCC mode register), the ENTER HUNT MODE command must be given to the channel before setting ENR again.

4.5.13.5 BISYNC Control Character Recognition

The BISYNC controller can recognize special control characters. These characters are used to “customize” the BISYNC protocol implemented by the BISYNC controller and may be used to aid its operation in a DMA-oriented environment. Their main use is for receive buffers longer than one byte. In single-byte buffers, each byte can easily be inspected, and control character recognition should be disabled.

The purpose of the control characters table is to enable automatic recognition (by the BISYNC controller) of the end of the current block. See 4.5.13.14 Programming the BISYNC Controllers for more information. Since the BISYNC controller imposes no restrictions on the format of the BISYNC blocks, user software must respond to the received characters and inform the BISYNC controller of mode changes and certain protocol events (e.g., resetting the BCS). However, correct use of the control characters table allows the remainder of the block to be received without interrupting the user software.

Up to eight control characters may be defined. These characters inform the BISYNC controller that the end of the current block has been reached and whether a BCS is expected following this character. For example, the end of text (ETX) character implies both an end of block (ETB) and a BCS should be received. An enquiry (ENQ) character designates end of block without a subsequent BCS. All the control characters are written into the data buffer.

The BISYNC controller uses a table of 16-bit entries to support control character recognition. Each entry consists of the control character, an end-of-table bit, a BCS expected bit, and a hunt mode bit. The control characters table is shown in Figure 4-31. To disable the entire control characters table, write $8000 to the first table entry.

	15	14	13	12	11	10	9	8	7 … 0
OFFSET + 0	E	B	H						CHARACTER1
OFFSET +2	E	B	H						CHARACTER2
OFFSET + 4	E	B	H						CHARACTER3
•									
•									
•									
OFFSET + E	E	B	H						CHARACTER8

Figure 4-31. BISYNC Control Characters Table

CHARACTER8–CHARACTER1—Control Character Value

These fields define control characters.

NOTE

When using 7-bit characters with parity, the parity bit should be included in the control character value.

E—End of Table

0 = This entry is valid. The lower eight bits will be checked against the incoming character.

1 = The entry is not valid. No valid entries exist beyond this entry.

NOTE

In tables with eight control characters, E should be zero in all eight positions.

B—BCS Expected

0 = The character is written into the receive buffer. The buffer is then closed.
1 = The character is written into the receive buffer. The receiver waits for one LRC or two CRC bytes of BCS and then closes the buffer. This should be used for ETB, ETX, and ITB.

NOTE

A maskable interrupt is generated after the buffer is closed.

H—Enter Hunt Mode

0 = The BISYNC controller will maintain character synchronization after closing this buffer.
1 = The BISYNC controller will enter hunt mode after closing the buffer. When the B bit is set, the controller will enter hunt mode after the reception of the BCS.

4.5.13.6 BSYNC-BISYNC SYNC Register

The 16-bit, memory-mapped, read-write BSYNC register is used to define the BISYNC stripping and insertion of the SYNC character. When an underrun occurs during message transmission, the BISYNC controller will insert SYNC characters until the next data buffer is available for transmission. When the BISYNC receiver is not in hunt mode and a SYN1 character has been received and discarded, the receiver will discard a SYNC character if the valid (V) bit is set.

NOTE

Normal Bisync operation requires that SYN1=SYN2=SYNC (and the V bit must be set in the BISYNC SYNC register).

When using 7-bit characters with parity, the parity bit should be included in the SYNC register value.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
V	0	0	0	0	0	0	0	SYNC							

4.5.13.7 BDLE-BISYNC DLE Register

The 16-bit, memory-mapped, read-write BDLE register is used to define the BISYNC stripping and insertion of the DLE character. When the BISYNC controller is in transparent mode and an underrun occurs during message transmission, the BISYNC controller inserts DLE-SYNC pairs until the next data buffer is available for transmission.

When the BISYNC receiver is in transparent mode and a DLE character is received, the receiver discards this character and excludes it from the BCS if the valid (V) bit is set. If the second (next) character is a SYNC character, the BISYNC controller discards it and ex-

cludes it from the BCS. If the second character is a DLE, the BISYNC controller will write it to the buffer and include it in the BCS. If the character is not a DLE or SYNC, the BISYNC controller will examine the control characters table and act accordingly. If the character is not in the table, the buffer will be closed with the DLE follow character error (DL) bit set. If the V bit is not set, the receiver will treat the character as a normal character.

NOTE

When using 7-bit characters with parity, the parity bit should be included in the DLE register value.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
V	0	0	0	0	0	0	0	DLE							

4.5.13.8 BISYNC Error-Handling Procedure

The BISYNC controller reports message reception and transmission error conditions using the channel BDs, the error counters, and the BISYNC event register. The modem interface lines can also be directly monitored in the SCC status register.

Transmission Errors:

1. Transmitter Underrun. When this error occurs, the channel terminates buffer transmission, closes the buffer, sets the underrun (UN) bit in the BD, and generates the TXE interrupt (if enabled). The channel resumes transmission after the reception of the RESTART TRANSMIT command. Underrun cannot occur between frames or during a DLE-XXX pair in transparent mode. The FIFO size is three bytes in BISYNC.
2. Clear-To-Send Lost During Message Transmission. When this error occurs and the channel is not programmed to control this line with software, the channel terminates buffer transmission, closes the buffer, sets the CTS lost (CT) bit in the BD, and generates the TXE interrupt (if enabled). The channel will resume transmission after the reception of the RESTART TRANSMIT command.

Reception Errors:

1. Overrun Error. The BISYNC controller maintains an internal three-byte FIFO for receiving data. The CP begins programming the SDMA channel (if the data buffer is in external memory) and updating the CRC when the first word is received into the FIFO. If a FIFO overrun occurs, the BISYNC controller writes the received data byte to the internal FIFO over the previously received byte. The previous character and its status bits are lost. Following this, the channel closes the buffer, sets the overrun (OV) bit in the BD, and generates the RX interrupt (if enabled). The receiver then enters hunt mode immediately.
2. Carrier Detect Lost During Message Reception. When this error occurs and the channel is not programmed to control this line with software, the channel terminates message reception, closes the buffer, sets the carrier detect lost (CD) bit in the BD, and generates the RX interrupt (if enabled). This error is the highest priority; the rest of the message is lost and no other errors are checked in the message. The receiver then enters hunt mode immediately.
3. Parity Error. When this error occurs, the channel writes the received character to the

buffer and sets the PR bit in the BD. The channel terminates message reception, closes the buffer, sets the PR bit in the BD, and generates the RX interrupt (if enabled). The channel also increments the parity error counter (PAREC), and the receiver then enters hunt mode immediately.

4. CRC Error. The channel updates the CRC error (CR) bit in the BD every time a character is received, with a byte delay (eight serial clocks) between the status update and the CRC calculation. When using control character recognition to detect the end of the block and cause the checking of the CRC that follows, the channel closes the buffer, sets the CR bit in the BD, and generates the RX interrupt (if enabled).

Error Counter

The CP main controller maintains one 16-bit (modulo–2**16) error counter for each BISYNC controller. It can be initialized by the user when the channel is disabled. The counter is as follows:

—PAREC—Parity Error Counter (on received characters)

4.5.13.9 BISYNC Mode Register

Each SCC mode register is a 16-bit, memory-mapped, read-write register that controls the SCC operation. The term BISYNC mode register refers to the protocol-specific bits (15–6) of the SCC mode register when that SCC is configured for BISYNC. The read-write BISYNC mode register is cleared by reset.

15	14	13	12	11	10	9	8	7	6	5 0
PM	EXSYN	NTSYN	REVD	BCS	—	RTR	RBCS	SYNF	ENC	COMMON SCC MODE BITS

PM—Parity Mode

0 = Odd Parity
1 = Even Parity

This bit is valid when the BCS bit is cleared. When odd parity is selected, the transmitter will count the number of ones in the 7-bit data character. If the total is not an odd number, then the parity bit is made equal to one to make an odd number of ones. Then, if the receiver counts an even number of ones, an error in transmission has occurred. In the same manner, for even parity, an even number must result from the calculation performed at both ends of the line.

EXSYN—External Sync Mode

When this mode is selected, the receiver expects external logic to indicate the beginning of the data field using the $\overline{\text{CD1}}$/L1SY1 pin, if SCC1 is used, and the $\overline{\text{CD2}}$ and $\overline{\text{CD3}}$ pins, respectively, if SCC2 or SCC3 are used in this mode. In this mode, there will be no carrier detect function for the SCC.

When the channel is programmed to work through the serial channels physical interface (IDL or GCI) and EXSYN is set, the layer-1 logic carries out the synchronization using the L1SY1 pin. In PCM mode, the L1SY1–L1SY0 pins are used.

In NMSI mode, the $\overline{\text{CD}}$ pins (and the $\overline{\text{CD}}$ timing) are used to synchronize the data. $\overline{\text{CD}}$ should be asserted on the second data bit of the frame when used as a sync.

If this bit is cleared, the BISYNC controller will look for the SYN1–SYN2 sequence in the data synchronization register.

NTSYN—No Transmit SYNC

When this bit is set, the SCC operates in a promiscuous, totally transparent mode. See 4.5.16 Transparent Controller for details.

REVD—Reverse DATA

When this bit is set, the receiver and transmitter will reverse the character bit order, transmitting the most significant bit first. This bit is valid in promiscuous mode.

BCS—Block Check Sequence

0 = LRC
For even LRC, the PRCRC and PTCRC preset registers in the BISYNC-specific parameter RAM should be initialized to zero before the channel is enabled. For odd LRC, the PRCRC and PTCRC registers should be initialized to ones. The LRC is formed by the Exclusive OR of each 7-bits of data (not including synchronization characters), and the parity bit is added after the final LRC calculation.

The receiver will check character parity when BCS is programmed to LRC and the receiver is not in transparent mode. The transmitter will transmit character parity when BCS is programmed to LRC and the transmitter is not in transparent mode. Use of parity in BISYNC assumes the use of 7-bit data characters.

1 = CRC16
The PRCRC and PTCRC preset registers should be initialized to a preset value of all zeros or all ones before the channel is enabled. In both cases, the transmitter sends the calculated CRC non-inverted, and the receiver checks the CRC against zero. Eight-bit characters (without parity) are configured when CRC16 is chosen. The CRC16 polynomial is as follows:

$$X^{16} + X^{15} + X^{2} + 1$$

Bit 10—Reserved for future use.

RTR—Receiver Transparent Mode

0 = The receiver is placed in normal mode with SYNC stripping and control character recognition operative.
1 = The receiver is placed in transparent mode. SYNCs, DLEs, and control characters are only recognized after a leading DLE character. The receiver will calculate the CRC16 sequence, even if programmed to LRC while in transparent mode. PRCRC should be first initialized to the CRC16 preset value before setting this bit.

RBCS—Receive Block Check Sequence

The BISYNC receiver internally stores two BCS calculations with a byte delay (eight serial clocks) between them. This enables the user to examine a received data byte and then decide whether or not it should be part of the BCS calculation. This is useful when control

character recognition and stripping is desired to be performed in software. The bit should be set (or reset) within the time taken to receive the following data byte. When this bit is reset, the BCS calculations exclude the latest fully received data byte. When RBCS is set, the BCS calculations continue normally.

0 = Disable receive BCS
1 = Enable receive BCS

SYNF—Transmit SYN1–SYN2 or IDLE between Messages and Control the RTS Pin

0 = Send ones between messages; $\overline{\text{RTS}}$ is negated between messages. The BISYNC controller can transmit ones in both NRZ and NRZI encoded formats.
1 = Send SYN1–SYN2 pairs between messages; $\overline{\text{RTS}}$ is always asserted.

ENC—Data Encoding Format

0 = Non-return to zero (NRZ). A one is a high level; a zero is a low level.
1 = Non-return to zero inverted (NRZI). A one is represented by no change in the level; a zero is represented by a change in the level. The receiver decodes NRZI, but a clock must be supplied. The transmitter encodes NRZI.

COMMON SCC MODE BITS—See 4.5.3 SCC Mode Register (SCM) for a description of the DIAG1, DIAG0, ENR, ENT, MODE1, and MODE0 bits.

4.5.13.10 BISYNC Receive Buffer Descriptor (Rx BD)

- The CP reports information about the received data for each buffer using BD. The Rx BD is shown in Figure 4-32. The CP closes the current buffer, generates a maskable interrupt, and starts to receive data into the next buffer after one of the following events:
- Receiving a user-defined control character
- Detecting an error
- Detecting a full receive buffer
- Issuing the ENTER HUNT MODE command

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET + 0	E	X	W	I	C	B	—	—	—	—	—	DL	PR	CR	OV	CD
OFFSET +2	DATA LENGTH															
OFFSET +4	RX BUFFER POINTER (24-bits used, upper 8 bits must be 0)															
OFFSET + 6																

Figure 4-32. BISYNC Receive Buffer Descriptor

The first word of the Rx BD contains control and status bits.

E—Empty

0 = The data buffer associated with this BD has been filled with received data, or data reception has been aborted due to an error condition. The M68000 core is free to examine or write to any fields of this BD.
1 = The data buffer associated with this BD is empty. This bit signifies that the BD and its associated buffer are available to the CP. After it sets this bit, the M68000 core

should not write to any fields of this BD when this bit is set. The empty bit will remain set while the CP is currently filling the buffer with received data.

X—External Buffer

0 = The buffer associated with this BD is in internal dual-port RAM.
1 = The buffer associated with this BD is in external memory.

W—Wrap (Final BD in Table)

0 = This is not the last BD in the Rx BD table.
1 = This is the last BD in the Rx BD table. After this buffer has been used, the CP will receive incoming data into the first BD in the table. Setting this bit allows the use of fewer than eight BD to conserve internal RAM.

NOTE

The user is required to set the wrap bit in one of the first eight BDs; otherwise, errant behavior may occur.

I—Interrupt

0 = No interrupt is generated after this buffer has been used.
1 = The RX bit in the BISYNC event register will be set when this buffer has been closed by the BISYNC controller, which can cause an interrupt.

The following status bits are written by the CP after the received data has been placed into the associated data buffer.

C—Control Character

The last byte in the buffer is a user-defined control character.

0 = The last byte of this buffer does not contain a control character.
1 = The last byte of this buffer contains a control character.

B—BCS Received

The last bytes in the buffer contain the received BCS.

0 = This buffer does not contain the BCS.
1 = This buffer contains the BCS. A control character may also reside one byte prior to this BCS.

Bits 9–5—Reserved for future use.

DL—DLE Follow Character Error

While in transparent mode, a DLE character was received, and the next character was not DLE, SYNC, or a valid entry in the control characters table.

PR—Parity Error

A character with a parity error was received and is the last byte of this buffer.

CR—BCS Error

BCS error (CR) is updated every time a byte is written into the buffer. The CR bit includes the calculation for the current byte. By clearing the RBCS bit in the BISYNC mode register within eight serial clocks, the user can exclude the current character from the message BCS calculation. The data length field may be read to determine the current character's position.

OV—Overrun

A receiver overrun occurred during message reception.

CD—Carrier Detect Lost

The carrier detect signal was negated during message reception.

Data Length

The data length is the number of octets that the CP has written into this BD's data buffer, including the BCS (if selected). In BISYNC mode, the data length should initially be set to zero by the user and is incremented each time a received character is written to the data buffer.

NOTE

The actual buffer size should be greater than or equal to the MR-BLR.

Rx Buffer Pointer

The receive buffer pointer, which always points to the first location of the associated data buffer, may be even or odd. The buffer may reside in either internal or external memory.

NOTE

For correct operation of the function codes, the upper 8 bits of the pointer must be initialized to zero.

4.5.13.11 BISYNC Transmit Buffer Descriptor (Tx BD).

Data is presented to the CP for transmission on an SCC channel by arranging it in buffers referenced by the channel's Tx BD table. The CP confirms transmission (or indicates error conditions) using the BDs to inform the processor that the buffers have been serviced. The Tx BD is shown in Figure 4-33.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET + 0	R	X	W	I	L	TB	B	BR	TD	TR	—	—	—	—	UN	CT
OFFSET + 2	DATA LENGTH															
OFFSET + 4	TX BUFFER POINTER (24-bits used, upper 8 bits must be 0)															
OFFSET +6																

Figure 4-33. BISYNC Transmit Buffer Descriptor

The first word of the Tx BD contains status and control bits. These bits are prepared by the user before transmission and are set by the CP after the buffer has been transmitted.

R—Ready

0 = This buffer is not currently ready for transmission. The user is free to manipulate this BD (or its associated buffer). The CP clears this bit after the buffer has been fully transmitted or after an error condition has been encountered.
1 = The data buffer has been prepared for transmission by the user (but not yet transmitted). No fields of this BD may be written by the user once this bit is set.

X—External Buffer

0 = The buffer associated with this BD is in internal dual-port RAM.
1 = The buffer associated with this BD is in external memory.

W—Wrap (Final BD in Table)

0 = This is not the last BD in the Tx BD table.
1 = This is the last BD in the Tx BD table. After this buffer has been used, the CP will transmit data from the first BD in the table.

NOTE

The user is required to set the wrap bit in one of the first eight BDs; otherwise, errant behavior may occur.

I—Interrupt

0= No interrupt is generated after this buffer has been serviced.
1= Either TX or TXE in the BISYNC event register will be set when this buffer has been serviced by the CP, which can cause an interrupt.

L—Last in Message

0 = The last character in the buffer is not the last character in the current block.
1 = The last character in the buffer is the last character in the current block. The transmitter will enter (remain in) normal mode after sending the last character in the buffer and the BCS (if enabled).

TB—Transmit BCS

This bit is valid only when the L bit is set.

0 = Transmit the SYN1–SYN2 sequence or IDLE (according to the SYNF bit in the BISYNC mode register) after the last character in the buffer.
1 = Transmit the BCS sequence after the last character. The BISYNC controller will also reset the BCS generator after transmitting the BCS sequence.

B—BCS Enable

0 = Buffer consists of characters to be excluded from the BCS accumulation.
1 = Buffer consists of characters to be included in the BCS accumulation.

BR—BCS Reset

0 = The BCS accumulation is not reset.
1 = The transmitter BCS accumulation is reset (used for STX or SOH) before sending the data buffer.

TD—Transmit DLE

0 = No automatic DLE transmission before the data buffer.
1 = The transmitter will transmit a DLE character before sending the data buffer, which saves writing the first DLE to a separate data buffer when working in transparent mode. The transmitter also checks for a DLE character in the middle of a buffer. If found, it will insert an extra DLE (if the V-bit is set in the BISYNC SYNC register).

TR—Transparent Mode

0 = The transmitter will enter (remain in) the normal mode after sending the data buffer. In this mode, the transmitter will automatically insert SYNCs in an underrun condition.
1 = The transmitter enters or remains in transparent mode after sending the data buffer. In this mode, the transmitter automatically inserts DLE-SYNC pairs in the underrun condition. Underrun occurs when the BISYNC controller finishes a buffer with L set to zero and the next BD is not available. The transmitter also checks all characters before sending them; if a DLE is detected, another DLE is automatically sent. The user must insert a DLE or program the BISYNC controller to insert it (using TD) before each control character required. The transmitter will calculate the CRC16 BCS even if the BCS bit in the BISYNC mode register is programmed to LRC. The PTCRC should be initialized to the CRC16 preset before setting this bit.

The following status bits are written by the CP after it has finished transmitting the associated data buffer.

UN—Underrun

The BISYNC controller encountered a transmitter underrun condition while transmitting the associated data buffer.

CT—CTS Lost

$\overline{\text{CTS}}$ in NMSI mode or L1GR in IDL/GCI mode was lost during message transmission.

Data Length

The data length is the number of octets that the CP should transmit from this BD's data buffer. It is never modified by the CP. The data length should be greater than zero.

Tx Buffer Pointer

The transmit buffer pointer, which always points to the first byte of the associated data buffer, may be even or odd. The buffer may reside in either internal or external memory.

NOTE

For correct operation of the function codes, the upper 8 bits of the pointer must be initialized to zero.

4.5.13.12 BISYNC Event Register

The SCC event register (SCCE) is referred to as the BISYNC event register when the SCC is programmed as a BISYNC controller. It is an 8-bit register used to report events recog-

nized by the BISYNC channel and to generate interrupts. On recognition of an event, the BISYNC controller sets the corresponding bit in the BISYNC event register. Interrupts generated by this register may be masked in the BISYNC mask register.

The BISYNC event register is a memory-mapped register that may be read at any time. A bit is cleared by writing a one (writing a zero does not affect a bit's value). More than one bit may be cleared at a time. All unmasked bits must be cleared before the CP will negate the internal interrupt request signal. This register is cleared at reset.

7	6	5	4	3	2	1	0
CTS	CD	—	TXE	RCH	BSY	TX	RX

CTS—Clear-To-Send Status Changed

A change in the status of the serial line was detected on the BISYNC channel. The SCC status register may be read to determine the current status.

CD—Carrier Detect Status Changed

A change in the status of the serial line was detected on the BISYNC channel. The SCC status register may be read to determine the current status.

Bit 5—Reserved for future use.

TXE—Tx Error

An error (CTS lost or underrun) occurred on the transmitter channel.

RCH—Receive Character

A character has been received and written to the buffer.

BSY—Busy Condition

A character was received and discarded due to lack of buffers. The receiver will resume reception after an ENTER HUNT MODE command.

TX—Tx Buffer

A buffer has been transmitted. This bit is set on the second to last bit of BCC or data.

RX—Rx Buffer

A complete buffer has been received on the BISYNC channel.

4.5.13.13 BISYNC Mask Register

The SCC mask register (SCCM) is referred to as the BISYNC mask register when the SCC is operating as a BISYNC controller. It is an 8-bit read-write register that has the same bit format as the BISYNC event register. If a bit in the BISYNC mask register is a one, the corresponding interrupt in the event register will be enabled. If the bit is zero, the corresponding interrupt in the event register will be masked. This register is cleared upon reset.

4.5.13.14 Programming the BISYNC Controllers

There are two general techniques that the software may employ to handle data received by the BISYNC controllers. The simplest way is to allocate single-byte receive buffers, request (in the status word in each BD) an interrupt on reception of each buffer (i.e., byte), and implement the BISYNC protocol entirely in software on a byte-by-byte basis. This simple approach is flexible and may be adapted to any BISYNC implementation. The obvious penalty is the overhead caused by interrupts on each received character.

A more efficient method is as follows. Multibyte buffers are prepared and linked to the receive buffer table. Software is used to analyze the first (two to three) bytes of the buffer to determine what type of block is being received. When this has been determined, reception can continue without further intervention to the user's software until a control character is encountered. The control character signifies the end of the block, causing the software to revert back to a byte-by-byte reception mode.

To accomplish this, the RCH bit in the BISYNC mask register should initially be set, enabling an interrupt on every byte of data received. This allows the software to analyze the type of block being received on a byte-by-byte basis. After analyzing the initial characters of a block, the user should either set the receiver transparent mode (RTR) bit in the BISYNC mode register or issue the RESET BCS CALCULATION command. For example, if DLE-STX is received, transparent mode should be entered. By setting the appropriate bit in the BISYNC mode register, the BISYNC controller automatically strips the leading DLE from <DLE-character> sequences. Thus, control characters are only recognized when they follow a DLE character. The RTR bit should be cleared after a DLE-ETX is received.

Alternatively, after receiving an SOH, the RESET BCS CALCULATION command should be issued. This command causes the SOH to be excluded from BCS accumulation and the BCS to be reset. Note that the RBCS bit in the BISYNC mode register (used to exclude a character from the BCS calculation) is not needed here since SYNCs and leading DLEs (in transparent mode) are automatically excluded by the BISYNC controller.

After recognizing the type of block above, the RCH interrupt should be masked. Data reception then continues without further interruption of the M68000 core until the end of the current block is reached. This is defined by the reception of a control character matching that programmed in the receive control characters table.

The control characters table should be set to recognize the end of the block as follows:

Control Characters	E	B	H
ETX	0	1	1
ITB	0	1	0
ETB	0	1	1
ENQ	0	0	0
Next Entry	1	X	X

After the end of text (ETX), a BCS is expected; then the buffer should be closed. Hunt mode should be entered when line turnaround occurs. ENQ characters are used to abort transmis-

sion of a block. For the receiver, the ENQ character designates the end of the block, but no CRC is expected.

Following control character reception (i.e., end of the block), the RCH bit in the BISYNC mask register should be set, re-enabling interrupts for each byte of received data.

4.5.14 DDCMP Controller

The byte-oriented digital data communications message protocol (DDCMP) was originated by DEC for use in networking products. The three classes of DDCMP frames are transparent (or maintenance) messages, data messages, and control messages (see Figure 4-34). Each class of frame starts with a standard two octet synchronization pattern and ends with a CRC. Depending upon the frame type, a separate CRC may be present for the header as well as the data portions of the frame. These CRCs use the same 16-bit generator polynomial as that used in HDLC.

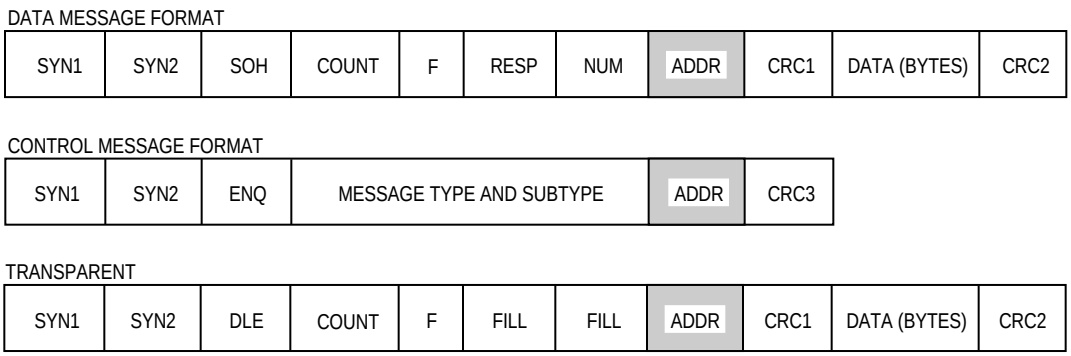


Figure 4-34. Typical DDCMP Frames

The most notable feature of the DDCMP frame is that the frame length is transmitted within the frame itself. Thus, any character pattern can be transmitted in the data field since the character count is responsible for ending the frame, not a special character. For this to work properly, the header containing the frame length must be protected, causing a need for a CRC in the frame header.

The bulk of the frame is divided into fields whose meaning depends on the frame type. Defined control characters are only used in the fixed-length frame headers (the fields between the synchronization octets and the first CRC). The following fields are one byte each: SYN1, SYN2, SOH, RESP, NUM, ADDR, ENQ, DLE, and FILL. The following fields are two bytes each: COUNT + F, CRC1, CRC2, and CRC3. The DATA field is a variable number of bytes, as defined in the COUNT field.

DDCMP communications can be either synchronous or asynchronous, with both types using the same frame format. Synchronous DDCMP frames require the physical layer to transmit the clock along with data over the link. Asynchronous DDCMP frames are composed of asynchronous UART characters, which together form the frame. The receiver and transmitter clocks are not linked; the receiver resynchronizes itself every byte using the start and stop bits of each UART character.

By setting its SCC mode register (SCM), any of the SCC channels may be configured to function as a DDCMP controller. The DDCMP link can be either synchronous (by programming the MODE1–MODE0 bits of the SCC mode register to DDCMP) or asynchronous (by programming the MODE1–MODE0 bits of the SCC mode register to asynchronous and setting the DDCMP bit in the UART mode register). The DDCMP controller handles the basic functions of the DDCMP protocol in both cases.

The SCC in DDCMP mode can work in either IDL, GCI, PCM highway, or NMSI interfaces. When the SCC is used with a modem interface (NMSI), the serial outputs are connected directly to the external pins. The modem interface uses seven dedicated pins: transmit data (TXD), receive data (RXD), receive clock (RCLK), transmit clock (TCLK), carrier detect (CD), clear to send (CTS), and request to send (RTS). Other modem lines can be supported through the parallel I/O pins.

The DDCMP controller consists of separate transmit and receive sections whose operations are asynchronous with the M68000 core and may be either synchronous or asynchronous with respect to the other SCCs. Each clock can be supplied either from the baud rate generator or externally. More information on the baud rate generator is available in 4.5.2 SCC Configuration Register (SCON).

The DDCMP controller key features are as follows:

- Synchronous or Asynchronous DDCMP Links Supported
- Flexible Data Buffers
- Four Address Comparison Registers with Mask
- Automatic Frame Synchronization
- Automatic Message Synchronization by Searching for SOH, ENQ, or DLE
- CRC16 Generation/Checking
- NRZ/NRZI Data Encoding
- Maintenance of Four 16-Bit Error Counters

4.5.14.1 DDCMP Channel Frame Transmission Processing

The DDCMP transmitter is designed to work with almost no intervention from the M68000 core (see Figure 4-35).

When the M68000 core enables the DDCMP transmitter and the link is synchronous, it starts transmitting SYN1–SYN2 pairs (programmed in the data synchronization register) or IDLEs as determined in the DDCMP mode register. The DDCMP controller polls the first buffer descriptor (BD) in the channel's transmit BD table. When there is a message to transmit, the DDCMP controller fetches the data from memory and starts transmitting the message (after first transmitting the SYN1–SYN2 pair when the link is synchronous).

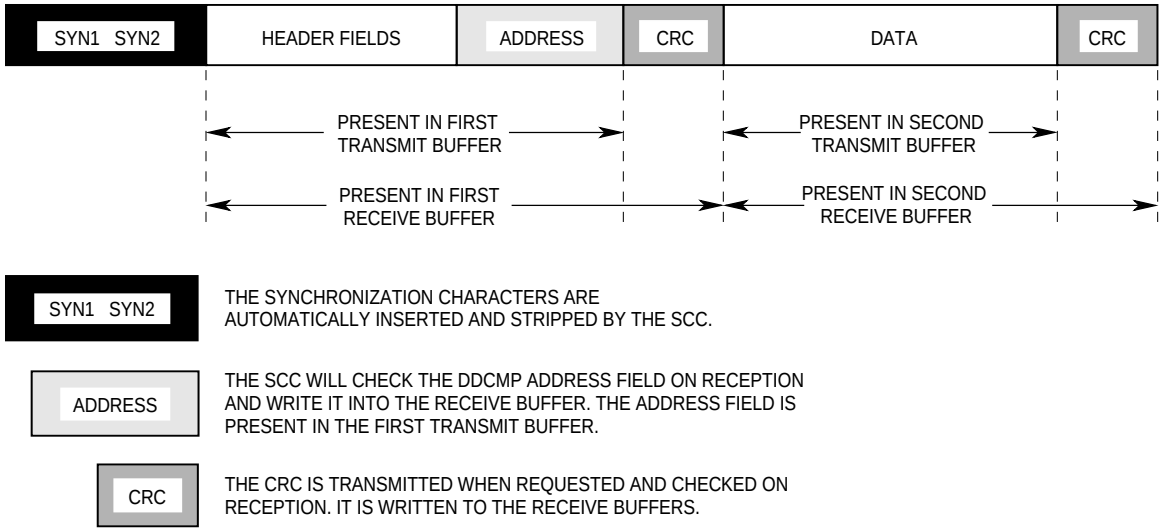


Figure 4-35. DDCMP Transmission/Reception Summary

When a BD has been completely transmitted, the transmit CRC (TC) bit is checked in the BD. If set, the DDCMP controller appends one of the block checks: CRC1, CRC2, or CRC3 for the header field, data message, or control messages, respectively. Next, the DDCMP controller writes the buffer's status bits into the BD and clears the ready bit in the BD. It then proceeds to the next BD in the table. When the last bit (L) is set and the TC bit is set in that BD, the DDCMP controller appends the CRC2 block check to the data field. This bit is also used for transmitting CRC3 in control messages. Next, it writes the buffer status bits into the BD and clears the ready bit. Finally, on synchronous links, either SYN1–SYN2 pairs or IDLEs (as programmed in the DDCMP mode register) are transmitted. When the end of the current BD has been reached and the last bit is not set (working in multibuffer mode or sending back-to-back messages), only the status bits are written. In either case, when a BD has been completely transmitted, an interrupt is issued if the interrupt (I) bit in the BD is set and the event is not masked in the DDCMP mask register. The appropriate setting of the I bit in each BD allows the user to be interrupted after transmission of each buffer, a specific buffer, or each message.

4.5.14.2 DDCMP Channel Frame Reception Processing.

The DDCMP receiver is also designed to work with almost no intervention from the M68000 core (see Figure 4-35).

The DDCMP receiver performs automatic SYN1–SYN2 synchronization on synchronous links and start/stop synchronization on asynchronous links. Automatic message synchronization is achieved by searching for the special starting characters SOH, ENQ, or DLE and making address comparisons with a mask. When the M68000 core enables the DDCMP receiver on synchronous links, it enters hunt mode. In this mode, as data is shifted into the receiver shift register one bit at a time, the contents of the register are compared to the SYN1–SYN2 fields of the data synchronization register (see 4.5.4 SCC Data Synchronization Register (DSR)). If the two are not equal, the next bit is shifted in, and the comparison is repeated. When the registers match, hunt mode is terminated, and character assembly

begins. However, if a character is not SOH, ENQ, DLE, or SYNC, hunt mode is again entered. On asynchronous links, byte synchronization is achieved by the start/stop protocol of the UART. The DDCMP controller is now byte-synchronized and performs SYN1–SYN2 stripping, until receiving one of the three user-defined special starting bytes (SOH for data messages, ENQ for control messages, and DLE for maintenance messages).

If a match is detected, the DDCMP controller fetches the next BD and, if it is empty, starts to transfer the incoming header to the BD's associated data buffer. The DDCMP controller counts the bytes of the fixed-length header and compares the received header address field to the four user-defined values after masking the result with the address mask. When a match is detected, the DDCMP controller continues to transfer the incoming message to the data buffer. The header CRC field (CRC1) is checked and is written to the data buffer. The DDCMP controller updates the CRC error (CR) bit, sets the header (H) bit, writes the message type and status bits into the BD, and clears the empty bit. It next generates a maskable receive block interrupt (RBK), indicating that a header has been received and is in memory. If the header was a control message, the DDCMP controller waits for a new message.

If there is no match in address comparison and the header is error free, the DDCMP controller will use the same buffer for the next message. To maintain synchronization, the DDCMP controller counts the data length based on the count field contained in the header.

When the data buffer has been filled, the DDCMP controller clears the empty bit in the BD and generates a maskable received buffer interrupt (RBD). If the incoming message exceeds the length of the data buffer, the DDCMP controller fetches the next BD in the table, and, if it is empty, continues to transfer the rest of the message to the new data buffer. When the message ends, the CRC2 field is checked and written to the data buffer. The DDCMP controller sets the last bit, writes the message type and other status bits into the BD, and clears the empty bit. Following this, it generates an RBK, indicating that a message has been received and is in memory. The DDCMP controller then waits for a new message.

4.5.14.3 DDCMP Memory Map

When configured to operate in DDCMP mode, the IMP overlays the structure illustrated in Table 4-9 onto the protocol-specific area of that SCC's parameter RAM. Refer to 2.8 MC68302 Memory Map for the placement of the three SCC parameter RAM areas and to Table 4-5 for the other parameter RAM values.

Table 4-10. DDCMP Specific Parameter RAM

Address	Name	Width	Description
SCC Base + 9C SCC Base + 9E SCC Base + A0 # SCC Base + A2	RCRC CRCC PCRC TCRC	Word Word Word Word	Temp Receive CRC CRC16 Constant Preset CRC16 Temp Transmit CRC
SCC Base + A4 # SCC Base + A5 # SCC Base + A6 SCC Base + A7 # SCC Base + A8 SCC Base + A9 #	DSYN1 DSOH Reserved DENQ Reserved DDLE	Byte Byte Byte Byte Byte Byte	DDCMP SYN1 Character DDCMP SOH Character DDCMP ENQ Character DDCMP DLE Character
SCC Base + AA # SCC Base + AC # SCC Base + AE # SCC Base + B0 #	CRC1EC CRC2EC NMARC DISMC	Word Word Word Word	CRC1 Error Counter CRC2 Error Counter Nonmatching Address Received Counter Discard Message Counter
SCC Base + B2 SCC Base + B4	RMLG RMLG_CNT	Word Word	Received Message Length Received Message Length Counter
SCC Base + B6 # SCC Base + B8 # SCC Base + BA # SCC Base + BC # SCC Base + BE #	DMASK DADDR1 DADDR2 DADDR3 DADDR4	Word Word Word Word Word	User-Defined Frame Address Mask User-Defined Frame Address User-Defined Frame Address User-Defined Frame Address User-Defined Frame Address

Initialized by the user (M68000 core).

4.5.14.4 DDCMP Programming Model

The M68000 core configures each SCC to operate in one of four protocols by the MODE1–MODE0 bits in the SCC mode register. If MODE1–MODE0 = 10, DDCMP operation is selected with synchronous links. For asynchronous links, MODE1–MODE0 = 01 (ASYNC) should be selected, and the DDCMP bit in the UART mode register should be set. The SYN1–SYN2 synchronization characters are programmed in the data synchronization register (DSR). See 4.5.4 SCC Data Synchronization Register (DSR) for more programming information. The DDCMP controller uses the same basic data structure as the UART, HDLC, and BISYNC controllers.

The DDCMP controller generates and checks the CRC16 message trailer. It can be preset to ones or zeros by writing to the preset CRC (PCRC) register before enabling the receiver or the transmitter. The received message length (RMLG) is the header byte count value as determined by the receiver, and the received message length counter (RMLG _ CNT) is the temporary received data downcounter.

Receive and transmit errors are reported in their respective BDs. The line status signals ($\overline{CD}$ and $\overline{CTS}$) may be read in the SCC status register and a maskable interrupt is generated upon each status change (see 4.5.2 SCC Configuration Register (SCON)).

4.5.14.5 DDCMP Command Set.

The following commands are issued to the command register:

STOP TRANSMIT Command

After a hardware or software reset and the enabling of the channel in the SCC mode register, the channel is in the transmit enable mode and starts polling the first BD in the table approximately every eight transmit clocks.

The channel STOP TRANSMIT command disables the transmission of messages on the transmit channel. If this command is received by the DDCMP controller during message

transmission, message transmission is aborted after the contents of the FIFO (up to three bytes) are transmitted. The TBD# is not advanced. No new BD is accessed, and no new messages are transmitted for this channel. Upon receipt of this command, the transmitter aborts the message transmission (if currently transmitting) and then transmits SYN1–SYN2 pairs or IDLEs as determined by the DDCMP mode register.

The STOP TRANSMIT command must be issued before the SCC mode register is used to disable the transmitter if the transmitter is to be re-enabled at a later time.

RESTART TRANSMIT Command

The RESTART TRANSMIT command re-enables the transmission of characters on the transmit channel. This command is expected by the DDCMP controller after a STOP TRANSMIT command, after a STOP TRANSMIT command followed by the disabling of the channel in its SCC mode register, or after a transmitter error (underrun or CTS lost during data or maintenance message header fields). The DDCMP controller will resume transmission from the current transmitter BD number (TBD#) in the channel's transmit BD table.

If the channel is being re-enabled, the RESTART TRANSMIT command must be used and should be followed by the enabling of the transmitter in the SCC mode register.

ENTER HUNT MODE Command

After a hardware or software reset and the enabling of the channel in the SCC mode register, the channel is in the receive enable mode and will use the first BD in the table.

The ENTER HUNT MODE command is used to force the DDCMP controller to abort reception of the current message, generate an RBD interrupt (if enabled) as the buffer is closed, and enter hunt mode. In hunt mode, the DDCMP controller continually scans the input data stream for the SYN1–SYN2 sequence on synchronous links. Then for synchronous or asynchronous links, the DDCMP controller scans the input bytes for the starting byte of one of the messages. After receiving the command, the current receive buffer is closed, and the CRC is reset. Message reception continues using the next BD.

If an enabled receiver has been disabled (by clearing ENR in the SCC mode register), the ENTER HUNT MODE command must be given to the channel before setting ENR again.

4.5.14.6 DDCMP Control Character Recognition

The DDCMP controller can recognize three special control characters. These characters are used to synchronize the message and allow the DDCMP controller to function in a DMA-controlled environment.

DSYN1—DDCMP Sync Character Register

The 8-bit DSYN1 register should be written with the same value that was written in the SYN1 byte of the data synchronization register (DSR). DSYN1 is a memory-mapped read-write register.

NOTE

For correct operation of DDCMP, DSYN1, SYN1, and SYN2 must be the same value.

DSOH—DDCMP SOH Register

The 8-bit DSOH register is used to synchronize data messages by the DDCMP controller. When the DDCMP controller is not in hunt mode (byte synchronization is now established), it searches for the SOH character to start processing data messages. The DDCMP controller transfers the header and the data fields of the message to the buffer, checks the header and data CRCs, counts the data field up to the value contained in the header byte count field, and compares the header address field against the user-defined addresses. The DSOH register is a memory-mapped read-write register.

DENQ—DDCMP ENQ Register

The 8-bit DENQ register is used to synchronize control messages by the DDCMP controller. When the DDCMP controller is not in hunt mode (byte synchronization is established), it searches for the ENQ character to start processing control messages. The DDCMP controller transfers the message to the buffer, checks the CRC, and compares the message address field against the user-defined addresses. The DENQ register is a memory-mapped read-write register.

DDLE—DDCMP DLE Register

The 8-bit DDLE register is used to synchronize maintenance messages by the DDCMP controller. When the DDCMP controller is not in hunt mode (byte synchronization is established), it searches for the DLE character to start processing the maintenance messages. The DDCMP controller transfers the header and the data fields of the message to the buffer, checks the header and data CRCs, counts the data field up to the value contained in the header byte count field, and compares the header address field against the user-defined addresses. The DDLE register is a memory-mapped read-write register.

4.5.14.7 DDCMP Address Recognition.

Each DDCMP controller has five 16-bit registers to support address recognition: one mask register and four address registers (DMASK, DADDR1, DADDR2, DADDR3, and DADDR4). The DDCMP controller reads the message address from the receiver, masks it with the user-defined DMASK bits, and then checks the result against the four address register values. A one in DMASK indicates a bit position where a comparison should take place; a zero masks the comparison. For 8-bit address comparison, the high byte of DMASK should be zero.

4.5.14.8 DDCMP Error-Handling Procedure

The DDCMP controller reports message reception and transmission errors using the channel BDs, the error counters, and the DDCMP event register. The modem interface lines can also be directly monitored with the SCC status register.

Transmission errors:

1. Transmitter Underrun. When this error occurs, the channel terminates buffer transmission, closes the buffer, sets the underrun (UN) bit in the BD, and generates the transmit error (TXE) interrupt (if enabled). The channel will resume transmission after the reception of the RESTART TRANSMIT command. The FIFO size is three bytes.

NOTE

This error can occur only on synchronous links.

2. Clear-To-Send Lost (Collision) During Message Transmission. When this error occurs and the channel is not programmed to control this line with software, the channel terminates buffer transmission, closes the buffer, sets the CTS lost (CT) bit in the BD, and generates the transmit error (TXE) interrupt (if enabled). The channel resumes transmission after the reception of the RESTART TRANSMIT command.

Reception Errors:

1. Carrier Detect Lost During Message Reception. When this error occurs and the channel is not programmed to control this line with software, the channel terminates message reception, closes the buffer, sets the carrier detect lost (CD) bit in the BD, and generates the receive block (RBK) interrupt (if enabled). This error has the highest priority. The rest of the message is lost, and other errors in that message are not checked.
   The channel will enter hunt mode immediately. It is possible that a SYN1–SYN2-(SOH,DLE,ENQ) sequence in data will be incorrectly interpreted as the start of the next header, but this "header" will have a CRC error.
2. Overrun Error. The DDCMP controller maintains an internal three-byte FIFO for receiving data. The CP begins programming the SDMA channel (if the data buffer is in external memory) and updating the CRC when the first word is received into the FIFO. If the receive FIFO overrun error occurs, the channel writes the received data byte to the internal FIFO on top of the previously received byte. The previous data byte is lost. Then the channel closes the buffer, sets the overrun (OV) bit in the BD, and generates the receive block (RBK) interrupt (if enabled).
   The channel will enter hunt mode immediately. It is possible that a SYN1–SYN2-(SOH,DLE,ENQ) sequence in data will be incorrectly interpreted as the start of the next header, but this “header” will have a CRC error.
3. CRC1 (Header CRC) Error. When this error occurs, the channel writes the received CRC to the data buffer, closes the buffer, sets the CRC error (CR) bit in the BD, generates the RBK interrupt (if enabled), increments the error counter (CRC1EC), and enters hunt mode.
   When this error occurs on data-and maintenance-message header fields, the channel will enter hunt mode immediately. It is possible that a SYN1–SYN2-(SOH,DLE,ENQ) sequence in data will be incorrectly interpreted as the start of the next header, but this “header” will have a CRC error.
4. CRC2 (Data or Maintenance CRC) or CRC3 (Control Message) Error. When this error occurs, the channel writes the received CRC to the data buffer, closes the buffer, sets the CRC error (CR) bit in the BD, and generates the RBK interrupt (if enabled). The channel also increments the CRC2EC counter and enters hunt mode.
5. Framing Error. A framing error is detected by the DDCMP controller when no stop bit is detected in a received data string. When this error occurs, the channel writes the received character to the buffer, closes the buffer, sets the framing error (FR) bit in the BD, and generates the RBK interrupt (if enabled). When this error occurs, parity is not checked for this character.

The channel will enter hunt mode immediately. It is possible that a SYN1–SYN2-(SOH,DLE,ENQ) sequence in data will be incorrectly interpreted as the start of the next header, but this “header” will have a CRC error.

NOTE

This error can occur only on asynchronous links.

6. Parity Error. When a parity error occurs, the channel writes the received character to the buffer, closes the buffer, sets the parity error (PR) bit in the BD, and generates the RBK interrupt (if enabled).
   The channel will enter hunt mode immediately. It is possible that a SYN1–SYN2-(SOH,DLE,ENQ) sequence in data will be incorrectly interpreted as the start of the next header, but this “header” will have a CRC error.

NOTE

This error can occur only on asynchronous links.

Error Counters

The CP maintains four 16-bit (modulo 2**16) error counters for each DDCMP controller. They can be initialized by the user when the channel is disabled. The counters are as follows:

—CRC1EC—CRC1 Error Counter
—CRC2EC—CRC2/CRC3 Error Counter
—NMARC — Nonmatching Address Received Counter (updated only when the frame is error-free)
—DISMC — Discarded Messages (received messages when there are no free buffers and the frame is error-free)

4.5.14.9 DDCMP Mode Register

Each SCC mode register is a 16-bit, memory- mapped, read-write register that controls the SCC operation. The term DDCMP mode register refers to the protocol-specific bits (15–6) of the SCC mode register when that SCC is configured for DDCMP. The read-write DDCMP mode register is cleared by reset.

15	14	13	12	11	10	9	8	7	6	5 … 0
NOS3	NOS2	NOS1	NOS0	—	V.110	—	—	SYNF	ENC	COMMON SCC MODE BITS

NOS3–NOS0—Minimum Number of SYN1—SYN2 Pairs between or before Messages (1 to 16 SYNC Pairs)

If NOS3–NOS0 = 0000, then 1 SYNC pair will be transmitted; if NOS3–NOS0 = 1111, then 16 SYNC pairs will be transmitted.

NOTE

With appropriate programming of the transmit BD (TC = 1 and L = 0), it is possible to transmit back-to-back messages.

Bits 11, 9–8—Reserved for future use.

V.110—V.110 Mode

0 = DDCMP mode; synchronous DDCMP is chosen.
1 = V.110 mode; the V.110 protocol description is in 4.5.15 V.110 Controller.

SYNF—Transmit SYN1–SYN2 or IDLE between Messages and Control the RTS Pin

0 = Send ones between messages. $\overline{RTS}$ is negated between messages.

NOTE

The DDCMP controller can transmit ones in both NRZ and NRZI data encoded formats. The minimum number of ones transmitted is 17.

1 = Send SYN1–SYN2 pairs between messages. $\overline{RTS}$ is always asserted. Note that SYN1 and SYN2 may be the same character.

ENC—Data Encoding Format

0 = Nonreturn to Zero (NRZ). A one is a high level; a zero is a low level.
1 = Nonreturn to Zero Inverted (NRZI). A one is represented by no change in the level; a zero is represented by a change in the level. The receiver decodes NRZI, but a clock must be supplied. The transmitter encodes NRZI.

COMMON SCC MODE BITS—See 4.5.3 SCC Mode Register (SCM) for a description of the DIAG1, DIAG0, ENR, ENT, MODE1, and MODE0 bits.

4.5.14.10 DDCMP Receive Buffer Descriptor (Rx BD)

The CP reports information about the received data for each buffer using the BDs. The Rx BD is shown in Figure 4-36. The CP closes the current buffer, generates a maskable interrupt, and starts to receive data in the next buffer after any of the following events:

- Receiving the received message length number of bytes (RMLG)
- Detecting an error
- Detecting a full receive buffer
- Issuing the ENTER HUNT MODE command

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET + 0	E	X	W	I	L	H	T2	T1	—	—	CF	FR	PR	CR	OV	CD
OFFSET + 2	DATA LENGTH															
OFFSET + 4	RX BUFFER POINTER (24-bits used, upper 8 bits must be 0)															
OFFSET +6																

Figure 4-36. DDCMP Receive Buffer Descriptor

The first word of the Rx BD contains control and status bits. Bits 15–12 are written by the user before the buffer is linked to the Rx BD table, and bits 5–0 and 11–8 are set by the IMP

following message reception. Bit 15 determines whether the M68000 core or the CP may currently access the BD.

E—Empty

0 = The data buffer associated with this BD has been filled with received data, or data reception has been aborted due to an error condition. The M6800 core is free to examine or write to any fields of the BD.
1 = The data buffer associated with this BD is empty. This bit signifies that the BD and its associated buffer are available to the DDCMP controller. The M68000 core should not write to any fields of this BD after it sets this bit. Note that the empty bit will remain set while the DDCMP controller is currently filling the buffer with received data.

X—External Buffer

0 = The buffer associated with this BD is in internal dual-port RAM.
1 = The buffer associated with this BD is in external memory.

W—Wrap (Final BD in Table)

0 = This is not the last BD in the Rx BD table.
1 = This is the last BD in the Rx BD table. After this buffer has been used, the DDCMP controller places incoming data into the first BD in the table.

NOTE

The user is required to set the wrap bit in one of the first eight BDs; otherwise, errant behavior may occur.

I—Interrupt

0 = No interrupt is generated after this buffer has been closed.
1 = The RBD or RBK bits in the DDCMP event register will be set when this buffer has been closed by the DDCMP controller, which can cause interrupts.

The following status bits are written by the DDCMP controller after it has finished receiving data in the associated data buffer.

L—Last in Message

0 = The buffer is not the last in a message.
1 = The buffer is the last in a message.

H—Header in Buffer

0 = The buffer does not contain a message header.
1 = The buffer contains a message header.

NOTE

To correctly identify buffers containing headers, the buffer size should be eight or more bytes in length so that the header will fit in a single buffer.

T2,T1—Message Type

00 = Data message
01 = Control message
10 = Maintenance message
11 = Reserved

Bits 7–6—Reserved for future use.

CF—CRC Follow Error

The character following the CRC for this message was not one of SOH, ENQ, DLE, SYN, or IDLE. The receiver then enters hunt mode.

FR—Framing Error

A character with a framing error was received. The associated character may be found at the last location in this buffer. A framing error is detected by the UART controller when no stop bit is detected in the receive data string.

NOTE

This error can occur only on asynchronous DDCMP links.

PR—Parity Error

A character with a parity error was received. The associated character may be found at the last location in this buffer.

NOTE

This error can occur only on asynchronous DDCMP links.

CR—Rx CRC Error

A message with a CRC error was received in the header (CRC1) or data (CRC2) fields or a control message (CRC3).

OV—Overrun

A receiver overrun occurred during message reception.

CD—Carrier Detect Lost

The CD signal was negated during message reception. This bit is valid only when working in NMSI mode.

Data Length

The data length is the number of octets that the DDCMP controller has written to this BD's data buffer. It is written by the CP once as the BD is closed.

NOTE

The actual buffer size should be greater than or equal to eight (to ensure the header is received in one buffer).

Rx Buffer Pointer

This pointer contains the address of the associated data buffer and may be even or odd. The buffer may reside in either internal or external memory.

NOTE

For correct operation of the function codes, the upper 8 bits of the pointer must be initialized to zero.

4.5.14.11 DDCMP Transmit Buffer Descriptor (Tx BD)

Data is presented to the CP for transmission over an SCC channel by arranging it in buffers referenced by the channel's Tx BD table. The CP confirms transmission (or indicates error conditions) using the BDs to inform the M68000 core that the buffers have been serviced. The Tx BD is shown in Figure 4-37.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET + 0	R	X	W	I	L	TC	OL	—	—	—	—	—	—	—	UN	CT
OFFSET + 2	DATA LENGTH															
OFFSET + 4	TX BUFFER POINTER (24-bits used, upper 8 bits must be 0)															
OFFSET +6																

Figure 4-37. DDCMP Transmit Buffer Descriptor

The first word contains status and control bits. Bits 15–9 are prepared by the user before transmission. Bits 1–0 are set by the DDCMP controller after the buffer has been transmitted. Bit 15 is set by the user when the buffer and BD have been prepared and is cleared by the DDCMP controller when the message is transmitted.

R—Ready

0 = This buffer is not currently ready for transmission. The user is free to manipulate this BD (or its associated buffer). The DDCMP controller clears this bit after the buffer has been completely transmitted (or after an error condition is encountered).
1 = The data buffer has been prepared for transmission by the user (but not yet transmitted). No fields of this BD may be written by the user once this bit is set.

X—External Buffer

0 = The buffer associated with this BD is in internal dual-port RAM.
1 = The buffer associated with this BD is in external memory.

W—Wrap (Final BD in Table)

0 = This is not the last BD in the Tx BD table.
1 = This is the last BD in the Tx BD table. After this buffer has been used, the DDCMP controller will transmit data from the first BD in the table.

NOTE

The user is required to set the wrap bit in one of the first eight BDs; otherwise, errant behavior may occur.

I—Interrupt

0 = No interrupt is generated after this buffer has been serviced.
1 = Either TX or TXE in the DDCMP event register will be set when this buffer has been serviced by the DDCMP controller, which can cause interrupts.

L—Last

0 = This buffer is not the last in the message.
1 = The last bit is set by the processor to indicate that this buffer is the last buffer in the current message.

NOTE

The DDCMP controller checks the TC bit, not the last bit, to determine whether to append the CRC sequence. The DDCMP controller will transmit the programmable number of SYN1–SYN2 pairs before transmitting the next buffer (message) when the last bit is set.

TC—Tx CRC

0 = Do not transmit a CRC sequence after the buffer's last data byte.
1 = Transmit a CRC16 sequence after the buffer's last data byte.

When the last bit is not set but TC is set (e.g., in a header buffer), the DDCMP controller will append the next buffer immediately following the CRC sequence. The preset value for the CRC16 calculation is located in the PCRC register and should be initialized to all zeros or all ones.

OL—Optional Last

This bit allows the user to transmit abutted messages in DDCMP.

0 = Normal operation. The SYNF bit in the DDCMP mode register determines the pattern transmitted between messages.
1 = Abutted messages. The CP checks the ready bit of the next Tx BD after processing the current BD, and, if set, abuts the next message to the current message. If the ready bit is not set, the SYNF bit determines the transmitted pattern.

Bits 8–2—Reserved for future use.

The following status bits are written by the DDCMP controller after it has finished transmitting the associated data buffer.

UN—Underrun

The DDCMP controller encountered a transmitter underrun condition while transmitting the associated data buffer.

NOTE

This error can occur only on synchronous links.

CT—CTS Lost

$\overline{\text{CTS}}$ in NMSI mode or grant in IDL/GCI mode was lost during message transmission.

Data Length

The data length is the number of octets that the DDCMP controller should transmit from this BD's data buffer. It is never modified by the CP. The data length should be greater than zero.

Tx Buffer Pointer

This pointer, which contains the address of the associated data buffer, may be even or odd. The buffer may reside in either internal or external memory.

NOTE

For correct operation of the function codes, the upper 8 bits of the pointer must be initialized to zero.

4.5.14.12 DDCMP Event Register

The SCC event register (SCCE) is referred to as the DDCMP event register when the SCC is configured for DDCMP. It is an 8-bit register used to report events recognized by the DDCMP channel and to generate interrupts. On recognition of an event, the DDCMP controller sets its corresponding bit in this register. Interrupts generated by this register may be masked in the DDCMP mask register.

The DDCMP event register is a memory-mapped register that may be read at any time. A bit is cleared by writing a one (writing zero does not affect a bit's value). More than one bit may be cleared at a time. All unmasked bits must be cleared before the CP will clear the internal interrupt request. This register is cleared at reset.

7	6	5	4	3	2	1	0
CTS	CD	—	TXE	RBK	BSY	TX	RBD

CTS—Clear-To-Send Status Changed

A change in the status of the $\overline{\text{CTS}}$ line was detected on the DDCMP channel. The SCC status register may be read to determine the current status.

CD—Carrier Detect Status Changed

A change in the status of the CD line was detected on the DDCMP channel. The SCC status register may be read to determine the current status.

Bit 5—Reserved for future use.

TXE—Tx Error

An error (CTS lost or underrun) occurred on the transmitter channel.

RBK—Receive Block

A complete block has been received on the DDCMP channel. A block is defined as reception of a complete header, a complete message, or a receiver error condition.

BSY—Busy Condition

A data byte was received and discarded due to lack of buffers. The receiver will enter hunt mode automatically.

TX—Tx Buffer

A buffer has been transmitted over the DDCMP channel. This bit is set no sooner than at the beginning of the transmission of the second-to-last data (or CRC) bit in the frame, if this buffer was the last in a frame. Otherwise, it is set as the last data byte is written to the transmit FIFO.

RBD—Rx Buffer

A buffer has been received on the DDCMP channel that was not a complete block.

4.5.14.13 DDCMP Mask Register

The SCC mask register (SCCM) is referred to as the DDCMP mask register when the SCC is operating as a DDCMP controller. It is an 8-bit read-write register that has the same bit format as the DDCMP event register. If a bit in the DDCMP mask register is a one, the corresponding interrupt in the event register will be enabled. If the bit is zero, the corresponding interrupt in the event register will be masked. This register is cleared upon reset.

4.5.15 V.110 Controller

V.110 is an ISDN protocol that interfaces non-ISDN terminal equipment into one of the B channels of the 2B + D basic rate ISDN S-interface. V.110 offers the ability to transmit data from non-ISDN terminal equipment over one of the B channels through an ISDN to other non-ISDN terminal equipment. A common application of V.110 rate adaption is providing a connection between RS-232 based terminal equipment over an ISDN.

Since V.110 uses the B channels, a V.110 application requires that an ISDN call first be set up over the D channel. This call setup uses the LAPD protocol, which can be implemented using another SCC in the MC68302 (see 4.5.12 HDLC Controller).

V.110 can adapt slower equipment up to the 64 kbps B channel rate. If the non-ISDN terminal equipment is synchronous, a one- or two-step process is required. If asynchronous equipment is adapted, a three-step process is required. The standard allows for the adaption of asynchronous rates up to 19.2 kbps and synchronous rates up to 56 kbps.

Only the third step (RA2) is required for adaption of synchronous 48- and 56-kbps rates commonly used by synchronous modems. RA1 and RA2 are needed for synchronous rates of 600, 1200, 2400, 4800, 7200, 9600, 12 kbps, 14.4 kbps, and 19.2 kbps. Asynchronous terminals require all three steps because rate-adapting asynchronous terminals require the additional task of compensating for slight underspeed or overspeed of the terminal with respect to the ISDN clock rate. This is why the RA0 function refers to stop-bit manipulation.

Data is transmitted over the ISDN in a defined 80-bit frame format. This frame includes all data from the terminal (including start and stop bits for the asynchronous terminals) as well as various framing and control functions.

Another rate adaption protocol, called V.120, is an alternative protocol to V.110. V.120 is an extension of the LAPD protocol and may be implemented on the MC68302 using an SCC configured in HDLC mode.

4.5.15.1 Bit Rate Adaption of Synchronous Data Signaling Rates up to 19.2 kbps

The V.110 synchronous bit rate adaption block diagram within the terminal adaptor is shown in Figure 4-38.

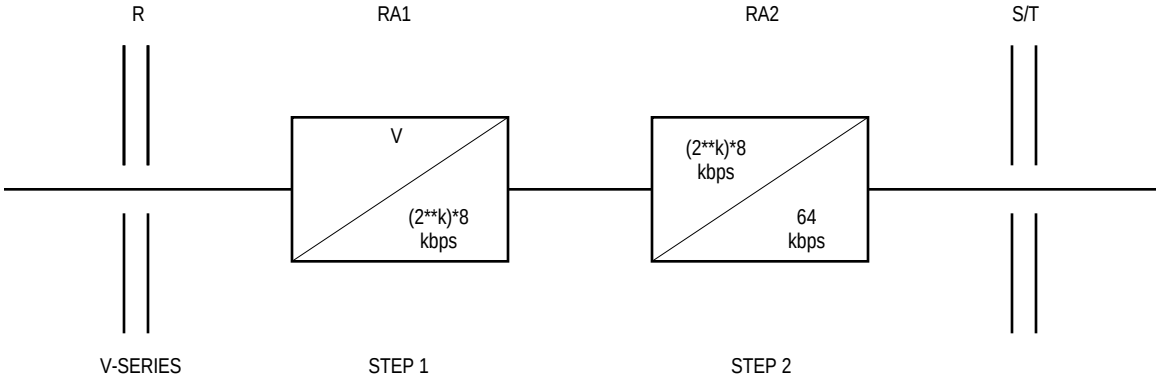


Figure 4-38. Two-Step Synchronous Bit Rate Adaption

This function may be implemented with two SCCs, one of which is configured for V.110 operation. Step 1 (RA1) rate adaption can be achieved using one SCC channel programmed to promiscuous (totally transparent) mode (see 4.5.13 BISYNC Controller). This SCC will transfer the data between the R interface and IMP memory. The M68000 core must be programmed to format the data in memory according to the V.110 protocol to create the V.110 80-bit frame. Another SCC is used to transfer the data between IMP memory and the S/T interface. This SCC should be programmed for V.110 operation, which provides the conversion of the data rate to 64 kbps. Data may be transmitted and received on 1, 2, or 4 bits of an ISDN B channel as programmed in the SIMASK register.

NOTE

V.110 contains a requirement (under further study) for control information on the R interface (i.e., RTS, CTS, CD, DTR, and DSR), conveyed by the S bits in the V.110 frame, not to have a different transmission delay than the user data conveyed by the D8–D1 bits. This very time-critical aspect of the standard is not supported by the IMP. In this case, provision would need to be made by the user to guarantee correct sampling times for this information to correspond with the user data. The IMP, however, can detect changes in these signals and issue appropriate interrupts to the M68000 core, allowing the function to be fully implemented in a slightly longer time period.

4.5.15.2 Rate Adaption of 48- and 56-kbps User Rates to 64 kbps

This function may again be implemented with two SCCs; however, in this case, the SCC connected to the B channel is programmed to promiscuous (totally transparent) mode rather than for V.110 operation (see 4.5.9 SCC Transparent Mode). The M68000 core will need to format the framing pattern in the 48-kbps conversion case. For the 56-kbps rate conversion, however, the B channel mask (SIMASK) in the serial channel physical interface can be used.

4.5.15.3 Adaption for Asynchronous Rates up to 19.2 kbps

The V.110 asynchronous bit rate adaption block diagram within the terminal adaptor is shown in Figure 4-39.

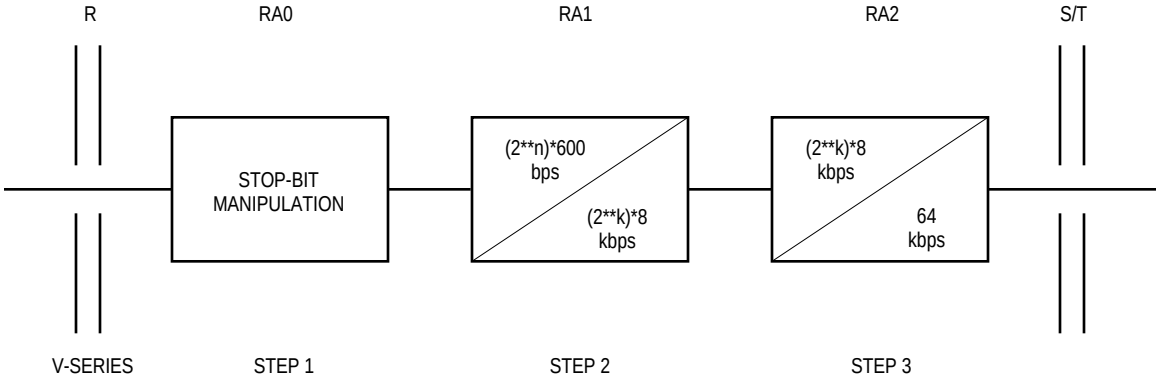


Figure 4-39. Three-Step Asynchronous Bit Rate Adaption

This function may be implemented in two SCCs. One SCC operates as a UART; the other SCC operates as a V.110 controller. The M68000 core formats the data for transmission by the V.110 at the 64 kbps data rate. Thus, the RA1 step is hidden in software.

4.5.15.4 V.110 Controller Overview.

By the appropriate setting of its SCC mode register, any of the SCC channels may be configured to function as a V.110 controller. MODE1–MODE0 bits the SCC mode register should be programmed to DDCMP, and the V.110 bit in the DDCMP mode register should be set. The V.110 controller has the ability to receive and transmit V.110 80-bit frames. The processing of those frames is handled by the M68000 core in software.

The V.110 receiver will synchronize on the 17-bit alignment pattern of the frame:

00000000 1xxxxxxx 1xxxxxxx 1xxxxxxx 1xxxxxxx

1xxxxxxx 1xxxxxxx 1xxxxxxx 1xxxxxxx 1xxxxxxx

After achieving frame synchronization, the receiver will transfer the frame data to a receive buffer (the leading one will be the MSB so that the programmer does not have to swap the bits). The V.110 controller will write nine bytes of data to the buffer (discarding the first byte of all zeros). The M68000 core should unformat the data in memory according to the V.110 protocol to create the data buffer; it may then use another SCC controller to transmit this data to the R interface.

The V.110 transmitter will transmit a data buffer transparently with a bit swap (the MSB will be transmitted first) onto a B channel. The data buffer should contain the 17-bit alignment pattern. Another SCC controller may be used to receive data from the R interface. The M68000 core should then format the data according to the V.110 protocol to create the V.110 80-bit frame data buffer. The V.110 controller will then transmit it onto the B channel.

The V.110 controller operates on the ISDN physical interface using either IDL or GCI (IOM-2) over one of the B channels. NMSI and PCM physical interfaces are also possible. The data synchronization register (DSR) should be programmed to 'xxxxxxx1 00000000'b to achieve the proper frame synchronization (see 4.5.4 SCC Data Synchronization Register (DSR)).

4.5.15.5 V.110 Programming Model

The M68000 core configures each SCC to operate in one of the protocols by the MODE1–MODE0 bits in the SCC mode register. If MODE1–MODE0 = 10, the synchronous link DDCMP protocol is selected. The V.110 bit should also be set in the DDCMP mode register. The V.110 controller uses the same basic data structure as the DDCMP controller, the same command set, and the same event and mask registers for interrupt generation.

4.5.15.6 Error-Handling Procedure

The V.110 controller reports frame reception and transmission error conditions using the channel buffer descriptors (BDs) and the V.110 event register.

Transmission Errors:

1. Transmitter Underrun. When this error occurs, the channel terminates buffer transmission, closes the buffer, sets the underrun (UN) bit in the BD, and generates the transmit error (TXE) interrupt (if enabled). The channel will resume transmission after the reception of the RESTART TRANSMIT command. The FIFO size is three bytes.

Reception Errors:

1. Overrun Error. The V.110 controller maintains an internal three-byte length FIFO for receiving data. When the receive FIFO overrun error occurs, the channel writes the received data byte to the internal FIFO on top of the previously received byte (the previous data byte is lost). Then the channel closes the buffer, sets the overflow (OV) bit in the BD, and generates the receive frame (RXF) interrupt (if enabled). The channel will automatically enter hunt mode.
2. Synchronization Error. A synchronization error is detected by the V.110 controller when the MSB of every byte is not one. When this error occurs, the channel writes the received byte to the buffer and continues to receive the V.110 frame. When the frame ends, the channel closes the buffer, sets the synchronization error (SE) bit in the BD, and generates the RXF interrupt (if enabled). The channel will automatically enter the hunt mode.

4.5.15.7 V.110 Receive Buffer Descriptor (Rx BD)

The CP reports information about the received data for each buffer using the BDs. The Rx BD is shown in Figure 4-40. The CP closes the current buffer, generates a maskable interrupt, and starts to receive data in the next buffer after any of the following events:

- Receiving of 10 bytes (80-bit frame)
- Detecting of an error
- Issuing the ENTER HUNT MODE command

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET + 0	E	X	W	—	—	—	—	—	—	—	—	—	SE	—	OV	—
OFFSET + 2	DATA LENGTH															
OFFSET + 4	RX BUFFER POINTER (24-bits used, upper 8 bits must be 0)															
OFFSET +6																

Figure 4-40. V.110 Receive Buffer Descriptor

The first word of the Rx BD contains control and status bits. Bits 15–13 are written by the user before the buffer is linked to the Rx BD table, and bits 1 and 3 are set by the IMP following message reception. Bit 15 is set by the M68000 core when the buffer is available to the V.110 controller and is cleared by the V.110 controller after filling the buffer.

E—Empty

0 = The data buffer associated with this BD has been filled with received data, or data reception has been aborted due to an error condition. The M68000 core is free to examine or write to any fields of the BD.

1 = The data buffer associated with this BD is empty. This bit signifies that the BD and its associated buffer are available to the V.110 controller. The M68000 core should not write to any fields of this BD after it sets this bit. The empty bit will remain set while the V.110 controller is currently filling the buffer with received data.

X—External Buffer

0 = The buffer associated with this BD is in internal dual-port RAM.

1 = The buffer associated with this BD is in external memory.

W—Wrap (Final BD in Table)

0 = This is not the last BD in the Rx BD table.

1 = This is the last BD in the Rx BD table. After this buffer has been used, the V.110 controller receives incoming data by placing it in the first BD in the table.

NOTE

The user is required to set the wrap bit in one of the first eight BDs; otherwise, errant behavior may occur.

Bits 12–4, 2, 0—Reserved for future use.

SE—Synchronization Error

A frame with a synchronization error was received. A synchronization error is detected by the V.110 controller when the MSB of a byte (except the all-zeros byte) is not one.

OV—Overrun

A receiver overrun occurred during message reception.

Data Length

The data length is the number of octets that the V.110 controller has written to this BD data buffer. It is written by the CP once as the BD is closed. The V.110 controller will write nine bytes of data to the buffer. It will not write the all-zeros byte to the buffer.

NOTE

The actual buffer size should be greater than or equal to 10 bytes.

Rx Buffer Pointer

This pointer contains the address of the associated data buffer. The buffer may reside in either internal or external memory.

NOTE

The Rx buffer pointer must be even, and the upper 8 bits of the pointer must be zero for the function codes to operate correctly.

4.5.15.8 V.110 Transmit Buffer Descriptor (Tx BD)

Data is presented to the CP for transmission on an SCC channel by arranging it in buffers referenced by the channel's Tx BD table. The CP confirms transmission (or indicates error conditions) using the BDs to inform the M68000 core whether the buffers have been serviced. The Tx BD is shown in Figure 4-41.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET + 0	E	X	W	I	L	0	—	—	—	—	—	—	—	—	UN	—
OFFSET + 2	DATA LENGTH															
OFFSET + 4	TX BUFFER POINTER (24-bits used, upper 8 bits must be 0)															
OFFSET +6																

Figure 4-41. V.110 Transmit Buffer Descriptor

The first word contains status and control bits. Bits 15–10 are prepared by the user before transmission. Bit 1 is set by the V.110 controller after the buffer has been transmitted. Bit 15 is set by the user and cleared by the V.110 controller.

R—Ready

0 = This buffer is not currently ready for transmission. The user is free to manipulate this BD and its associated buffer. The V.110 controller clears this bit after the buffer has been fully transmitted (or after an error condition is encountered).
1 = The data buffer has been prepared for transmission by the user (but not yet transmitted). No fields of this BD may be written by the user once this bit is set.

X—External Buffer

0 = The buffer associated with this BD is in internal dual-port RAM.
1 = The buffer associated with this BD is in external memory.

W—Wrap (Final BD in Table)

0 = This is not the last BD in the Tx BD table.
1 = This is the last BD in the Tx BD table. After this buffer has been used, the V.110 controller will transmit data from the first BD in the table.

NOTE

The user is required to set the wrap bit in one of the first eight BDs; otherwise, errant behavior may occur.

I—Interrupt

0 = No interrupt is generated after this buffer has been serviced.
1 = Either TX or TXE in the V.110 event register will be set when this buffer has been serviced by the V.110 controller, which can cause interrupts.

L—Last

0 = This buffer is not the last in the message.
1 = This bit is set by the processor to indicate that this buffer is the last buffer in the current frame. The V.110 controller will transmit ones until the next BD is ready.

Bit 10—Must be set to zero by the user.

Bits 9–2, 0—Reserved for future use.

The following bits are written by the V.110 controller after it has finished transmitting the associated data buffer.

UN—Underrun

The V.110 controller encountered a transmitter underrun condition while transmitting the associated data buffer.

Data Length

The data length is the number of octets that the V.110 controller should transmit from this BD's data buffer. It is never modified by the CP. The data length should be greater than zero.

Tx Buffer Pointer

This pointer, which contains the address of the associated data buffer, may be even or odd. The buffer may reside in either internal or external memory.

NOTE

For correct operation of the function codes, the upper 8 bits of the pointer must be initialized to zero.

4.5.15.9 V.110 Event Register

The SCC event register (SCCE) is referred to as the V.110 event register when the SCC is configured as a V.110 controller. It is an 8-bit register used to report events recognized by the V.110 channel and to generate interrupts. On recognition of an event, the V.110 control-

ler sets its corresponding bit in this register. Interrupts generated by this register may be masked in the V.110 mask register.

The V.110 event register is a memory-mapped register that may be read at any time. A bit is cleared by writing a one (writing a zero does not affect a bit's value). More than one bit may be cleared at a time. All unmasked bits must be cleared before the CP will clear the internal interrupt request signal. This register is cleared at reset.

7	6	5	4	3	2	1	0
—	—	—	TXE	RXF	BSY	TX	—

Bits 7–5, 0—Reserved for future use.

TXE—Tx Error

An error (underrun) occurred on the transmitter channel.

RXF—Receive Frame

A complete frame has been received on the V.110 channel.

BSY—Busy Condition

A data byte was received and discarded due to lack of buffers. The receiver will automatically enter hunt mode.

TX —Tx Buffer

A buffer has been transmitted.This bit is set on the second to last bit of an 80-bit frame.

4.5.15.10 V.110 Mask Register

The SCC mask register (SCCM) is referred to as the V.110 mask register when the SCC is operating as a V.110 controller. It is an 8-bit read-write register that has the same bit format as the V.110 event register. If a bit in the V.110 mask register is a one, the corresponding interrupt in the event register will be enabled. If the bit is zero, the corresponding interrupt in the event register will be masked. This register is cleared upon reset.

4.5.16 Transparent Controller

The transparent controller allows transmission and reception of serial data over an SCC without any modification to that data stream. Transparent mode provides a clear channel on which no bit-level manipulation is performed by the SCC. Any protocol run over transparent mode is performed in software. The job of an SCC in transparent mode is to function simply as a high-speed serial-to-parallel and parallel-to-serial converter. This mode is also referred to as totally transparent or promiscuous operation.

There are several basic applications for transparent mode. First, some data may need to be moved serially but requires no protocol superimposed. An example of this is voice data. Second, some board-level applications require a serial-to-parallel and parallel-to-serial conversion. Often this conversion is performed to allow communication between chips on the same board. The SCCs on the MC68302 can do this very efficiently with very little M68000 core intervention. Third, some applications require the switching of data without interfering with

the protocol encoding itself. For instance, in a multiplexer, data from a high-speed time-multiplexed serial stream is multiplexed into multiple low-speed data streams. The concept is to switch the data path but not alter the protocol encoded on that data path.

By appropriately setting the SCC mode register, any of the SCC channels can be configured to function as a transparent controller. Transparent mode is achieved by setting the SCM MODE1–MODE0 bits to 11 and setting the NTSYN bit (bit 13) to 1. Note that, if the NTSYN bit is cleared, normal BISYNC operation will occur rather than transparent operation. See 4.5.13 BISYNC Controller for a description of BISYNC operation.

The SCC in transparent mode can work with IDL, GCI (IOM-2), PCM highway, or NMSI interfaces. When the SCC in transparent mode is used with a modem interface (NMSI), the SCC outputs are connected directly to the external pins. The modem interface uses seven dedicated pins: transmit data (TXD), receive data (RXD), receive clock (RCLK), transmit clock (TCLK), carrier detect or carrier detect sync ($\overline{\text{CD}}$), clear to send ($\overline{\text{CTS}}$), and request to send ($\overline{\text{RTS}}$).

The transparent controller consists of separate transmit and receive sections whose operations are asynchronous with the M68000 core and may be either synchronous or asynchronous with respect to the other SCCs. Transparent mode on the MC68302 is a synchronous protocol; thus, a clock edge must be provided with each bit of data received or transmitted. Each clock can be supplied from either the internal baud rate generator or from external pins. More information on the baud rate generator is available in 4.5.2 SCC Configuration Register (SCON).

The main transparent controller features are as follows:

- Flexible Data Buffers
- External Sync Pin or BISYNC-Like Frame Sync on Receive
- Reverse Data Mode
- Interrupts on Buffers Transmitted or Received
- Clear to Send and Carrier Detect Lost Reporting
- Maskable Interrupt Available on Each Character Received
- Three Commands

4.5.16.1 Transparent Channel Buffer Transmission Processing

When the M68000 core enables the transparent transmitter, it will start transmitting ones. The transparent controller then polls the first BD in the transmit channel's BD table approximately every 16 transmit clocks. When there is a buffer to transmit, the transparent controller will fetch the data from memory and start transmitting the buffer. Transmission will not begin until the internal transmit FIFO is preloaded and the SCC achieves synchronization. See 4.5.16.5 Transparent Synchronization for details of the synchronization process.

When a BD's data is completely transmitted, the last bit (L) is checked in the BD. If the L bit is cleared, then the transmitter moves immediately to the next buffer to begin its transmission, with no gap on the serial line between buffers. Failure to provide the next buffer in time results in a transmit underrun, causing the TXE bit in the transparent event register to be set.

If the L bit is set, the frame ends, and the transmission of ones resumes until a new buffer is made ready. $\overline{RTS}$ is negated during this period. Regardless of whether or not the next buffer is available immediately, the next buffer will not begin transmission until achieving synchronization.

The transmit buffer length and starting address may be even or odd; however, since the transparent transmitter reads a word at a time, better performance can be achieved with an even buffer length and starting address. For example, if a transmit buffer begins on an odd-byte boundary and is 10 bytes in length (the worst case), six word reads will result, even though only 10 bytes will be transmitted.

Any whole number of bytes may be transmitted. If the REVD bit in the transparent mode register is set, each data byte will be reversed in its bit order before transmission.

If the interrupt (I) bit in the Tx BD is set, then the TX bit will be set in the transparent event register following the transmission of the buffer. The TX bit can generate a maskable interrupt.

4.5.16.2 Transparent Channel Buffer Reception Processing

When the M68000 core enables the transparent receiver, it will enter hunt mode. In this mode, it waits to achieve synchronization before receiving data. See 4.5.16.5 Transparent Synchronization for details.

Once data reception begins, the transparent receiver begins moving data from the receive FIFO to the receive buffer, always moving a 16-bit word at a time. After each word is moved to memory, the RCH bit in the transparent event register is set, which can generate a maskable interrupt, if desired. The transparent receiver continues to move data to the receive buffer until the buffer is completely full, as defined by the byte count in MRBLR. The receive buffer length (stored in MRBLR) and starting address must always be even, so the minimum receive buffer length must be 2.

After a buffer is filled, the transparent receiver moves to the next Rx BD in the table and begins moving data to its associated buffer. If the next buffer is not available when needed, a busy condition is signified by the setting of the BSY bit in the transparent event register, which can generate a maskable interrupt.

Received data is always packed into memory a word at a time, regardless of how it is received. For example, in NMSI mode, the first word of data will not be moved to the receive buffer until after the sixteenth receive clock occurs. In PCM highway mode, the same principle applies except that the clocks are only internally active during an SCC time slot. For example, if each SCC time slot is seven bits long, the first word of data will not be moved to the receive buffer until after the second bit of the third time slot, regardless of how much time exists between individual time slots.

Once synchronization is achieved for the receiver, the reception process continues unabated until a busy condition occurs, a $\overline{CD}$ lost condition occurs, or a receive overrun occurs. The busy condition error should be followed by an ENTER HUNT MODE command to the

channel. In all three error cases, the reception process will not proceed until synchronization has once again been achieved.

If the REVD bit in the transparent mode register is set, each data byte will be reversed in its bit order before it is written to memory.

If the interrupt (I) bit in the Rx BD is set, then the RX bit will be set in the transparent event register following the reception of the buffer. The RX bit can generate a maskable interrupt.

4.5.16.3 Transparent Memory Map

When configured to operate in transparent mode, the IMP overlays the structure illustrated in Table 4-11 onto the protocol specific area of that SCC parameter RAM. Refer to 2.8 MC68302 Memory Map for the placement of the three SCC parameter RAM areas and Table 4-5 for the other parameter RAM values.

Table 4-11. Transparent-Specific Parameter RAM

Address	Name	Width	Description
SCC BASE + 9C	RES	WORD	Reserved
SCC BASE + 9E	RES	WORD	Reserved
SCC BASE + A0	RES	WORD	Reserved
SCC BASE + A2	RES	WORD	Reserved
SCC BASE + A4	RES	WORD	Reserved
SCC BASE + A6	RES	WORD	Reserved
SCC BASE + A8	RES	WORD	Reserved
SCC BASE + AA	RES	WORD	Reserved
SCC BASE + AC	RES	WORD	Reserved
SCC BASE + AE	RES	WORD	Reserved
SCC BASE + B0	RES	WORD	Reserved
SCC BASE + B2	RES	WORD	Reserved
SCC BASE + B4	RES	WORD	Reserved
SCC BASE + B6	RES	WORD	Reserved
SCC BASE + B8	RES	WORD	Reserved
SCC BASE + BA	RES	WORD	Reserved
SCC BASE + BC	RES	WORD	Reserved
SCC BASE + BE	RES	WORD	Reserved

Although there are no transparent-specific parameter RAM locations that must be initialized by the user, the general SCC parameter RAM must still be initialized (see Table 4-5).

The transparent controller uses the same basic data structure as the other protocol controllers. Receive and transmit errors are reported through receive and transmit BDs. The status of the line is reflected in the SCC status register, and a maskable interrupt is generated upon each status change.

If in-line synchronization is used with the transparent controller, then the DSR (see 4.5.4 SCC Data Synchronization Register (DSR)) must be initialized with the SYN1–SYN2 synchronization characters. See 4.5.16.5 Transparent Synchronization for details.

4.5.16.4 Transparent Commands

The following commands are issued to the command register.

STOP TRANSMIT Command

After a hardware or software reset and the enabling of the channel using the SCC mode register, the channel is in the transmit enable mode and starts polling the first BD in the table approximately every 16 transmit clocks.

The STOP TRANSMIT command aborts transmission. If this command is received by the transparent controller during a buffer transmission, transmission of that buffer is aborted after the FIFO contents (up to four words) are transmitted. The TBD# is not advanced. Ones are continuously transmitted until transmission is re-enabled by issuing the RESTART TRANSMIT command.

The STOP TRANSMIT command must be issued before the SCC mode register is used to disable the transmitter if the transmitter is to be re-enabled at a later time.

RESTART TRANSMIT Command

The RESTART TRANSMIT command is used to begin or resume transmission from the current Tx BD number (TBD#) in the channel's Tx BD table. When this command is received by the channel, it will start polling the ready bit in this BD. This command is expected by the transparent controller after a STOP TRANSMIT command, after a STOP TRANSMIT command and the disabling of the channel in its mode register, or after a transmitter error (underrun or CTS lost occurs).

If the transmitter is being re-enabled, the RESTART TRANSMIT command must be used and should be followed by the enabling of the transmitter in the SCC mode register.

ENTER HUNT MODE Command

After a hardware or software reset and the enabling of the channel in the SCC mode register, the channel is in the receive enable mode and will use the first BD in the table.

The ENTER HUNT MODE command is used to force the transparent controller to abort reception of the current block, generate an RX interrupt (if enabled) as the buffer is closed, and enter the hunt mode. In the hunt mode, the transparent controller waits for a synchronization to occur on the SCC (see 4.5.16.5 Transparent Synchronization). After receiving the ENTER HUNT MODE command, the current receive buffer is closed. Reception continues using the next BD.

If an enabled receiver has been disabled (by clearing ENR in the SCC mode register), the ENTER HUNT MODE command must be given to the channel before setting ENR again.

4.5.16.5 Transparent Synchronization

Once the SCC is enabled for transparent operation in the SCM, the transmit and receive buffer descriptors are made ready for the SCC, and the transmit FIFO has been preloaded by the SDMA channel (signaled by the $\overline{\text{RTS}}$ pin in NMSI and PCM modes), one additional process must occur before data can be transmitted and received. This process is called

transparent synchronization. Transparent synchronization gives the user bit-level control over when the transmission and reception can begin.

The method of synchronization is controlled by the DIAG1–DIAG0 bits in the SCM, the EXSYN bit in the SCM, and, in some cases, the data synchronization register (DSR). The resulting timing is dependent on the physical interface chosen.

NOTE

See D.8 Using the MC68302 Transparent Mode for timing diagrams and additional details concerning mode.

Five ways exist to achieve transparent synchronization.

1. With the physical interface in the NMSI mode, the SCC may be configured with the EXSYN bit set, and the DIAG1–DIAG0 bits set to software operation. In this case, the $\overline{CTS}$ pin is ignored, and the $\overline{CD}$ pin is used to control both transmission and reception. For the transmitter, once $\overline{RTS}$ is asserted and the transmitter samples $\overline{CD}$ as low, the transmission will begin after a fixed 6.5 transmit clock delay. For the receiver, the first valid bit of data received occurs one bit prior to the receive clock that sampled $\overline{CD}$ as low. Note that $\overline{CD}$ is sampled on a rising TCLK for the transmitter and a rising RCLK for the receiver.
   Once $\overline{CD}$ is sampled as low by the receiver and transmitter, further toggling of $\overline{CD}$ will have no effect since synchronization has already been achieved.
2. With the physical interface in NMSI mode, the SCC may be configured with the EXSYN bit cleared and the DIAG1–DIAG0 bits set to software operation. For the transmitter, the transmission will begin without any synchronization. For the receiver, reception will begin as soon as the receive data pattern matches the SYN1–SYN2 pattern programmed into the DSR. Thus, the receiver uses an in-line synchronization method.
3. If case 2 is used but the DIAG1–DIAG0 bits are set to normal operation, then the normal operation characteristics as described in the SCM register also apply. The transmitter will be controlled by the $\overline{CTS}$ pin, and the receiver will wait for the SYN1–SYN2 pattern once the $\overline{CD}$ pin is detected as low.

NOTE

In cases 2 and 3 above, the SYN2 character is written into the receive data buffer.

4. With the physical interface configured for PCM highway mode, the SCC may be configured with the EXSYN bit set and the DIAG1–DIAG0 bits set to either software operation or normal operation. In this case, the L1SY1–L1SY0 pins carry out the synchronization. For the transmitter, once data is preloaded into the transmit FIFO, the rising edge of the L1SY1–L1SY0 pins will cause a transmission to occur. This transmission will be comprised of one leading $FF byte, followed by the first bit of the transmit buffer. For the receiver, reception will begin at the beginning of a time slot.

NOTE

This technique is not valid for the PCM envelope sync method when the time slots are less than six bits in length. In such a case, the user may clear EXSYN to cause transmission to begin, and then, for the receiver, provide the required SYN1–SYN2 sequence. To accomplish this, the user may configure the SCC to loopback mode with the EXSYN bit cleared and the DSR set to $FFFF. Then after 16 serial clocks, the receiver and transmitter are synchronized, and the SCC may be dynamically reconfigured to normal or software operation. At this point, reception begins immediately, and transmission begins after the transmit BD is made ready.

5. With the physical interface configured for IDL or GCI mode, the SCC may be configured with the EXSYN bit set and the DIAG1–DIAG0 bits set to either software operation or normal operation. In this case, the data will be byte-aligned to the B or D channel time slots.

Once synchronization is achieved for the transmitter, it will remain in effect until an error occurs, a STOP TRANSMIT command is given, or a buffer has completed transmission with the Tx BD last (L) bit set. Once synchronization is achieved for the receiver, it will remain in effect until an error occurs or the ENTER HUNT MODE command is given.

4.5.16.6 Transparent Error-Handling Procedure

The transparent controller reports message reception and transmission error conditions using the channel BDs and the transparent event register. The modem interface lines can also be directly monitored in the SCC status register.

Transmission Errors:

1. Transmitter Underrun—When this error occurs, the channel terminates buffer transmission, closes the buffer, sets the underrun (UN) bit in the BD, and generates the TXE interrupt (if enabled). The channel resumes transmission after the reception of the RESTART TRANSMIT command. Underrun can occur after a transmit frame for which the L bit in the Tx BD was not set. In this case, only the TXE bit is set. The FIFO size is four words in transparent mode.
2. Clear-To-Send Lost During Message Transmission—When this error occurs and the channel is not programmed to control this line with software, the channel terminates buffer transmission, closes the buffer, sets the CTS lost (CT) bit in the BD, and generates the TXE interrupt (if enabled). The channel will resume transmission after the reception of the RESTART TRANSMIT command.

Reception Errors:

1. Overrun Error—The transparent controller maintains an internal three-word FIFO for receiving data. The CP begins programming the SDMA channel (if the data buffer is in external memory) when the first word is received into the FIFO. If a FIFO overrun occurs, the transparent controller writes the received data word to the internal FIFO over the previously received word. The previous word is lost. Next, the channel closes

the buffer, sets the overrun (OV) bit in the BD, and generates the RX interrupt (if enabled). The receiver then enters hunt mode immediately.

2. Carrier Detect Lost During Message Reception—When this error occurs and the channel is not programmed to control this line with software, the channel terminates reception, closes the buffer, sets the carrier detect lost (CD) bit in the BD, and generates the RX interrupt (if enabled). This error has the highest priority; the rest of the message is lost and no other errors are checked. The receiver then enters hunt mode immediately.
3. Busy Condition—If the RISC controller tries to use an Rx BD that is not empty, the busy condition is encountered. No data is received and the current Rx BD is left unmodified. After new buffers are provided, the user should issue the ENTER HUNT MODE command.

4.5.16.7 Transparent Mode Register

Each SCC mode register is a 16-bit, memory-mapped, read-write register that controls the SCC operation. The term transparent mode register refers to the protocol-specific bits (15–6) of the SCC mode register when that SCC is configured for transparent mode. The transparent mode register is cleared by reset. All undefined bits should be written with zero.

15	14	13	12	11	10	9	8	7	6	5 0
—	EXSYN	NTSYN	REVD	—	—	—	—	—	—	COMMON SCC MODE BITS

Bit 15—Reserved for future use; should be written with zero.

EXSYN — External Sync Mode

When this mode is selected, the receiver and transmitter expect external logic to indicate the beginning of the data field by using the $\overline{CD1}$/L1SY1 pin, if SCC1 is used, and the $\overline{CD2}$ and $\overline{CD3}$ pins, respectively, if SCC2 or SCC3 is used. In this mode, there is no carrier detect function for the SCC.

When the channel is programmed to work through the serial channels physical interface (IDL or GCI) and EXSYN is set, the layer 1 logic carries out the synchronization using the L1SY1 pin. In PCM mode, the L1SY1–L1SY0 pins are used. In NMSI mode, the $\overline{CD}$ pins (and the $\overline{CD}$ timing) are used to synchronize the data. $\overline{CD}$ should go low on the second valid data bit of the receive data stream.

If this bit is cleared, the receiver will look for the SYN1–SYN2 sequence in the data synchronization register to achieve synchronization, and the transmitter uses the $\overline{CTS}$ pin according to the DIAG1–DIAG0 bits in the SCM. The receiver also uses the $\overline{CD}$ pin according to the DIAG1–DIAG0 bits in the SCM.

NTSYN—No Transmit SYNC

This bit must be set for the SCC to operate in a totally transparent (promiscuous) mode.

REVD—Reverse Data

When this bit is set, the receiver and transmitter will reverse the character bit order, transmitting the most significant bit first.

Bits 11–6—Reserved for future use; should be written with zero.

COMMON SCC MODE BITS—See 4.5.3 SCC Mode Register (SCM) for a description of the DIAG1, DIAG0, ENR, ENT, MODE1, and MODE0 bits.

4.5.16.8 Transparent Receive Buffer Descriptor (RxBD)

The CP reports information about the received data for each buffer using BD. The Rx BD is shown in Figure 4-42. The CP closes the current buffer, generates a maskable interrupt, and starts to receive data into the next buffer after one of the following events:

- Detecting an error
- Detecting a full receive buffer
- Issuing the ENTER HUNT MODE command

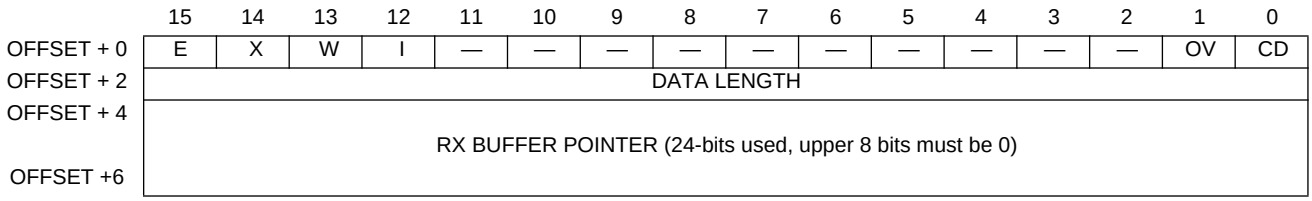


Figure 4-42. Transparent Receive Buffer Descriptor

The first word of the Rx BD contains control and status bits.

E—Empty

0 = The data buffer associated with this BD has been filled with received data, or data reception has been aborted due to an error condition. The M68000 core is free to examine or write to any fields of this BD.

1 = The data buffer associated with this BD is empty. This bit signifies that the BD and its associated buffer are available to the CP. After it sets this bit, the M68000 core should not write to any fields of this BD when this bit is set. The empty bit will remain set while the CP is currently filling the buffer with received data.

X—External Buffer

0 = The buffer associated with this BD is in internal dual-port RAM.

1 = The buffer associated with this BD is in external memory.

W—Wrap (Final BD in Table)

0 = This is not the last BD in the Rx BD table.

1 = This is the last BD in the Rx BD table. After this buffer has been used, the CP will receive incoming data into the first BD in the table. Setting this bit allows the use of fewer than eight BDs to conserve internal RAM.

NOTE

The user is required to set the wrap bit in one of the first eight BDs; otherwise, errant behavior may occur.

I—Interrupt

0 = No interrupt is generated after this buffer has been used.
1 = When this buffer has been closed by the transparent controller, the RX bit in the transparent event register will be set, which can cause an interrupt.

The following status bits are written by the CP after the received data has been placed into the associated data buffer.

Bits 11–2—Reserved for future use. Should be written with zero by the user.

OV—Overrun

A receiver overrun occurred during reception.

CD—Carrier Detect Lost

The carrier detect signal was negated during buffer reception.

Data Length

The data length is the number of octets that the CP has written into this BD's data buffer. It is written only once by the CP as the buffer is closed.

NOTE

The actual buffer size should be greater than or equal to the MRBLR.

Rx Buffer Pointer

The receive buffer pointer, which always points to the first location of the associated data buffer, must be even. The buffer may reside in either internal or external memory.

NOTE

For correct operation of the function codes, the upper 8 bits of the pointer must be initialized to zero.

4.5.16.9 Transparent Transmit Buffer Descriptor (Tx BD)

Data is presented to the CP for transmission on an SCC channel by arranging it in buffers referenced by the channel's Tx BD table. The CP confirms transmission (or indicates error conditions) using the BDs to inform the processor that the buffers have been serviced. The Tx BD is shown in Figure 4-43.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFSET + 0	R	X	W	I	L	—	—	—	—	—	—	—	—	—	UN	CT
OFFSET + 2	DATA LENGTH															
OFFSET + 4	TX BUFFER POINTER (24-bits used, upper 8 bits must be 0)															
OFFSET +6																

Figure 4-43. Transparent Transmit Buffer Descriptor

The first word of the Tx BD contains status and control bits. These bits are prepared by the user before transmission and are set by the CP after the buffer has been transmitted.

R—Ready

0 = This buffer is not currently ready for transmission. The user is free to manipulate this BD (or its associated buffer). The CP clears this bit after the buffer has been fully transmitted or after an error condition has been encountered.
1 = The data buffer has been prepared for transmission by the user (but not yet transmitted). No fields of this BD may be written by the user once this bit is set.

X—External Buffer

0 = The buffer associated with this BD is in internal dual-port RAM.
1 = The buffer associated with this BD is in external memory.

W—Wrap (Final BD in Table)

0 = This is not the last BD in the Tx BD table.
1 = This is the last BD in the Tx BD table. After this buffer has been used, the CP will transmit data from the first BD in the table.

NOTE

The user is required to set the wrap bit in one of the first eight BDs; otherwise, errant behavior may occur.

I—Interrupt

0 = No interrupt is generated after this buffer has been serviced.
1 = When this buffer is serviced by the CP, the TX or TXE bit in the transparent event register will be set, which can cause an interrupt.

L—Last in Message

0 = The last byte in the buffer is not the last byte in the transmitted block. Data from the next transmit buffer (if ready) will be transmitted immediately following the last byte of this buffer.
1 = The last byte in the buffer is the last byte in the transmitted block. After this buffer is transmitted, the transmitter will require synchronization before the next buffer can be transmitted.

Bits 10—2 are reserved for future use; they should be written with zero.

The following status bits are written by the CP after it has finished transmitting the associated data buffer.

UN—Underrun

The transparent controller encountered a transmitter underrun condition while transmitting the associated data buffer.

CT—CTS Lost

CTS in NMSI mode or L1GR in IDL/GCI mode was lost during frame transmission.

Data Length

The data length is the number of octets that the CP should transmit from this BD's data buffer. The data length, which should be greater than zero, may be even or odd. This value is never modified by the CP.

Tx Buffer Pointer

The transmit buffer pointer, which always points to the first byte of the associated data buffer, may be even or odd. The buffer may reside in either internal or external memory.

NOTE

For correct operation of the function codes, the upper 8 bits of the pointer must be initialized to zero.

4.5.16.10 Transparent Event Register

The SCC event register (SCCE) is referred to as the transparent event register when the SCC is programmed as a transparent controller. It is an 8-bit register used to report events recognized by the transparent channel and to generate interrupts. On recognition of an event, the transparent controller sets the corresponding bit in the transparent event register. Interrupts generated by this register may be masked in the transparent mask register.

The transparent event register is a memory-mapped register that may be read at any time. A bit is cleared by writing a one (writing a zero does not affect a bit's value). More than one bit may be cleared at a time. All unmasked bits must be cleared before the CP will negate the internal interrupt request signal. This register is cleared at reset.

7	6	5	4	3	2	1	0
CTS	CD	—	TXE	RCH	BSY	TX	RX

CTS—Clear-To-Send Status Changed

A change in the status of the serial line was detected on the transparent channel. The SCC status register may be read to determine the current status.

CD—Carrier Detect Status Changed

A change in the status of the serial line was detected on the transparent channel. The SCC status register may be read to determine the current status.

Bit 5—Reserved for future use.

TXE—Tx Error

An error (CTS lost or underrun) occurred on the transmitter channel.

RCH—Receive Character

A word has been received and written to the receive buffer.

BSY—Busy Condition

A word was received and discarded due to lack of buffers. The receiver will resume reception after an ENTER HUNT MODE command.

TX—Tx Buffer

A buffer has been transmitted. If the L bit in the Tx BD is set, TX is set no sooner than on the second-to-last bit of the last byte being transmitted on the TXD pin. If the L bit in the Tx BD is cleared, TX is set after the last byte was written to the transmit FIFO.

RX—Rx Buffer

A complete buffer has been received on the transparent channel. RX is set no sooner than 10 serial clocks after the last bit of the last byte in the buffer is received on the RXD pin.

4.5.16.11 Transparent Mask Register

The SCC mask register (SCCM) is referred to as the transparent mask register when the SCC is operating as a transparent controller. It is an 8-bit read-write register that has the same bit format as the transparent event register. If a bit in the transparent mask register is a one, the corresponding interrupt in the event register will be enabled. If the bit is zero, the corresponding interrupt in the event register will be masked. This register is cleared at reset.

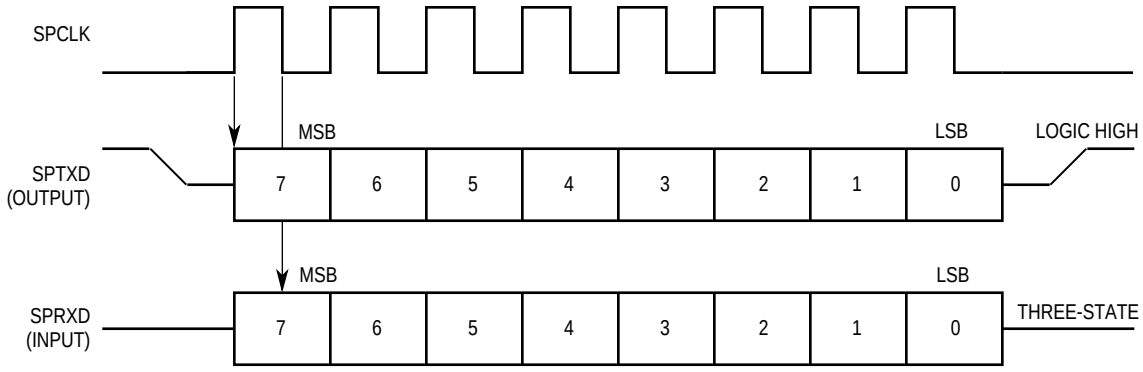
4.6 SERIAL COMMUNICATION PORT (SCP)

The SCP (see Figure 4-44) is a full-duplex, synchronous, character-oriented channel that provides a three-wire interface (receive, transmit, and clock). The SCP consists of independent transmitter and receiver sections and a common clock generator. The transmitter and receiver sections use the same clock, which is derived from the main clock by a separate on-chip baud rate generator. Since the MC68302 is an SCP master for this serial channel, it generates both the enable and the clock signals.

The SCP allows the MC68302 to exchange status and control information with a variety of serial devices, using a subset of the Motorola serial peripheral interface (SPI). The SCP is compatible with SPI slave devices. These devices include industry-standard CODECs as well as other microcontrollers and peripherals.

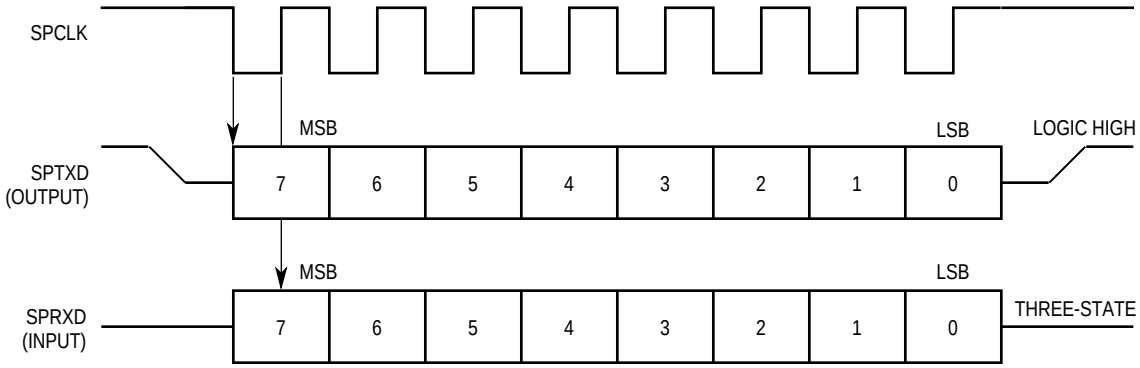
The SCP enable signals, which can be implemented using the general-purpose I/O pins, are used to enable one of several potential SCP slave devices. The clock signal (SPCLK) shifts the received data (SPRXD) in and shifts the transmitted data (SPTXD) out. The clock is gated; it operates only while data is being transferred and is idle otherwise.

Two successive byte transmissions over the SCP cannot occur immediately back-to-back. A minimum delay of two to eight bit times is imposed by the SCP, depending on the SCP clock rate (Communication processor priorities and software handling of interrupts may contribute extra delays). Higher SCP clock rates give higher minimum delay.



NOTE: Transmitted data bits shift on rising edges; received bits are sampled on falling edges.

(a) CI=0



NOTE: Transmitted data bits shift on falling edges; received bits are sampled on rising edges.

(b) CI=1

Figure 4-44. SCP Timing

The SCP can be configured to operate in a local loopback mode, which is useful for local diagnostic functions.

Note that the least significant bit of the SCP is labeled as data bit 0 on the serial line; whereas, other devices, such as the MC145554 CODEC, may label the most significant bit as data bit 0. The MC68302 SCP bit 7 (most significant bit) is shifted out first.

The SCP key features are as follows:

- Three-Wire Interface (SPTXD, SPRXD, and SPCLK)
- Full-Duplex Operation
- Clock Rate up to 4.096 MHz
- Programmable Clock Generator
- Local Loopback Capability for Testing

4.6.1 SCP Programming Model

The SCP mode register consists of the upper eight bits of SPMODE. The SCP mode register, an internal read-write register that controls both the SCP operation mode and clock source, is cleared by reset.

15	14	13	12	11	10	9	8
STR	LOOP	CI	PM3	PM2	PM1	PM0	EN

STR—Start Transmit

When set, this bit causes the SCP controller to transmit eight bits from the SCP transmit/receive buffer descriptor (BD) and to receive eight bits of data in this same BD. This bit is cleared automatically after one system clock cycle.

LOOP—Loop Mode

When set, the loop mode bit selects local loopback operation. The ones complement of the transmitter output is internally connected to the receiver input; the receiver and transmitter operate normally except that SPRXD is ignored. When cleared, this bit selects normal operation.

CI—Clock Invert

When set, the CI bit inverts the SCP clock polarity. When CI is zero, transmitted data bits shift on rising clock edges, and received bits are sampled on falling edges. When the SCP is idle, the clock is low. While CI is one, transmitted data bits are shifted on falling edges, and received bits are sampled on rising edges. In this case, when the SCP is idle, the clock is high.

PM3–PM0—Prescale Modulus Select

The prescale modulus select bits specify the divide ratio of the prescale divider in the SCP clock generator. The divider value is 4*(“PM3–PM0” + 1) giving a clock divide ratio of 4 to 64 in multiples of 4. With a 16.384-MHz system clock, the maximum SCP clock is 4.096 MHz.

EN—Enable SCP

When set, this bit enables the SCP operation and connects the external pins SPRXD/$\overline{\text{CTS3}}$, SPTXD/$\overline{\text{RTS3}}$, and SPCLK/$\overline{\text{CD3}}$ internally to the SCP (see Figure 4-45). When cleared, the SCP is put into a reset state consuming minimal power, and the three pins are connected back to SCC3.

NOTE

When the DIAG1–DIAG0 bits of SCC3 are programmed to normal operation control of the $\overline{\text{CTS}}$ and $\overline{\text{CD}}$ lines and the ENT or ENR bits of SCC3 are set, the user may not modify the EN bit.

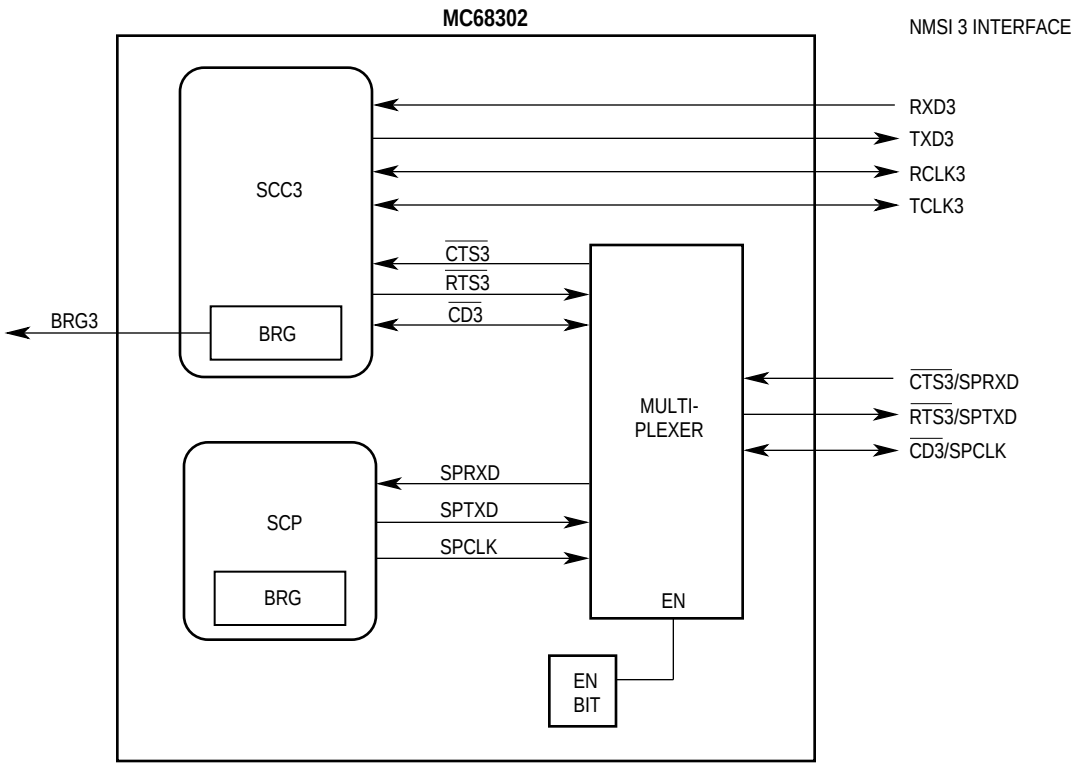


Figure 4-45. SCP vs. SCC Pin Multiplexing

4.6.2 SCP Transmit/Receive Buffer Descriptor

The transmit/receive BD contains the data to be transmitted (written by the M68000 core) and the received data (written by the SCP). The done (D) bit indicates that the received data is valid and is cleared by the SCP.

15	14 … 8	7 … 0
D	RESERVED	DATA

4.6.3 SCP Transmit/Receive Processing

The IMP SCP always functions in the master mode. Thus, in a typical exchange of messages, the IMP transmits a message to an external peripheral (SCP slave) which, in turn, sends back a reply. When the IMP works with more than one slave, it can use the general-purpose parallel I/O pins as enable (select) signals. To begin the data exchange, the M68000 core writes the data to be transmitted into the transmit/receive BD, and sets the done bit. The M68000 core should then set the start transmit (STR) bit in the SPMODE register to start transmission of data. STR is cleared by hardware after one system clock cycle.

Upon recognizing the STR bit, the SCP also begins receiving eight bits of data. It writes the data into the transmit/receive BD, clears the done bit, and issues a maskable interrupt to the IMP interrupt controller. When working in a polled environment, the done bit should be set

by the M68000 core before setting the STR bit so that received replies may be easily recognized by the software.

4.7 SERIAL MANAGEMENT CONTROLLERS (SMCS)

The SMC key features are as follows:

- Two Modes of Operation:
  - —IDL—SMC1 supports the maintenance channel and SMC2 supports the auxiliary channel
  - —GCI (IOM-2)—SMC1 supports the monitor channel and SMC2 supports the C/I channel
- Full-Duplex Operation
- Local Loopback Capability for Testing

4.7.1 Overview

The SMCs are two synchronous, full-duplex serial management control (SMC) ports. The SMC ports may be configured to operate in either Motorola interchip digital link (IDL) or general circuit interface (GCI) modes. GCI is also known as ISDN oriented modular 2 (IOM-2). See 4.4 Serial Channels Physical Interface for the details of configuring the IDL and GCI interfaces. The SMC ports are not used when the physical serial interface is configured for PCM highway or NMSI modes.

4.7.1.1 Using IDL with the SMCs

In this mode, SMC1 transfers the maintenance (M) bits of the IDL to and from the internal RAM, and SMC2 transfers the auxiliary (A) bits to and from the internal RAM. The CP generates a maskable interrupt upon reception/transmission of eight bits. The SMC1 and SMC2 receivers can be programmed to work in hunt-on-zero mode, in which the receiver will search the line signals for a zero bit. When it is found, the receiver will transfer data to the internal RAM.

4.7.1.2 Using GCI with the SMCs

In this mode, SMC1 controls the GCI monitor channel.

SMC1 Transmission

The monitor channel is used to transfer commands to the layer-1 component. The M68000 core writes the data byte into the SMC1 Tx BD. SMC1 will transmit the data on the monitor channel.

The SMC1 channel transmitter can be programmed to work in one of two modes:

Transparent Mode

In this mode, SMC1 transmits the monitor channel data and the A and E control bits transparently into the channel. When the M68000 core has not written new data to the buffer, the SMC1 transmitter will retransmit the previous monitor channel data and the A and E control bits.

Monitor Channel Protocol

In this mode, SMC1 transmits the data and handles the A and E control bits according to the GCI monitor channel protocol. When using the monitor channel protocol, the user may issue the TIMEOUT command to solve deadlocks in case of bit errors in the A and E bit positions on data line. The IMP will transmit an abort on the E bit.

SMC1 Reception

The SMC1 receiver can be programmed to work in one of two modes:

Transparent Mode

In this mode, SMC1 receives the data, moves the A and E control bits transparently into the SMC1 receive BD, and generates a maskable interrupt. The SMC1 receiver discards new data when the M68000 core has not read the receive BD.

Monitor Channel Protocol

In this mode, SMC1 receives data and handles the A and E control bits according to the GCI monitor channel protocol. When a received data byte is stored by the CP in the SMC1 receive BD, a maskable interrupt is generated.

When using the monitor channel protocol, the user may issue the TRANSMIT ABORT REQUEST command. The IMP will then transmit an abort request on the A bit.

SMC2 Controls the GCI Command/Indication (C/I) Channel

SMC2 Transmission

The M68000 core writes the data byte into the SMC2 Tx BD. SMC2 will transmit the data continuously on the C/I channel to the physical layer device.

SMC2 Reception

The SMC2 receiver continuously monitors the C/I channel. When a change in data is recognized and this value is received in two successive frames, it will be interpreted as valid data. The received data byte is stored by the CP in the SMC2 receive BD, and a maskable interrupt is generated.

The receive and transmit clocks are derived from the same physical clock (L1CLK) and are only active while serial data is transferred between the SMC controllers and the serial interface.

When SMC loopback mode is chosen, SMC transmitted data is routed to the SMC receiver. Transmitted data appears on the L1TXD pin, unless the SDIAG1–SDIAG0 bits in the SIMODE register are programmed to “loopback control” (see 4.4 Serial Channels Physical Interface).

4.7.2 SMC Programming Model

The operating mode of both SMC ports is defined by SMC mode, which consists of the lower eight bits of SPMODE. As previously mentioned, the upper eight bits program the SCP.

7	6	5	4	3	2	1	0
—	SMD3	SMD2	SMD1	SMD0	LOOP	EN2	EN1

Bit 7—This bit is reserved and should be set to zero.

SMD3–SMD0—SMC Mode Support

X00X = GCI—The monitor channel is not used.
001X = GCI—The monitor channel data and the A and E control bits are internally controlled according to the monitor channel protocol.
101X = GCI—The monitor channel data and the A and E control bits are received and transmitted transparently by the IMP.
X100 = IDL—The M and A channels are in hunt-on-zero mode.
X101 = IDL—Only the M channel is in hunt-on-zero mode.
X110 = IDL—Only the A channel is in hunt-on-zero mode.
X111 = IDL—Regular operation; no channel is in hunt-on-zero mode.

LOOP—Local Loopback Mode

0 = Normal mode
1 = Local loopback mode. In GCI mode, EN1 and EN2 must also be set.

EN2—SMC2 Enable

0 = Disable SMC2
1 = Enable SMC2

EN1—SMC1 Enable

0 = Disable SMC1
1 = Enable SMC1

4.7.3 SMC Commands

The following commands issued to the CP command register (see 4.3 Command Set) are used only when GCI is selected for the serial channels physical interface.

TRANSMIT ABORT REQUEST Command

This receiver command may be issued when the IMP implements the monitor channel protocol. When issued, the IMP sends an abort request on the A bit.

TIMEOUT Command

This transmitter command may be issued when the IMP implements the monitor channel protocol. It is issued because the device is not responding or because GCI A bit errors are detected. When issued, the IMP sends an abort request on the E bit.

4.7.4 SMC Memory Structure and Buffers Descriptors

The CP uses several memory structures and memory-mapped registers to communicate with the M68000 core. All the structures detailed in the following paragraphs reside in the dual-port RAM of the IMP (see Figure 3-4). The SMC buffer descriptors allow the user to define one data byte at a time for each transmit channel and receive one data byte at a time for each receive channel.

4.7.4.1 SMC1 Receive Buffer Descriptor

The CP reports information about the received byte using this (BD).

15	14	13	12	11 10	9	8	7 0
E	L	ER	MS	—	AB	EB	DATA

E—Empty

0 = This bit is cleared by the CP to indicate that the data byte associated with this BD is now available to the M68000 core.

1 = This bit is set by the M68000 core to indicate that the data byte associated with this BD is empty.

In GCI mode, when the IMP implements the monitor channel protocol, the IMP will wait until this bit is set by the M68000 core before acknowledging the monitor channel data. In other modes (transparent GCI and IDL), additional received data bytes will be discarded until the empty bit is set by the M68000 core.

L—Last (EOM)

This bit is valid only in GCI mode when the IMP implements the monitor channel protocol. This bit is set when the end-of-message (EOM) indication is received on the E bit.

NOTE

When this bit is set, the data byte is not valid.

ER—Error Condition

This bit is valid only in GCI mode when the IMP implements the monitor channel protocol and the L bit is set. This bit is set when an error condition occurs on the monitor channel protocol. A new byte is transmitted before the IMP acknowledges the previous byte.

MS—Data Mismatch

This bit is valid only in GCI mode when the IMP implements the monitor channel protocol. This bit is set when two different consecutive bytes are received and is cleared when the last two consecutive bytes match. The IMP waits for the reception of two identical consecutive bytes before writing new data to the receive BD.

Bits 11–10—Reserved for future use.

AB—Received A Bit

This bit is valid only in GCI mode when the monitor channel is in transparent mode.

EB—Received E Bit

This bit is valid only in GCI mode when the monitor channel is in transparent mode.

Data—Data Field

The data field contains the byte of data received by SMC1.

4.7.4.2 SMC1 Transmit Buffer Descriptor

The CP reports information about this transmit byte through the BD.

15	14	13	12 — 10	9	8	7 — 0
R	L	AR	—	AB	EB	DATA

R—Ready

0 = This bit is cleared by the CP after transmission. The Tx BD is now available to the M68000 core.

1 = This bit is set by the M68000 core to indicate that the data byte associated with this BD is ready for transmission.

In GCI mode, when the IMP implements the monitor channel protocol, it will clear this bit after receiving an acknowledgment on the A bit. When the SMC1 data should be transmitted and this bit is cleared, the channel will retransmit the previous data until new data is provided by the M68000 core.

L—Last (EOM)

This bit is valid only in GCI mode when the IMP implements the monitor channel protocol. When this bit is set, the SMC1 channel will transmit the buffer's data and then the end of message (EOM) indication on the E bit.

AR—Abort Request

This bit is valid only in GCI mode when the IMP implements the monitor channel protocol. This bit is set by the IMP when an abort request was received on the A bit. The SMC1 transmitter will transmit EOM on the E bit.

Bits 12–10—Reserved for future use.

AB—Transmit A Bit Value

This bit is valid only in GCI mode when the monitor channel is in transparent mode.

EB—Transmit E Bit Value

This bit is valid only in GCI mode when the monitor channel is in transparent mode.

Data—Data Field

The data field contains the data to be transmitted by SMC1.

4.7.4.3 SMC2 Receive Buffer Descriptor

In the IDL mode, this BD is identical to the SMC1 receive BD. In the GCI mode, SMC2 is used to control the C/I channel.

15	14 — 6	5 — 2	1	0
E	RESERVED	C/I	0	0

E—Empty

0 = This bit is cleared by the CP to indicate that the data bits associated with this BD are now available to the M68000 core.

1 = This bit is set by the M68000 core to indicate that the data bits associated with this BD have been read.

NOTE

Additional data received will be discarded until the empty bit is set by the M68000 core.

Bits 14–6—These bits are reserved and should be set to zero by the M68000 core.

C/I—Command/Indication Channel Data

Bits 1–0—The CP always writes these bits with zeros.

4.7.4.4 SMC2 Transmit Buffer Descriptor

In the IDL mode, this BD is identical to the SMC1 transmit BD. In the GCI mode, SMC2 is used to control the C/I channel.

15	14 … 6	5 … 2	1	0
R	RESERVED	C/I	0	0

R—Ready

0 = This bit is cleared by the CP after transmission to indicate that the BD is now available to the M68000 core.

1 = This bit is set by the M68000 core to indicate that the data associated with this BD is ready for transmission.

Bits 14–6—Reserved for future use; should be set to zero by the user.

C/I—Command/Indication Channel Data

Bits 1–0—These bits should be written with zeros by the M68000 core.

4.7.5 SMC Interrupt Requests

SMC1 and SMC2 send individual interrupt requests to the IMP interrupt controller when one of the respective SMC receive buffers is full or when one of the SMC transmit buffers is empty. Each of the two interrupt requests from each SMC is enabled when its respective SMC channel is enabled in the SPMODE register. Interrupt requests from SMC1 and SMC2 can be masked in the interrupt mask register. See 3.2 Interrupt Controller for more details.

SECTION 5
SIGNAL DESCRIPTION

This section defines the MC68302 pinout. The input and output signals of the MC68302 are organized into functional groups and are described in the following sections. The MC68302 is offered in a 132-pin (13 x 13) pin grid array (PGA), a 132-lead plastic quad flat package (PQFP), and a 144-lead thin quad flat package (TQFP).

The MC68302 uses a standard M68000 bus for communication between both on-chip and external peripherals. This bus is a single, continuous bus existing both on-chip and off-chip the MC68302. Any access made internal to the device is visible externally. Any access made external is visible internally. Thus, when the M68000 core accesses the dual-port RAM, the bus signals are driven externally. Likewise, when an external device accesses an area of external system memory, the chip-select logic can be used to generate the chip-select signal and $\overline{\text{DTACK}}$.

5.1 FUNCTIONAL GROUPS

The input and output signals of the MC68302 are organized into functional groups as shown in Table 5-1 and Figure 5-1.

Table 5-1. Signal Definitions

Functional Group	Signals	Number
Clocks	XTAL, EXTAL, CLKO	3
System Control	$\overline{\text{RESET}}$, $\overline{\text{HALT}}$, $\overline{\text{BERR}}$, BUSW, DISCPU	5
Address Bus	A23–A1	23
Data Bus	D15–D0	16
Bus Control	$\overline{\text{AS}}$, R/$\overline{\text{W}}$, $\overline{\text{UDS}}$/A0, $\overline{\text{LDS/DS}}$, $\overline{\text{DTACK}}$	5
Bus Control	$\overline{\text{RMC}}$, IAC, $\overline{\text{BCLR}}$	3
Bus Arbitration	$\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{BGACK}}$	3
Interrupt Control	$\overline{\text{IPL2}}$–$\overline{\text{IPL0}}$, FC2–FC0, $\overline{\text{AVEC}}$	7
NMSI1/ISDN I/F	RXD, TXD, RCLK, TCLK, $\overline{\text{CD}}$, $\overline{\text{CTS}}$, $\overline{\text{RTS}}$, BRG1	8
NMSI2/PAIO	RXD, TXD, RCLK, TCLK, $\overline{\text{CD}}$, $\overline{\text{CTS}}$, $\overline{\text{RTS}}$, SDS2	8
NMSI3/SCP/PAIO	RXD, TXD, RCLK, TCLK, $\overline{\text{CD}}$, $\overline{\text{CTS}}$, $\overline{\text{RTS}}$, PA12	8
IDMA/PAIO	DREQ, DACK, DONE	3
IACK/PBIO	IACK7, IACK6, IACK1	3
Timer/PBIO	TIN2, TIN1, $\overline{\text{TOUT2}}$, $\overline{\text{TOUT1}}$, $\overline{\text{WDOG}}$	5
PBIO	PB11–PB8	4

Table 5-1. Signal Definitions

Chip Select	CS3–CS0	4
Testing	$\overline{FRZ}$ (2 Spare)	3
V_{DD}		8
GND		13

All pins except EXTAL, CLKO, and the layer 1 interface pins in IDL mode support TTL levels. EXTAL, when used as an input clock, needs a CMOS level. CLKO supplies a CMOS level output. The IDL interface is specified as a CMOS electrical interface.

All outputs (except CLKO and the GCI pins) drive 130 pF. CLKO is designed to drive 50 pF. The GCI output pins drive 150 pF.

5.2 POWER PINS

The IMP has 21 power supply pins. Careful attention has been paid to reducing IMP noise, potential crosstalk, and RF radiation from the output drivers. Inputs may be +5 V when V_{DD} is 0 V without damaging the device.

- V_{DD} (8)—There are 8 power pins.
- GND (13)—There are 13 ground pins.

NOTE

The Input High Voltage and Input Low Voltage for EXTAL and the values for power are specified in the DC Electrical Characteristics.A valid clock signal oscillates between a low voltage of between V_{SS}-0.3 and .6 volts and a high voltage of between 4.0 and V_{DD} volts. This EXTAL signal must be present within 20 mS after V_{DD} reaches its minimum specified level of 4.5 volts.

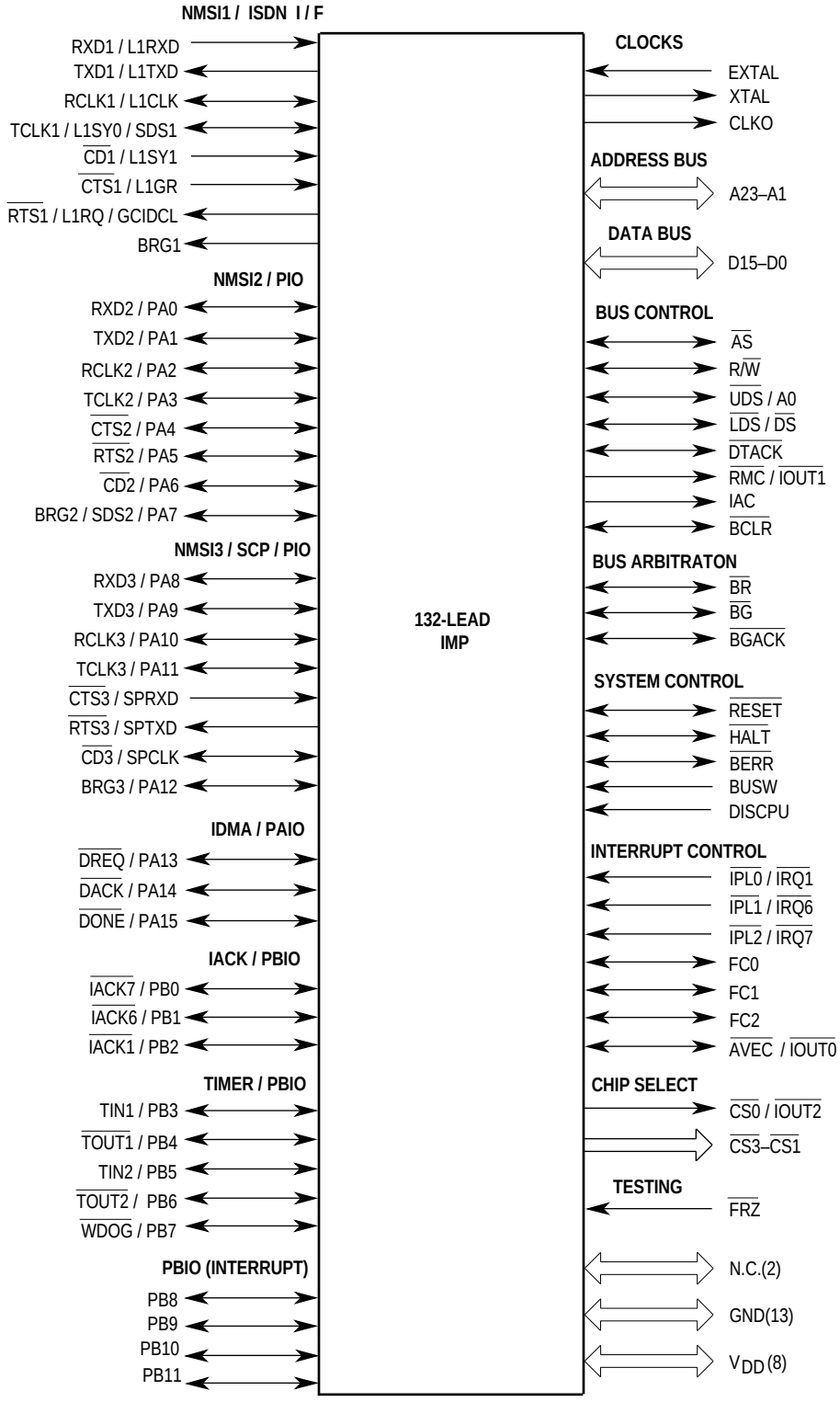


Figure 5-1. Functional Signal Groups

5.3 CLOCKS

The clock pins are shown in Figure 5-2.

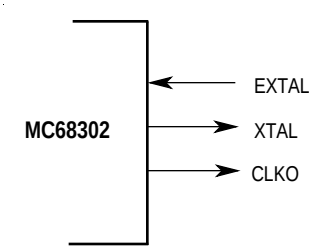


Figure 5-2. Clock Pins

EXTAL—External Clock/Crystal Input

This input provides two clock generation options (crystal and external clock). EXTAL may be used (with XTAL) to connect an external crystal to the on-chip oscillator and clock generator. If an external clock is used, the clock source should be connected to EXTAL, and XTAL should be left unconnected. The oscillator uses an internal frequency equal to the external crystal frequency. The frequency of EXTAL may range from 8 MHz to 25 MHz. When an external clock is used, it must provide a CMOS level at this input frequency.

NOTE

The Input High Voltage and Input Low Voltage for EXTAL and the values for Power are specified in the DC Electrical Characteristics.A valid clock signal oscillates between a low voltage of between V_{SS}-0.3 and .6 volts and a high voltage of between 4.0 and V_{DD} volts. This EXTAL signal must be present within 20 mS after V_{DD} reaches its minimum specified level of 4.5 volts.

The frequency range of the original MC68302 was 8 MHz to 16.67 MHz. Thus, in this manual, many references to the frequency “16.67 MHz” are made when the maximum operating frequency of the MC68302 is discussed. Similarly, the value “8 MHz” is often used when discussing the minimum operating frequency. When using faster versions of the MC68302, such as 20 or 25 MHz, all references to 16.67 MHz may be replaced with 20 or 25 MHz. When using versions with slower minimum operating frequencies, such as 4 MHz, all references to 8 MHz may be replaced with 4 MHz. Note, however, that resulting parameters such as baud rates and timer periods change accordingly.

XTAL—Crystal Output

This output connects the on-chip oscillator output to an external crystal. If an external clock is used, XTAL should be left unconnected. See 3.7 On-Chip Clock Generator for more details.

CLKO—Clock Out

This output clock signal is derived from the on-chip clock oscillator. This clock signal is internally connected to the clock input of the M68000 core, the communication processor,

and system integration block. All M68000 bus timings are referenced to the CLKO signal. CLKO supports both CMOS and TTL output levels. The output drive capability of the CLKO signal is programmable in the CKCR register (see 3.9 Clock Control Register) to one-third, two-thirds, or full strength, or this output can be disabled.

5.4 SYSTEM CONTROL

The system control pins are shown in Figure 5-3.

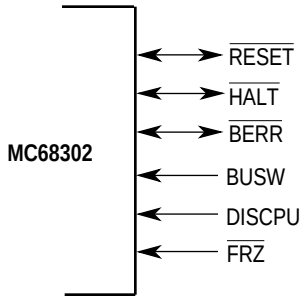


Figure 5-3. System Control Pins

RESET

This bidirectional, open-drain signal, acting as an input and asserted along with the HALT pin, starts an initialization sequence called a total system reset that resets the entire MC68302. RESET and HALT should remain asserted for at least 100 ms at power-on reset, and at least 10 clocks otherwise. The on-chip system RAM is not initialized during reset except for several locations initialized by the CP.

An internally generated reset, from the M68000 RESET instruction, causes the RESET line to become an output for 124 clocks. In this case, the M68000 core is not reset; however, the communication processor is fully reset, and the system integration block is almost fully reset (refer to Table 2-6 and Table 2-9 for a list of the unaffected registers). The user may also use the RESET output signal in this case to reset all external devices.

During total system reset, the address, data, and bus control pins are all three-stated, except for CS3–CS0, which are high, and IAC, which is low. The BG pin output is the same as that on the BR input. The general-purpose I/O pins are configured as inputs, except for WDOG, which is an open-drain output. The NMSI1 pins are all inputs, except for RTS1 and TXD1, which output a high value. RTS3, NC1, and NC3 are also high. CLKO is active and BRG1 is CLO/3.

NOTE

The RESET pin should not be asserted externally without also asserting the HALT pin. To reset just the internal MC68302 peripherals, the RESET instruction may be used. If the RESET instruction is to be used, then the pull-up resistor on RESET should not be greater than 1.2 k ohms.

Besides the total system reset and the RESET instruction, some of the MC68302 peripherals have reset bits in one of their registers that cause that particular peripheral to be reset to the same state as a total system reset or the RESET instruction. Reset bits may be found in the CP (in the CR), the IDMA (in the CMR), timer 1 (in the TMR1), and timer 2 (in the TMR2).

$\overline{\text{HALT}}$—Halt

When this bidirectional, open-drain signal is driven by an external device, it will cause the IMP bus master (M68000 core, SDMA, or IDMA) to stop at the completion of the current bus cycle. If the processor has stopped executing instructions due to a double-fault condition, this line is driven by the processor to indicate to external devices that the processor has stopped. An example of a double-fault condition is the occurrence of a bus error followed by a second bus error during the bus error exception stacking process. This signal is asserted with the $\overline{\text{RESET}}$ signal to cause a total MC68302 system reset. If $\overline{\text{BERR}}$ is asserted with the $\overline{\text{HALT}}$ signal, a retry cycle is performed.

$\overline{\text{BERR}}$—Bus Error

This bidirectional, open-drain signal informs the bus master (M68000 core, SDMA, IDMA, or external bus master) that there is a problem with the cycle currently being executed. This signal can be asserted by the on-chip hardware watchdog (bus timeout because of no $\overline{\text{DTACK}}$), by the chip-select logic (address conflict or write-protect violation), or by external circuitry. If $\overline{\text{BERR}}$ is asserted with the $\overline{\text{HALT}}$ signal, a retry cycle is performed.

BUSW—Bus Width Select

This input defines the M68000 processor mode (MC68000 or MC68008) and the data bus width (16 bits or 8 bits, respectively). BUSW may only be changed upon a total system reset. In 16-bit mode, all accesses to internal and external memory by the MC68000 core, the IDMA, SDMA, and external master may be 16 bits, according to the assertion of the UDS and LDS pins. In 8-bit mode, all M68000 core and IDMA accesses to internal and external memory are limited to 8 bits. Also in 8-bit mode, SDMA accesses to external memory are limited to 8 bits, but CP accesses to the CP side of the dual-port RAM continue to be 16 bits. In 8-bit mode, external accesses to internal memory are also limited to 8 bits at a time.

Low = 8-bit data bus, MC68008 core processor

High = 16-bit data bus, MC68000 core processor

DISCPU—Disable CPU (M68000 core)

The MC68302 can be configured to work solely with an external CPU. In this mode the on-chip M68000 core CPU should be disabled by asserting the DISCPU pin high during a total system reset ($\overline{\text{RESET}}$ and $\overline{\text{HALT}}$ asserted). DISCPU may only be changed upon a total system reset.

The DISCPU pin, for instance, allows use of several IMPs to provide more than three SCC channels without the need for bus isolation techniques. Only one of the IMP M68000 cores is active and services the other IMPs as peripherals (with their respective cores disabled). Refer to 3.8.4 Disable CPU Logic (M68000) for more details.

$\overline{FRZ}$—Freeze Activity

The $\overline{FRZ}$ pin is used to freeze the activity of selected peripherals. This is useful for system debugging purposes. Refer to 3.8 System Control for more details on which peripherals are affected. $\overline{FRZ}$ should be continuously negated during total system reset.

5.5 ADDRESS BUS PINS (A23–A1)

The address bus pins are shown in Figure 5-4.

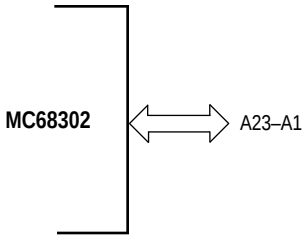


Figure 5-4. Address Bus Pins

A23—A1 form a 24-bit address bus when combined with $\overline{UDS}$/A0. The address bus is a bidirectional, three-state bus capable of addressing 16M bytes of data (including the IMP internal address space). It provides the address for bus operation during all cycles except CPU space cycles. In CPU space cycles, the CPU reads a peripheral device vector number.

These lines are outputs when the IMP (M68000 core, SDMA or IDMA) is the bus master and are inputs otherwise.

5.6 DATA BUS PINS (D15—D0)

The data bus pins are shown in Figure 5-5.

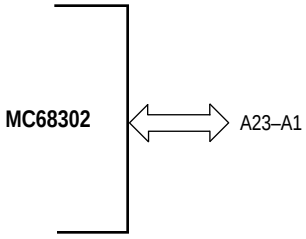


Figure 5-5. Data Bus Pins

This 16-bit, bidirectional, three-state bus is the general-purpose data path. It can transmit and accept data in either word or byte lengths. For all 16-bit IMP accesses, byte 0, the high-order byte of a word, is available on D15–D8, conforming to the standard M68000 format.

When working with an 8-bit bus (BUSW is low), the data is transferred through the low-order byte (D7–D0). The high-order byte (D15–D8) is not used for data transfer, but D8-D15 are outputs during write cycles and are not three-stated.

5.7 BUS CONTROL PINS

The bus control pins are shown in Figure 5-6.

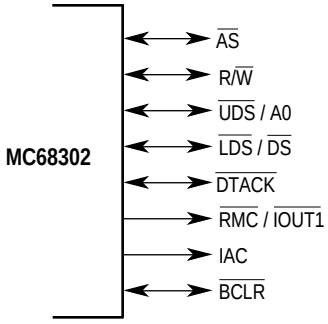


Figure 5-6. Bus Control Pins

AS—Address Strobe

This bidirectional signal indicates that there is a valid address on the address bus. This line is an output when the IMP (M68000 core, SDMA or IDMA) is the bus master and is an input otherwise.

R/W—Read/Write

This bidirectional signal defines the data bus transfer as a read or write cycle. It is an output when the IMP is the bus master and is an input otherwise.

UDS/A0—Upper Data Strobe/Address 0

This bidirectional line controls the flow of data on the data bus. When using a 16-bit data bus, this pin functions as upper data strobe (UDS). When using an 8-bit data bus, this pin functions as A0. When used as A0 (i.e., the BUSW pin is low), then the pin takes on the timing of the other address pins, as opposed to the strobe timing. This line is an output when the IMP is the bus master and is an input otherwise.

LDS/DS—Lower Data Strobe/Data Strobe

This bidirectional line controls the flow of data on the data bus. When using a 16-bit data bus, this pin functions as lower data strobe (LDS). When using an 8-bit data bus, this pin functions as DS. This line is an output when the IMP (M68000 core, SDMA or IDMA) is the bus master and is an input otherwise.

DTACK—Data Transfer Acknowledge

This bidirectional signal indicates that the data transfer has been completed. DTACK can be generated internally in the chip-select logic either for an IMP bus master or for an external bus master access to an external address within the chip-select ranges. It will also be generated internally during any access to the on-chip dual-port RAM or internal regis-

ters. If $\overline{\text{DTACK}}$ is generated internally, then it is an output. It is an input when the IMP accesses an external device not within the range of the chip-select logic or when programmed to be generated externally.

$\overline{\text{RMC}}$/$\overline{\text{IOUT1}}$—Read-Modify-Write Cycle Indication/Interrupt Output 1

This signal functions as $\overline{\text{RMC}}$ in normal operation. $\overline{\text{RMC}}$ is an output signal that is asserted when a read-modify-write cycle is executed. It indicates that the cycle is indivisible.

When the M68000 core is disabled, this pin operates as $\overline{\text{IOUT1}}$. $\overline{\text{IOUT2}}$–$\overline{\text{IOUT0}}$ provide the interrupt request output signals from the IMP interrupt controller to an external CPU when the M68000 core is disabled.

IAC—Internal Access

This output indicates that the current bus cycle accesses an on-chip location. This includes the on-chip 4K byte block of internal RAM and registers (both real and reserved locations), and the system configuration registers ($0F0–$0FF). The above-mentioned bus cycle may originate from the M68000 core, the IDMA, or an external bus master. Note that, if the SDMA accesses the internal dual-port RAM, it does so without arbitration on the M68000 bus; therefore, the IAC pin is not asserted in this case. The timing of IAC is identical to that of the $\overline{\text{CS3}}$–$\overline{\text{CS0}}$ pins.

IAC can be used to disable an external address/data buffer when the on-chip dual-port RAM and registers are accessed, thus preventing bus contention. Such a buffer is optional and is only required in larger systems. An external address/data buffer with its output enable (E) and direction control (dir) may be placed between the two bus segments as shown in Figure 5-7. The IAC signal saves the propagation delay and logic required to OR all the various system chip-select lines together to determine when to enable the external buffers.

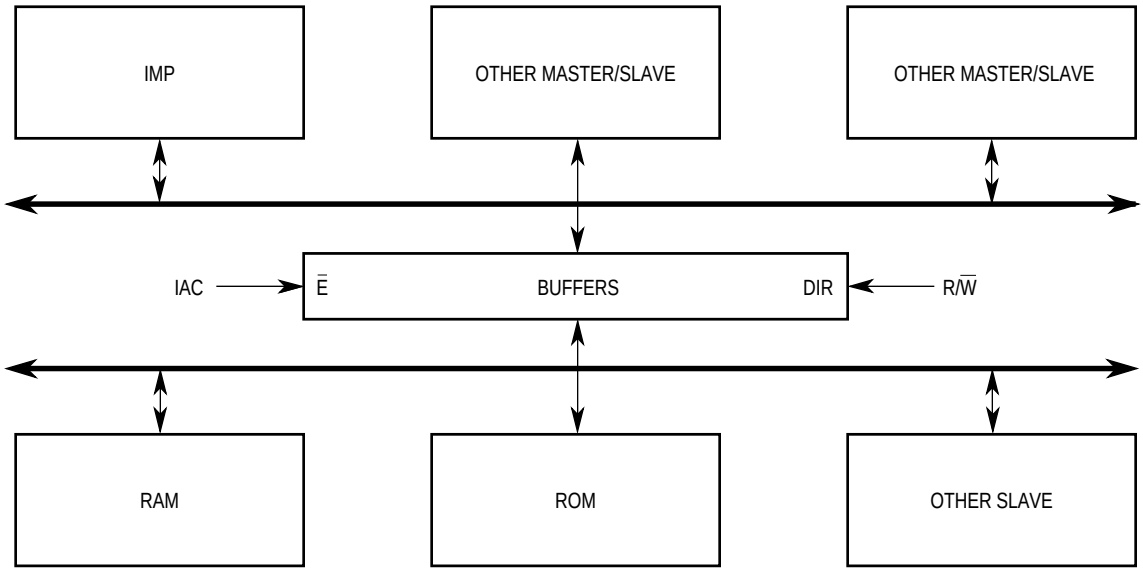


Figure 5-7. External Address/Data Buffer

$\overline{\text{BCLR}}$—Bus Clear

This open-drain output indicates that the M68000 core or the serial DMA (SDMA) requests the external bus master to release the bus. The core may be configured to assert this signal when it has a pending interrupt to execute. The SDMA asserts this signal when one of the SCCs is requesting DMA service.

When the M68000 core is disabled, this signal is an input to the independent DMA (IDMA) and is interpreted as a bus release request. It remains an output from the SDMA in this mode.

5.8 BUS ARBITRATION PINS

The bus arbitration pins are shown in Figure 5-8.

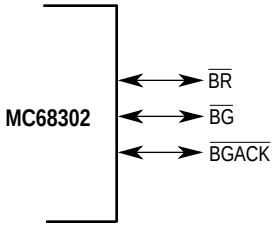


Figure 5-8. Bus Arbitration Pins

$\overline{\text{BR}}$—Bus Request

This input signal indicates to the on-chip bus arbiter that an external device desires to become the bus master. See 3.8.5.2 External Bus Arbitration for details. This signal is an open-drain output request signal from the IDMA and SDMA when the internal M68000 core is disabled.

$\overline{\text{BG}}$—Bus Grant

This output signal indicates to all external bus master devices that the processor will release bus control at the end of the current bus cycle to an external bus master. This signal is an input to the IDMA and SDMA when the internal M68000 core is disabled. During total system reset, $\overline{\text{BG}} = \overline{\text{BR}}$.

$\overline{\text{BGACK}}$—Bus Grant Acknowledge

This bidirectional signal indicates that some other device besides the M68000 core has become the bus master. This signal is an input when an external device or the M68000 core owns the bus. This signal is an output when the IDMA or SDMA has become the master of the bus. If the SDMA steals a cycle from the IDMA, the $\overline{\text{BGACK}}$ pin will remain asserted continuously.

NOTE

$\overline{\text{BGACK}}$ should always be used in the external bus arbitration process. See 3.8.5.2 External Bus Arbitration for details.

5.9 INTERRUPT CONTROL PINS

The interrupt control pins are shown in Figure 5-9.

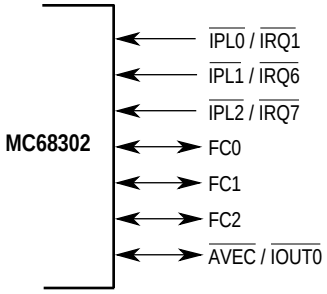


Figure 5-9. Interrupt Control Pins

These inputs have dual functionality:

- IPL0/IRQ1
- IPL1/IRQ6
- IPL2/IRQ7—Interrupt Priority Level 2–0/Interrupt Request 1,6,7

As IPL2–IPL0 (normal mode), these input pins indicate the encoded priority level of the external device requesting an interrupt. Level 7 is the highest (nonmaskable) priority; whereas, level 0 indicates that no interrupt is requested. The least significant bit is IPL0, and the most significant bit is IPL2. These lines must remain stable until the M68000 core signals an interrupt acknowledge through FC2–FC0 and A19–A16 to ensure that the interrupt is properly recognized.

As IRQ1, IRQ6, and IRQ7 (dedicated mode), these inputs indicate to the MC68302 that an external device is requesting an interrupt. Level 7 is the highest level and cannot be masked. Level 1 is the lowest level. Each one of these inputs (except for level 7) can be programmed to be either level-sensitive or edge-sensitive. The M68000 always treats a level 7 interrupt as edge sensitive.

FC2–FC0—Function Codes 2–0

These bidirectional signals indicate the state and the cycle type currently being executed. The information indicated by the function code outputs is valid whenever AS is active.

These lines are outputs when the IMP (M68000 core, SDMA, or IDMA) is the bus master and are inputs otherwise. The function codes output by the M68000 core are predefined; whereas, those output by the SDMA and IDMA are programmable. The function code lines are inputs to the chip-select logic and IMP internal register decoding in the BAR.

AVEC/IOUT0—Autovector Input/Interrupt Output 0

In normal operation, this signal functions as the input AVEC. AVEC, when asserted during an interrupt acknowledge cycle, indicates that the M68000 core should use automatic vectoring for an interrupt. This pin operates like VPA on the MC68000, but is used for au-

tomatic vectoring only. AVEC instead of DTACK should be asserted during autovectoring and should be high otherwise.

When the M68000 core is disabled, this pin operates as IOUT0. IOUT2–IOUT0 provide the interrupt request output signals from the IMP interrupt controller to an external CPU when the M68000 core is disabled.

5.10 MC68302 BUS INTERFACE SIGNAL SUMMARY

Table 5-2 and Table 5-3 summarize all bus signals discussed in the previous paragraphs. They show the direction of each pin for the following bus masters: M68000 core, IDMA, SDMA (includes DRAM refresh), and external. Each bus master can access either internal dual-port RAM and registers or an external device or memory. When an external bus master accesses the internal dual-port RAM or registers, the access may be synchronous or asynchronous.

When the M68000 core is disabled, BR and BG change their direction, and BCLR becomes bidirectional.

Table 5-2. Bus Signal Summary—Core and External Master

		M68000 Core Master Access To		External Master Access To	
Signal Name	**Pin Type**	**Internal Memory Space**	**External Memory Space**	**Internal Memory Space**	**External Memory Space**
A23–A1, FC2–FC0, AS, UDS, LDS, R/W, RMC	I/O	O	O	I	I
BCLR	I/O Open Drain	O	O	O	O
IAC	O	O	O	O	O
D15–D0 Read	I/O	O	I	O	I
D15–D0 Write	I/O	O	O	I	I
DTACK	I/O	O	**	O	**
BR	I/O Open Drain	I	I	I	I
BG	I/O	O	O	O	O
BGACK	I/O	I	I	I	I
HALT	I/O Open Drain	I/O	I/O	I	I
RESET	I/O Open Drain	I/O	I/O	I	I
BERR	I/O Open Drain	I/O***	I/O***	I/O***	I/O***
IPL2–IPL0	I	I	I	I	I
AVEC	I	I	I	I	I
IOUT2–IOUT0	O	O	O	O	O

**If DTACK is generated automatically (internally) by the chip-select logic, then it is an output. Otherwise, it is an input.
***BERR is an open-drain output, and may be asserted by the IMP when the hardware watchdog is used or when the chip-select logic detects address conflict or write protect violation. BERR may be asserted by external logic in all cases.

Table 5-3. Bus Signal Summary—IDMA and SDMA

		IDMA Master Access To		SDMA Master Access To	
Signal Name	**Pin Type**	**Internal Memory Space**	**External Memory Space**	**Internal Memory Space**	**External Memory Space**
A23–A1, FC–FC0, $\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$, R/$\overline{W}$, $\overline{RMC}$	I/O	O	O	N/A	O
$\overline{BCLR}$	I/O Open Drain	I #	I #	N/A	O
IAC	O	O	O	N/A	O
D15—D0 Read	I/O	O	I	N/A	I
D15—D0 Write	I/O	O	O	N/A	O
$\overline{DTACK}$	I/O	O	**	N/A	**
$\overline{BR}$	I/O	O ##	O ##	N/A	O ##
$\overline{BG}$	I/O	I ##	I ##	N/A	I ##
$\overline{BGACK}$	I/O	O	O	N/A	O
$\overline{HALT}$	I/O Open Drain	I	I	N/A	I
$\overline{RESET}$	I/O Open Drain	I	I	N/A	I
$\overline{BERR}$	I/O Open Drain	I/O***	I/O***	N/A	I/O***

**If $\overline{DTACK}$ is generated automatically (internally) by the chip-select logic, then it is an output. Otherwise, it is an input.

***$\overline{BERR}$ is an open-drain output, and may be asserted by the IMP when the hardware watchdog is used or when the chip-select logic detects address conflict or write protect violation. $\overline{BERR}$ may be asserted by external logic in all cases.

Applies to disable CPU mode only. The internal signal IBCLR is used otherwise.

Applies to disable CPU mode only, otherwise N/A.

5.11 PHYSICAL LAYER SERIAL INTERFACE PINS

The physical layer serial interface has 24 pins, and all but one of them have multiple functionality. The pins can be used in a variety of configurations in ISDN or non-ISDN environments. Table 5-3 shows the functionality of each group of pins and their internal connection to the three SCC and one SCP controllers. The physical layer serial interface can be configured for non-multiplexed operation (NMSI) or multiplexed operation that includes IDL, GCI, and PCM highway modes. IDL and GCI are ISDN interfaces. When working in one of the multiplexed modes, the NMSI1/ISDN physical interface can be connected to all three SCC controllers.

Table 5-4. Serial Interface Pin Functions

First Function	Connected To	Second Function	Connected To
NMSI1 (8)	SCC1 Controller	ISDN Interface	SCC1/SCC2/SCC3
NMSI2 (8)	SCC2 Controller	PIO—Port A	Parallel I/O
NMSI3 (5)	SCC3 Controller	PIO—Port A	Parallel I/O
NMSI3 (3)	SCC3 Controller	SCP	SCP Controller

NOTE: Each one of the parallel I/O pins can be configured individually.

5.12 TYPICAL SERIAL INTERFACE PIN CONFIGURATIONS

Table 5-4 shows typical configurations of the physical layer interface pins for an ISDN environment. Table 5-6 shows potential configurations of the physical layer interface pins for a non-ISDN environment. The IDMA, IACK, and timer pins can be used in all applications either as dedicated functions or as PIO pins.

Table 5-5. Typical ISDN Configurations

Pins	Connected To	Used As
NMSI1 or ISDN I/F	SCC1 and SCC3	SCC1 Used as ISDN D-ch SCC3 Used as ISDN B2-ch
NMSI2	SCC2	SCC2 is Connected to Terminal
NMSI3	PA12–PA8 SCP	PIO (Extra Modem Signals and SCP Select Signals) Status/Control Exchange

NOTES:
1. ISDN environment with SCP port for status/control exchange and with existing terminal (for rate adaption).
2. D-ch is used for signaling.
3. B1-ch is used for voice (external CODEC required).
4. B2-ch is used for data transfer.

Table 5-6. Typical Generic Configurations

Pins	Connected To	Used As
NMSI1 or ISDN I/F	SCC1	Terminal with Modem
NMSI2	SCC2	Terminal with Modem
NMSI3 (5)	SCC3	Terminal without Modem
NMSI3 (3)	SCP	Status/Control Exchange

NOTE: Generic environment with three SCC ports (any protocol) and the SCP port. SCC3 does not use modem control signals.

5.13 NMSI1 OR ISDN INTERFACE PINS

The NMSI1 or ISDN interface pins are shown in Figure 5-10.

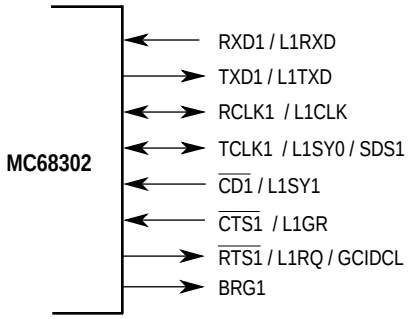


Figure 5-10. NMSI1 or ISDN Interface Pins

These eight pins can be used either as NMSI1 in nonmultiplexed serial interface (NMSI) mode or as an ISDN physical layer interface in IDL, GCI, and PCM highway modes. The input buffers have Schmitt triggers.

Table 5-7 shows the functionality of each pin in NMSI, GCI, IDL, and PCM highway modes.

Table 5-7. Mode Pin Functions

Signal Name	NMSI1		GCI		IDL		PCM	
RXD1/L1RXD	I	RXD1	I	L1RXD	I	L1RXD	I	L1RXD
TXD1/L1TXD	O	TXD1	O	L1TXD	O	L1TXD	O	L1TXD
RCLK1/L1CLK	I/O	RCLK1	I	L1CLK	I	L1CLK	I	L1CLK
TCLK1/L1SY0	I/O	TCLK1	O	SDS1	O	SDS1	I	L1SY0
$\overline{\text{CD1}}$/L1SY1	I	$\overline{\text{CD1}}$	I	L1SYNC	I	L1SYNC	I	L1SY1
$\overline{\text{CTS1}}$/L1GR	I	$\overline{\text{CTS1}}$	I	L1GR	I	L1GR		
$\overline{\text{RTS1}}$/L1RQ	O	$\overline{\text{RTS1}}$	O	GCIDCL	O	L1RQ	O	$\overline{\text{RTS}}$
BRG1	O	BRG1	O	BRG1	O	BRG1	O	BRG1

NOTES:
1. In IDL and GCI mode, SDS2 is output on the PA7 pin.
2. CD1 may be used as an external sync in NMSI mode.
3. $\overline{\text{RTS}}$ is the $\overline{\text{RTS1}}$, $\overline{\text{RTS2}}$, or RTS3 pin according to which SCCs are connected to the PCM highway.

RXD1/L1RXD—Receive Data/Layer-1 Receive Data

This input is used as the NMSI1 receive data in NMSI mode and as the receive data input in IDL, GCI, and PCM modes.

TXD1/L1TXD—Transmit Data/Layer-1 Transmit Data

This output is used as NMSI1 transmit data in NMSI mode and as the transmit data output in IDL, GCI, and PCM modes. TXD1 may be configured as an open-drain output in NMSI mode. L1TXD in IDL and PCM mode is a three-state output. In GCI mode, it is an open-drain output.

RCLK1/L1CLK—Receive Clock/Layer-1 Clock

This pin is used as an NMSI1 bidirectional receive clock in NMSI mode or as an input clock in IDL, GCI, and PCM modes. In NMSI mode, this signal is an input when SCC1 is working with an external clock and is an output when SCC1 is working with its baud rate generator. The RCLK1 output can be three-stated by setting bit 12 in the CKCR register (see 3.9 Clock Control Register).

TCLK1/L1SY0/SDS1—Transmit Clock/PCM Sync/Serial Data Strobe 1

This pin is used as an NMSI1 bidirectional transmit clock in NMSI mode, as a sync signal in PCM mode, or as the SDS1 output in IDL/GCI modes. In NMSI mode, this signal is an input when SCC1 is working with an external clock and is an output when SCC1 is working with its baud rate generator. The TCLK1 output can be three-stated by setting bit 13 in the CKCR register (see 3.9 Clock Control Register).

NOTE

When using SCC1 in the NMSI mode with the internal baud rate generator operating, the TCLK1 and RCLK1 pins will always output the baud rate generator clock unless disabled in the CKCR register. Thus, if a dynamic selection between an internal and external clock source is required in an application, the clock pins should be disabled first in the CKCR register before switching the TCLK1 and RCLK1 lines. On SCC2 and SCC3, contention may be avoided by disabling the clock line outputs in the PACNT register.

In PCM mode, L1SY1–L1SY0 are encoded signals used to create channels that can be independently routed to the SCCs.

Table 5-8. PCM Mode Signals

L1SY1	L1SY0	Data (L1RXD, L1TXD) is Routed to SCC
0	0	L1TXD is Three-Stated, L1RXD is Ignored
0	1	CH-1
1	0	CH-2
1	1	CH-3

NOTE: CH-1, 2, and 3 are connected to the SCCs as determined in the SIMODE register.

In IDL/GCI modes, the SDS2–SDS1 outputs may be used to route the B1 and/or B2 channels to devices that do not support the IDL or GCI buses. This is configured in the serial interface mode (SIMODE) and serial interface mask (SIMASK) registers.

$\overline{\text{CD1}}$/L1SY1—Carrier Detect/Layer-1 Sync

This input is used as the NMSI1 carrier detect ($\overline{\text{CD}}$) pin in NMSI mode, as a PCM sync signal in PCM mode, and as an L1SYNC signal in IDL/GCI modes.

If the $\overline{\text{CD1}}$ pin has changed for more than one receive clock cycle, the IMP asserts the appropriate bit in the SCC1 event register. If the SCC1 channel is programmed not to support $\overline{\text{CD1}}$ automatically (in the SCC1 mode register), then this pin may be used as an external interrupt source. The current value of $\overline{\text{CD1}}$ may be read in the SCCS1 register. See 4.5.8.3 SCC Status Register (SCCs) for details. $\overline{\text{CD1}}$ may also be used as an external sync in NMSI mode.

$\overline{\text{CTS1}}$/L1GR—Clear to Send/Layer-1 Grant

This input is the NMSI1 $\overline{\text{CTS}}$ signal in the NMSI mode or the grant signal in the IDL/GCI mode. If this pin is not used as a grant signal in GCI mode, it should be connected to V_{DD}.

If the $\overline{\text{CTS1}}$ pin has changed for more than one transmit clock cycle, the IMP asserts the appropriate bit in the SCC1 event register and optionally aborts the transmission of that frame.

If SCC1 is programmed not to support $\overline{\text{CTS1}}$ (in the SCC1 mode register), then this pin may be used as an external interrupt source. The current value of the $\overline{\text{CTS1}}$ pin may be read in the SCCS1 register. See 4.5.8.3 SCC Status Register (SCCs) for details.

$\overline{\text{RTS1}}$/L1RQ/GCIDCL—Request to Send/Layer-1 Request/GCI Clock Out

This output is the NMSI1 $\overline{\text{RTS}}$ signal in NMSI mode, the IDL request signal in IDL mode, or the GCI data clock output in GCI mode.

$\overline{\text{RTS1}}$ is asserted when SCC1 (in NMSI mode) has data or pad (flags or syncs) to transmit.

In GCI mode this pin is used to output the GCI data clock.

BRG1—Baud Rate Generator 1

This output is always the baud rate generator clock of SCC1. (This pin used to be NC2.) The BRG clock output on the BRG pins is 180 degrees out of phase with the internal BRG clock output on the RCLK and TCLK pins. This statement applies to all BRG pins: BRG1, BRG2, and BRG3. The BRG1 output can be disabled by setting bit 11 in the CKCR register (see 3.9 Clock Control Register). When BRG1 is disabled the pin is driven high.

5.14 NMSI2 PORT OR PORT A PINS

The NMSI2 port or port A pins are shown in Figure 5-11.

These eight pins can be used either as the NMSI2 port or as a general-purpose parallel I/O port. Each one of these pins can be configured individually to be general-purpose I/O pins or a dedicated function in NMSI2. When they are used as NMSI2 pins, they function exactly as the NMSI1 pins in NMSI mode.

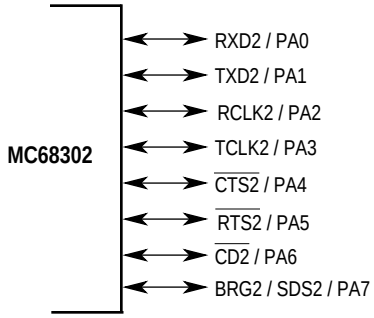


Figure 5-11. NMSI2 Port or Port A Pins

The PA7 signal in dedicated mode becomes serial data strobe 2 (SDS2) in IDL and GCI modes. In IDL/GCI modes, the SDS2–SDS1 outputs may be used to route the B1 and/or B2 channels to devices that do not support the IDL or GCI buses. This is configured in the SIMODE and SIMASK registers. If SCC2 is in NMSI mode, this pin operates as BRG2, the output of the SCC2 baud rate generator, unless SDS2 is enabled to be asserted during the B1 or B2 channels of ISDN (bits SDC2–SDC1 of SIMODE). SDS2/BRG2 may be temporarily disabled by configuring it as a general-purpose output pin. The input buffers have Schmitt

triggers. TCLK2 acts as the SCC2 baud rate generator output if SCC2 is in one of the multiplexed modes.

- RXD2/PA0
- TXD2/PA1
- RCLK2/PA2
- TCLK2/PA3
- $\overline{\text{CTS2}}$/PA4
- $\overline{\text{RTS2}}$/PA5
- $\overline{\text{CD2}}$/PA6
- SDS2/PA7/BRG2

Table 5-9. Baud Rate Generator Outputs

Source	NMSI	GCI	IDL	PCM
SCC1	BRG1	BRG1	BRG1	BRG1
SCC2	BRG2	TCLK2	TCLK2	TCLK2
SCC3	BRG3	TCLK3	TCLK3	TCLK3

NOTE: In NMSI mode, the baud rate generator outputs can also appear on the RCLK and TCLK pins as programmed in the SCON register.

5.15 NMSI3 PORT OR PORT A PINS OR SCP PINS

The NMSI3 port or port A pins or SCP pins are shown in Figure 5-12.

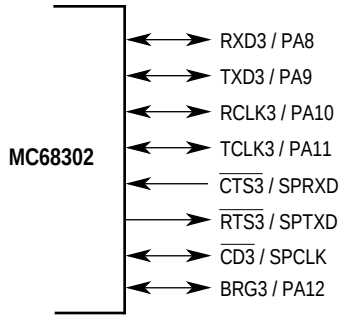


Figure 5-12. NMSI3 Port or Port A Pins or SCP Pins

These eight pins can be used either as the NMSI3 port or as the NMSI3 port (less three modem lines) and the SCP port. If the SCP is enabled (EN bit in SPMODE register is set), then the three lines are connected to the SCP port. Otherwise, they are connected to the SCC3 port.

Each of the port A I/O pins can be configured individually to be general-purpose I/O pins or a dedicated function in NMSI3. When they are used as the NMSI3 pins, they function exactly

as the NMSI1 pins (see the previous description). The input buffers have Schmitt triggers. TCLK3 acts as the SCC3 baud rate generator output if SCC3 is in one of the multiplexed modes.

- RXD3/PA8
- TXD3/PA9
- RCLK3/PA10
- TCLK3/PA11

SPRXD/$\overline{\text{CTS3}}$—SCP Receive Serial Data/NMSI3 Clear-to-Send Pin

This signal functions as the SCP receive data input or may be used as the NMSI3 $\overline{\text{CTS}}$ input pin.

SPTXD/$\overline{\text{RTS3}}$—SCP Transmit Serial Data/NMSI3 Request-to-Send Pin

This output is the SCP transmit data output or may be used as the NMSI3 $\overline{\text{RTS}}$ pin.

SPCLK/$\overline{\text{CD3}}$—SCP Clock/NMSI3 CD Pin

This bidirectional signal is used as the SCP clock output or the NMSI3 $\overline{\text{CD3}}$ input pin.

PA12/BRG3

This pin functions as bit 12 of port A or may be used as the SCC3 baud rate generator output clock when SCC3 is operating in NMSI mode.

5.16 IDMA OR PORT A PINS

The IDMA or port A pins are shown in Figure 5-13.

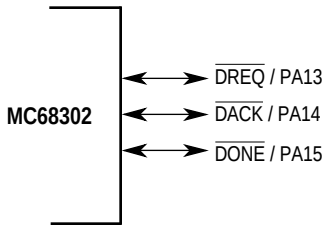


Figure 5-13. IDMA or Port A Pins

Each of these three pins can be used either as dedicated pins for the IDMA signals or as general-purpose parallel I/O port A pins. Note that even if one or more of the IDMA pins are used as general-purpose I/O pins, the IDMA can still be used. For example, if $\overline{\text{DONE}}$ is not needed by the IDMA, it can be configured as a general-purpose I/O pin. If the IDMA is used for memory-to-memory transfers only, then all three pins can be used as general-purpose I/O pins. The input buffer of $\overline{\text{DACK}}$ has a Schmitt trigger.

$\overline{\text{DREQ}}$/PA13—DMA Request

This input is asserted by a peripheral device to request an operand transfer between that peripheral device and memory. In the cycle steal request generation mode, this input is edge-sensitive. In burst mode, it is level-sensitive.

$\overline{\text{DACK}}$/PA14—DMA Acknowledge

This output, asserted by the IDMA, signals to the peripheral that an operand is being transferred in response to a previous transfer request.

$\overline{\text{DONE}}$/PA15—DONE

This bidirectional, open-drain signal is asserted by the IDMA or by a peripheral device during any IDMA bus cycle to indicate that the data being transferred is the last item in a block. The IDMA asserts this signal as an output during a bus cycle when the byte count register is decremented to zero. Otherwise, this pin is an input to the IDMA to terminate IDMA operation.

5.17 IACK OR PIO PORT B PINS

The IACK or PIO port B pins are shown in Figure 5-14.

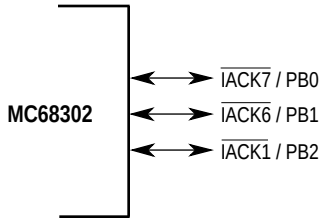


Figure 5-14. IACK or PIO Port B Pins

Each one of these three pins can be used either as an interrupt acknowledge signal or as a general-purpose parallel I/O port. Note that the IMP interrupt controller does not require the use of the IACK pins when it supplies the interrupt vector for the external source. The input buffers have Schmitt triggers.

$\overline{\text{IACK7}}$/PB0

$\overline{\text{IACK6}}$/PB1

$\overline{\text{IACK1}}$/PB2—Interrupt Acknowledge/Port B I/O

As $\overline{\text{IACK1}}$, $\overline{\text{IACK6}}$, and $\overline{\text{IACK7}}$, these active low output signals indicate to the external device that the MC68302 is executing an interrupt acknowledge cycle. The external device must then place its vector number on the lower byte of the data bus or use AVEC for autovectoring (unless internal vector generation is used).

5.18 TIMER PINS

The timer pins are shown in Figure 5-15.

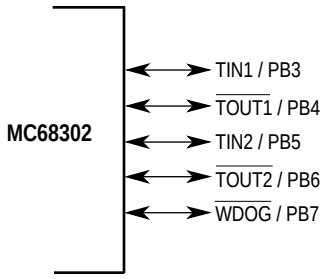


Figure 5-15. Timer Pins

Each of these five pins can be used either as a dedicated timer function or as a general-purpose port B I/O port pin. Note that the timers do not require the use of external pins. The input buffers have Schmitt triggers.

TIN1/PB3—Timer 1 Input

This input is used as a timer clock source for timer 1 or as a trigger for the timer 1 capture register. TIN1 may also be used as the external clock source for any or all three SCC baud rate generators.

$\overline{\text{TOUT1}}$/PB4—Timer 1 Output

This output is used as an active-low pulse timeout or an event overflow output (toggle) from timer 1.

TIN2/PB5—Timer 2 Input

This input can be used as a timer clock source for timer 2 or as a trigger for the timer 2 capture register.

$\overline{\text{TOUT2}}$/PB6—Timer 2 Output

This output is used as an active-low pulse timeout or as an event overflow output (toggle) from timer 2.

$\overline{\text{WDOG}}$/PB7—Watchdog Output

This active-low, open-drain output indicates expiration of the watchdog timer. $\overline{\text{WDOG}}$ is asserted for a period of 16 clock (CLKO) cycles and may be externally connected to the $\overline{\text{RESET}}$ and $\overline{\text{HALT}}$ pins to reset the MC68302. $\overline{\text{WDOG}}$ is never asserted by the on-chip hardware watchdog (see the $\overline{\text{BERR}}$ signal description). The $\overline{\text{WDOG}}$ pin function is enabled after a total system reset. It may be reassigned as the PB7 I/O pin in the PBCNT register.

5.19 PARALLEL I/O PINS WITH INTERRUPT CAPABILITY

The four parallel I/O pins with interrupt are shown in Figure 5-16.

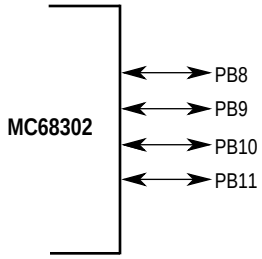


Figure 5-16. Port B Parallel I/O Pins with Interrupt

PB11–PB8—Port B Parallel I/O pins

These four pins may be configured as a general-purpose parallel I/O ports with interrupt capability. Each of the pins can be configured either as an input or an output. When configured as an input, each pin can generate a separate, maskable interrupt on a high-to-low transition. PB8 may also be used to request a refresh cycle from the DRAM refresh controller rather than as an I/O pin. The input buffers have Schmitt triggers.

5.20 CHIP-SELECT PINS

The chip-select pins are shown in Figure 5-17.

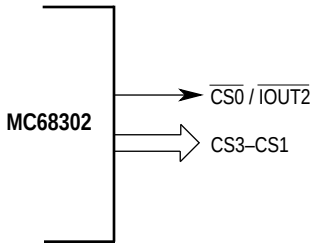


Figure 5-17. Chip-Select Pins

$\overline{CS0}$/$\overline{IOUT2}$—Chip-Select 0/Interrupt Output 2

In normal operation, this pin functions as CS0. CS0 is one of the four active-low output pins that function as chip selects for external devices or memory. It does not activate on accesses to the internal RAM or registers (including the BAR, SCR, or CKCR registers).

When the M68000 core is disabled, this pin operates as $\overline{IOUT2}$. $\overline{IOUT2}$—$\overline{IOUT0}$ provide the interrupt request output signals from the IMP interrupt controller to an external CPU when the M68000 core is disabled.

$\overline{CS3}$–$\overline{CS1}$—Chip Selects 3–1

These three active-low output pins function as chip selects for external devices or memory. $\overline{CS3}$—$\overline{CS0}$ do not activate on accesses to the internal RAM or registers (including the BAR SCR, or CKCR registers).

5.21 NO-CONNECT PINS

NC1 and NC3 output high values and are reserved for future use.

5.22 WHEN TO USE PULLUP RESISTORS

Pins that are output-only do not require external pullups. The bidirectional bus control signals require pullups since they are three-stated by the MC68302 when they are not being driven. Open-drain signals always require pullups.

Unused inputs should not be left floating. If they are input-only, they may be tied directly to V_{CC} or ground, or a pullup or pulldown resistor may be used. Unused outputs may be left unconnected. Unused I/O pins may be configured as outputs after reset and left unconnected.

If the MC68302 is to be held in reset for extended periods of time in an application (other than what occurs in normal power-on reset or board test sequences) due to a special application requirement (such as V_{DD} dropping below required specifications, etc.), then three-stated signals and inputs should be pulled up or down. This decreases stress on the device transistors and saves power.

See the $\overline{RESET}$ pin description for the condition of all pins during reset.

SECTION 6
ELECTRICAL CHARACTERISTICS

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock (CLKO pin) and possibly to one or more other signals.

6.1 MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	- 0.3 to + 7.0	V
Input Voltage	V_{in}	- 0.3 to + 7.0	V
Operating Temperature Range MC68302 MC68302C	T_A	 0 to 70 - 40 to 85	°C
Storage Temperature Range	T_{stg}	- 55 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to his high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{DD})

6.2 THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance for PGA	θ_{JA}	25	°C/W
	θ_{JC}	2	°C/W
Thermal Resistance for CQFP	θ_{JA}	40	°C/W
	θ_{JC}	15	°C/W
Thermal Resistance for PQFP	θ_{JA}	42	°C/W
	θ_{JC}	20	°C/W

$T_J = T_A + (P_D \cdot {}_A)$
$P_D = (V_{DD} \cdot I_{DD}) + P_{I/O}$

where:
$P_{I/O}$ is the power dissipation on pins.
For T_A = 70°C and $P_{I/O}$ + 0 W, 16.67 MHz, 5.5 V, and CQFP package, the worst case value of T_J is:
T_J = 70°C + (5.5 V · 30 mA · 40°C/W) = 98.65C

6.3 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction to Ambient, °C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = $I_{DD} \times V_{DD}$, Watts—Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins—User Determined

For most applications $P_{I/O} < 0.3 \bullet P_{INT}$ and can be neglected.

If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

6.4 POWER DISSIPATION

Characteristic	Symbol	Typ	Max	Unit
Power Dissipation at 25 MHz- Rev C.8µ (see Notes 1 & 2)	PD	85	130	mA
Power Dissipation at 25 MHz -Rev C.65µ (see Notes 1 & 2)	PD	65	90	mA
Power Dissipation at 20 MHz-Rev C.8µ (see Notes 1 & 2)	PD	65	100	mA
Power Dissipation at 20 MHz-Rev C.65µ (see Notes 1 & 2)	PD	50	80	mA
Power Dissipation at 16.67 MHz-Rev C.8µ (see Notes 1 & 2)	PD	54	85	mA
Power Dissipation at 16.67 MHz-Rev C.65µ (see Notes 1 & 2)	PD	44	70	mA
Power Dissipation at 4 MHz-Rev C.8µ (see Notes 1,2 & 3)	PD	40	-	mA
Power Dissipation at 4 MHz-Rev C.65µ (see Notes 1, 2 & 3)	PD	27	-	mA
Power Dissipation at 3.3V 20 MHz-Rev C.65µ (see Note 2)	PD	30	60	mA
Power Dissipation at 3.3V 16.67 MHz-Rev C.65µ (see Note 2)	PD	25	50	mA

NOTES:

1. Values measured with maximum loading of 130 pF on all output pins. Typical means 5.0 V at 25°C. Maximum means guaranteed maximum over maximum temperature (85°C) and voltage (5.5 V).
2. The IMP is tested with the M68000 core executing, all three baud rate generators enabled and clocking at a rate of 64 kHz, and the two general-purpose timers running with a prescaler of 256. Power measurements are not significantly impacted by baud rate generators or timers until their clocking frequency becomes a much more sizable fraction of the system frequency than in these test conditions.
3. The M68000 core will not operate at 4 MHz. This is only for low power mode.

6.5 DC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input High Voltage (Except EXTAL)	V_{IH}	2.0	V_{DD}	V
Input Low Voltage (Except EXTAL)	V_{IL}	V_{SS} - 0.3	0.8	V
Input High Voltage (EXTAL)	V_{CIH}	4.0	VDD	V
Input Low Voltage (EXTAL)	V_{CIL}	V_{SS} - 0.3	0.6	V
Input Leakage Current	II_N	—	20	µA
Input Capacitance All Pins	C_{IN}	—	15	pF
Three-State Leakage Current (2.4/0.5 V)	I_{TSI}	—	20	µA
Open Drain Leakage Current (2.4 V)	I_{OD}	—	20	µA
Output High Voltage (I_{OH} = 400 µA) (see Note)	V_{OH}	V_{DD}–1.0	—	V
Output Low Voltage	V_{OL}			
(I_{OL} = 3.2 mA) A1–A23, PB0–PB11, FC0–FC2, $\overline{CS0}$–$\overline{CS3}$		—	0.5	V
$\overline{IAC}$, $\overline{AVEC}$, $\overline{BG}$, RCLK1, RCLK2, RCLK3, TCLK1, TCLK2, TCLK3, $\overline{RTS1}$, $\overline{RTS2}$, $\overline{RTS3}$, SDS2, PA12, RXD2, RXD3, CTS2, CD2, CD3 $\overline{DREQ}$, BRG1				
(I_{OL} = 5.3 mA) $\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$, R/$\overline{W}$, $\overline{BERR}$		—	0.5	
$\overline{BGACK}$, $\overline{BCLR}$, $\overline{DTACK}$, $\overline{DACK}$, $\overline{RMC}$, D0–D15, $\overline{RESET}$				
(I_{OL} = 7.0 mA) TXD1, TXD2, TXD3		—	0.5	
(I_{OL} = 8.9 mA) $\overline{DONE}$, $\overline{HALT}$, $\overline{BR}$ (as output)		—	0.5	
(I_{OL} = 3.2 mA) CLKO		—	0.4	
Output Drive CLKO	O_{CLK}	—	50	pF
Output Drive ISDN I/F (GCI Mode)	O_{GCI}	—	150	pF
Output Drive All Other Pins	O_{ALL}	—	130	pF
Output Drive Derating Factor for CLKO of 0.030 ns/pF	O_{KF}	20	50	pF
Output Drive Derating Factor for CLKO of 0.035 ns/pF	O_{KF}	50	130	pF
Output Drive Derating Factor for All Other Pins 0.035 ns/pF	O_{KF}	20	130	pF
Output Drive Derating Factor for All Other Pins 0.055 ns/pF	O_{KF}	130	220	pF
Power	V_{DD}	4.5	5.5	V
Common	V_{SS}	0	0	V

NOTE: The maximum I_{OH} for a given pin is one-half the I_{OL} rating for that pin. For an I_{OH} between 400 µA and I_{OL}/2 mA, the minimum V_{OH} is calculated as: V_{DD} - (1 +.05 V/mA(I_{OH} -.400 mA)).

NOTE: All AC specs are assume an output load of 130pf (except for CLKO).

6.6 DC ELECTRICAL CHARACTERISTICS—NMSI1 IN IDL MODE

Characteristic	Symbol	Min	Max	Unit	Condition
Input Pin Characteristics: L1CLK, L1SY1, L1RXD, L1GR					
Input Low Level Voltage	V_{IL}	-10%	+ 20%	V	(% of V_{DD})
Input High Level Voltage	V_{IH}	V_{DD} - 20%	V_{DD} + 10%	V	
Input Low Level Current	II_L	—	± 10	µA	$V_{in} = V_{ss}$
Input High Level Current	II_H	—	± 10	µA	$V_{in} = V_{DD}$
Output Pin Characteristics: L1TXD, SDS1- SDS2, L1RQ					
Output Low Level Voltage	V_{OL}	0	1.0	V	I_{OL} = 5.0 mA
Output High Level Voltage	V_{OH}	V_{DD} - 1.0	V_{DD}	V	I_{OH} = 400 µA

6.7 AC ELECTRICAL SPECIFICATIONS—CLOCK TIMING

(see Figure 6-1, Figure 6-2, Figure 6-3, and Figure 6-4)

			16.67 MHz		20 MHz		25 MHz		
Num.	**Characteristic**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
	Frequency of Operation	f	8	16.67	8	20	8	25	MHz
1	Clock Period (EXTAL) (See note 3)	t_{cyc}	60	125	50	125	40	125	ns
2, 3	Clock Pulse Width (EXTAL)	t_{CL}, t_{CH}	25	62.5	21	62.5	16	62.5	ns
4, 5	Clock Rise and Fall Times (EXTAL)	t_{Cr}, t_{Cf}	—	5	—	4	—	4	ns
5a	EXTAL to CLKO Delay (See Notes 1 and 2)	t_{CD}	2	11	2	9	2	7	ns

NOTE:
1. CLKO loading is 50 pF max.
2. CLKO skew from the rising and falling edges of EXTAL will not differ from each other by more than 1 ns, if the EXTAL rise time equals the EXTAL fall time.
3. You may not stop the clock input at any time.

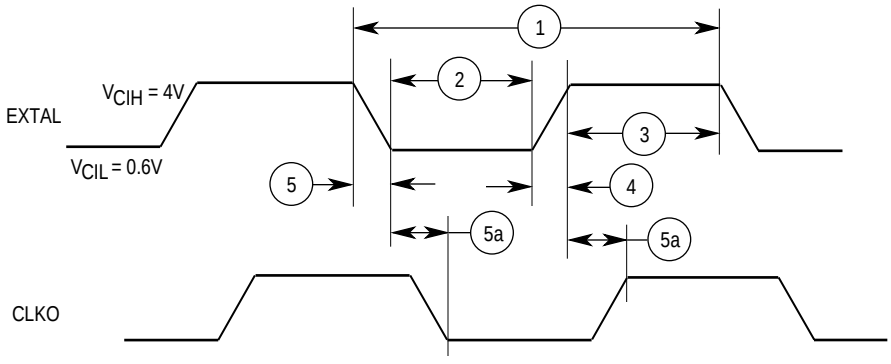


Figure 6-1. Clock Timing Diagram

6.8 AC ELECTRICAL SPECIFICATIONS—IMP BUS MASTER CYCLES

(see Figure 6-2, Figure 6-3, Figure 6-4, and Figure 6-5))

			16.67 MHz		20 MHz		25 MHz		
Num.	**Characteristic**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
6	Clock High to FC, Address Valid	$t_{CHFCADV}$	0	45	0	40	0	30	ns
7	Clock High to Address, Data Bus High Impedance (Maximum)	t_{CHADZ}	—	50	—	42	—	33	ns
8	Clock High to Address, FC Invalid (Minimum)	t_{CHAFI}	0	—	0	—	0	—	ns
9	Clock High to $\overline{AS}$, $\overline{DS}$ Asserted (see Note 1)	t_{CHSL}	3	30	3	25	3	20	ns
11	Address, FC Valid to $\overline{AS}$, $\overline{DS}$ Asserted (Read) $\overline{AS}$ Asserted Write (see Note 2)	t_{AFCVSL}	15	—	12	—	10	—	ns
12	Clock Low to $\overline{AS}$, $\overline{DS}$ Negated (see Note 1)	t_{CLSH}	—	30	—	25	—	20	ns
13	$\overline{AS}$, $\overline{DS}$ Negated to Address, FC Invalid (see Note 2)	t_{SHAFI}	15	—	12	—	10	—	ns
14	$\overline{AS}$ (and $\overline{DS}$ Read) Width Asserted (see Note 2)	t_{SL}	120	—	100	—	80	—	ns
14A	$\overline{DS}$ Width Asserted, Write (see Note 2)	t_{DSL}	60	—	50	—	40	—	ns
15	$\overline{AS}$, $\overline{DS}$ Width Negated (see Note 2)	t_{SH}	60	—	50	—	40	—	ns
16	Clock High to Control Bus High Impedance	t_{CHCZ}	—	50	—	42	—	33	ns
17	$\overline{AS}$, $\overline{DS}$ Negated to R/$\overline{W}$ Invalid (see Note 2)	t_{SHRH}	15	—	12	—	10	—	ns
18	Clock High to R/$\overline{W}$ High (see Note 1)	t_{CHRH}	—	30	—	25	—	20	ns
20	Clock High to R/$\overline{W}$ Low (see Note 1)	t_{CHRL}	—	30	—	25	—	20	ns
20A	$\overline{AS}$ Asserted to R/$\overline{W}$ Low (Write) (see Notes 2 and 6)	t_{ASRV}	—	10	—	10	—	7	ns
21	Address FC Valid to R/$\overline{W}$ Low (Write) (see Note 2)	t_{AFCVRL}	15	—	12	—	10	—	ns
22	R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write) (see Note 2)	t_{RLSL}	30	—	25	—	20	—	ns
23	Clock Low to Data-Out Valid	t_{CLDO}	—	30	—	25	—	20	ns
25	$\overline{AS}$, $\overline{DS}$, Negated to Data-Out Invalid (Write) (see Note 2)	t_{SHDOI}	15	—	12	—	10	—	ns
26	Data-Out Valid to $\overline{DS}$ Asserted (Write) (see Note 2)	t_{DOSL}	15	—	12	—	10	—	ns
27	Data-In Valid to Clock Low (Setup Time on Read) (see Note 5)	t_{DICL}	7	—	6	—	5	—	ns
28	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DTACK}$ Negated (Asynchronous Hold) (see Note 2)	t_{SHDAH}	0	110	0	95	0	75	ns
29	$\overline{AS}$, $\overline{DS}$ Negated to Data-In Invalid (Hold Time on Read)	t_{SHDII}	0	—	0	—	0	—	ns
30	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{BERR}$ Negated	t_{SHBEH}	0	—	0	—	0	—	ns
31	$\overline{DTACK}$ Asserted to Data-In Valid (Setup Time) (see Notes 2 and 5)	t_{DALDI}	—	50	—	42	—	33	ns
32	$\overline{HALT}$ and $\overline{RESET}$ Input Transition Time	t_{RHr}, t_{RHf}	—	150	—	150	—	150	ns
33	Clock High to $\overline{BG}$ Asserted	t_{CHGL}	—	30	—	25	—	20	ns
34	Clock High to $\overline{BG}$ Negated	t_{CHGH}	—	30	—	25	—	20	ns
35	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted (see Note 11)	t_{BRLGL}	2.5	4.5	2.5	4.5	2.5	4.5	clks
36	$\overline{BR}$ Negated to $\overline{BG}$ Negated (see Note 7)	t_{BRHGH}	1.5	2.5	1.5	2.5	1.5	2.5	clks

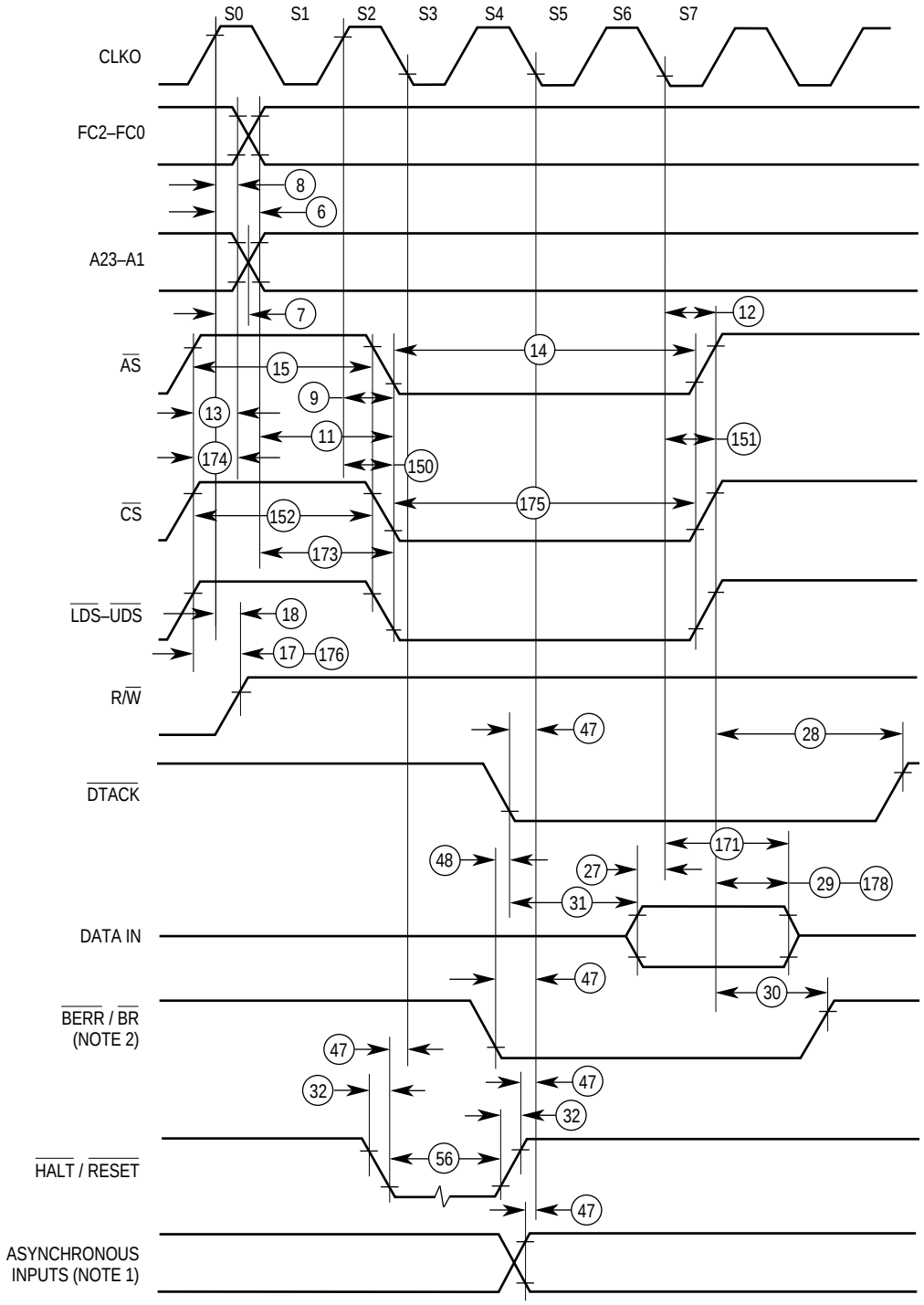
			16.67 MHz		20 MHz		25 MHz		
Num.	**Characteristic**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	t_{GALGH}	2.5	4.5	2.5	4.5	2.5	4.5	clks
37A	$\overline{BGACK}$ Asserted to $\overline{BR}$ Negated (see Note 8)	t_{GALBRH}	10	1.5	10	1.5	10	1.5	ns/ clks
38	$\overline{BG}$ Asserted to Control, Address, Data Bus High Impedance ($\overline{AS}$ Negated)	t_{GLZ}	—	50	—	42	—	33	ns
39	$\overline{BG}$ Width Negated	t_{GH}	1.5	—	1.5	—	1.5	—	clks
40	$\overline{BGACK}$ Asserted to Address Valid	t_{GALAV}	15	—	15	—	15	—	ns
41	$\overline{BGACK}$ Asserted to $\overline{AS}$ Asserted	t_{GALASA}	30	—	30	—	20	—	ns
44	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{AVEC}$ Negated	t_{SHVPH}	0	50	0	42	0	33	ns
46	$\overline{BGACK}$ Width Low	t_{GAL}	1.5	—	1.5	—	1.5	—	clks
47	Asynchronous Input Setup Time (see Note 5)	t_{ASI}	10	—	10	—	7	—	ns
48	$\overline{BERR}$ Asserted to $\overline{DTACK}$ Asserted (see Notes 2 and 3)	t_{BELDAL}	10	—	10	—	7	—	ns
53	Data-Out Hold from Clock High	t_{CHDOI}	0	—	0	—	0	—	ns
55	R/$\overline{W}$ Asserted to Data Bus Impedance Change	t_{RLDBD}	0	—	0	—	0	—	ns
56	$\overline{HALT}$/$\overline{RESET}$ Pulse Width (see Note 4)	t_{HRPW}	10	—	10	—	10	—	clks
57	$\overline{BGACK}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven	t_{GASD}	1.5	—	1.5	—	1.5	—	clks
57A	$\overline{BGACK}$ Negated to FC	t_{GAFD}	1	—	1	—	1	—	clks
58	$\overline{BR}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven (see Note 7)	t_{RHSD}	1.5	—	1.5	—	1.5	—	clks
58A	$\overline{BR}$ Negated to FC (see Note 7)	t_{RHFD}	1	—	1	—	1	—	clks
60	Clock High to $\overline{BCLR}$ Asserted	t_{CHBCL}	—	30	—	25	—	20	ns
61	Clock High to $\overline{BCLR}$ High Impedance (See Note 10)	t_{CHBCH}	—	30	—	25	—	20	ns
62	Clock Low (S0 Falling Edge during read) to $\overline{RMC}$ Asserted	t_{CLRML}	—	30	—	25	—	20	ns
63	Clock High (during write) to $\overline{RMC}$ Negated	t_{CHRMH}	—	30	—	25	—	20	ns
64	$\overline{RMC}$ Negated to $\overline{BG}$ Asserted (see Note 9)	t_{RMHGL}	—	30	—	25	—	20	ns

NOTES:

1. For loading capacitance of less than or equal to 50 pF, subtract 4 ns from the value given in the maximum columns.
2. Actual value depends on clock period since signals are driven/latched on different CLKO edges. To calculate the actual spec for other clock frequencies, the user may derive the formula for each specification. First, derive the margin factor as: M = N(P/2) - Sa
   where N is the number of one-half CLKO periods between the two events as derived from the timing diagram, P is the rated clock period of the device for which the specs were derived (e.g., 60 ns with a 16.67-MHz device or 50 ns with a 20 MHz device), and Sa is the actual spec in the data sheet. Thus, for spec 14 at 16.67 MHz:
   M = 5(60 ns/2) - 120 ns = 30 ns.
   Once the margin (M) is calculated for a given spec, a new value of that spec (Sn) at another clock frequency with period (Pa) is calculated as:
   Sn = N(Pa/2) - M
   Thus for spec 14 at 12.5 MHz:
   Sn = 5(80 ns/2) - 30 ns = 170 ns.
   These two formulas assume a 50% duty cycle. Otherwise, if N is odd, the previous values N(P/2) and N(Pa/2) must be reduced by X, where X is the difference between the nominal pulse width and the minimum pulse width of the EXTAL input clock for that duty cycle.
3. If #47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, #48 may be ignored. In the absence of $\overline{DTACK}$, $\overline{BERR}$ is a

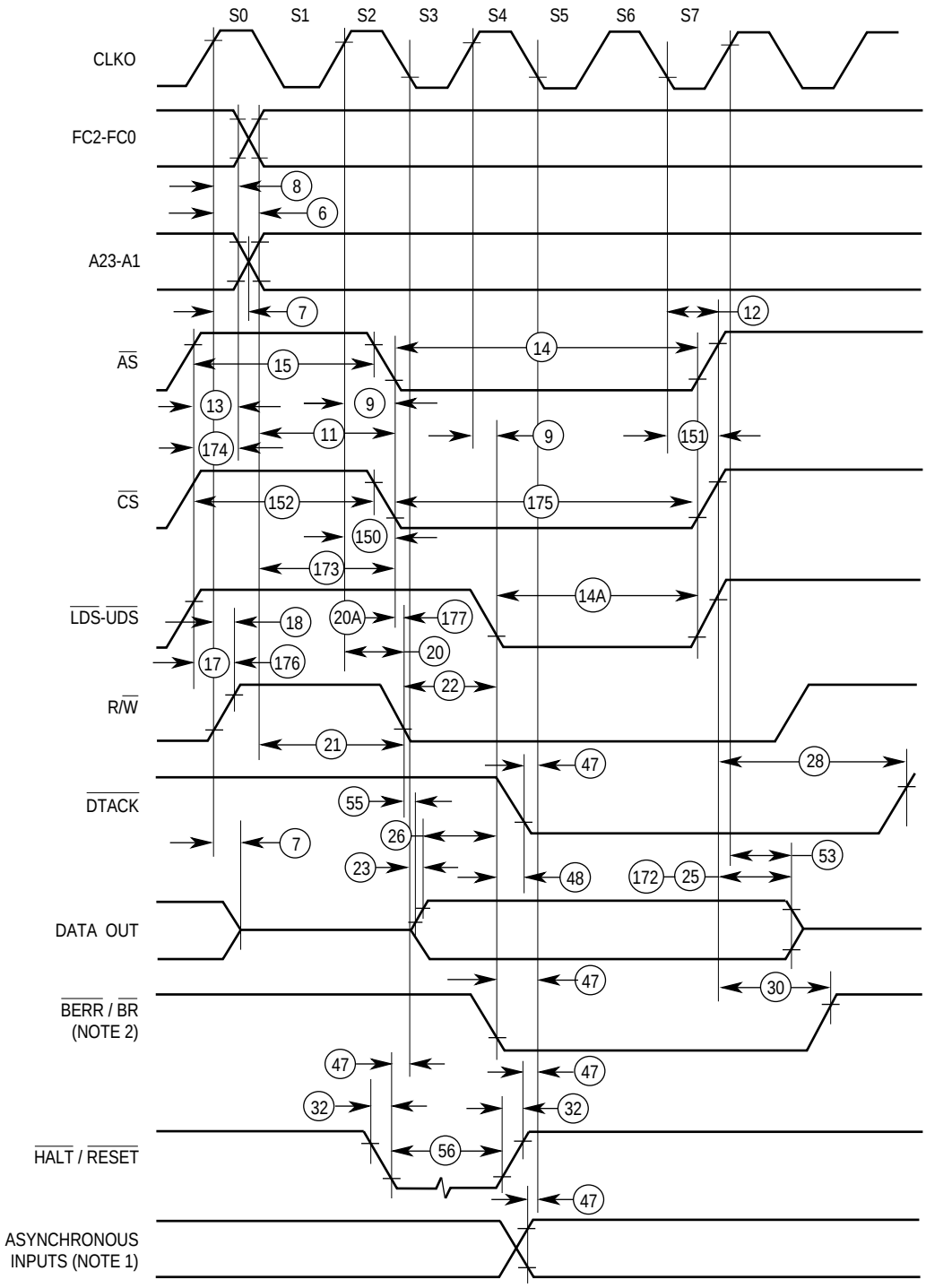
synchronous input using the asynchronous input setup time (#47).

4. For power-up, the MC68302 must be held in the reset state for 100 ms to allow stabilization of on-chip circuit. After the system is powered up #56 refers to the minimum pulse width required to reset the processor.
5. If the asynchronous input setup (#47) requirement is satisfied for $\overline{\text{DTACK}}$, the $\overline{\text{DTACK}}$ asserted to data setup time (#31) requirement can be ignored. The data must only satisfy the data-in to clock low setup time (#27) for the following clock cycle.
6. When $\overline{\text{AS}}$ and R/$\overline{\text{W}}$ are equally loaded (±20%), subtract 5 ns from the values given in these columns.
7. The MC68302 will negate $\overline{\text{BG}}$ and begin driving the bus if external arbitration logic negates $\overline{\text{BR}}$ before asserting $\overline{\text{BGACK}}$.
8. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, $\overline{\text{BG}}$ may be reasserted.
9. This specification is valid only when the RMCST bit is set in the SCR register.
10. Occurs on S0 of SDMA read/write access when the SDMA becomes bus master.
11. Specification may be exceeded during the TAS instruction if the RMCST bit in the SCR is set.



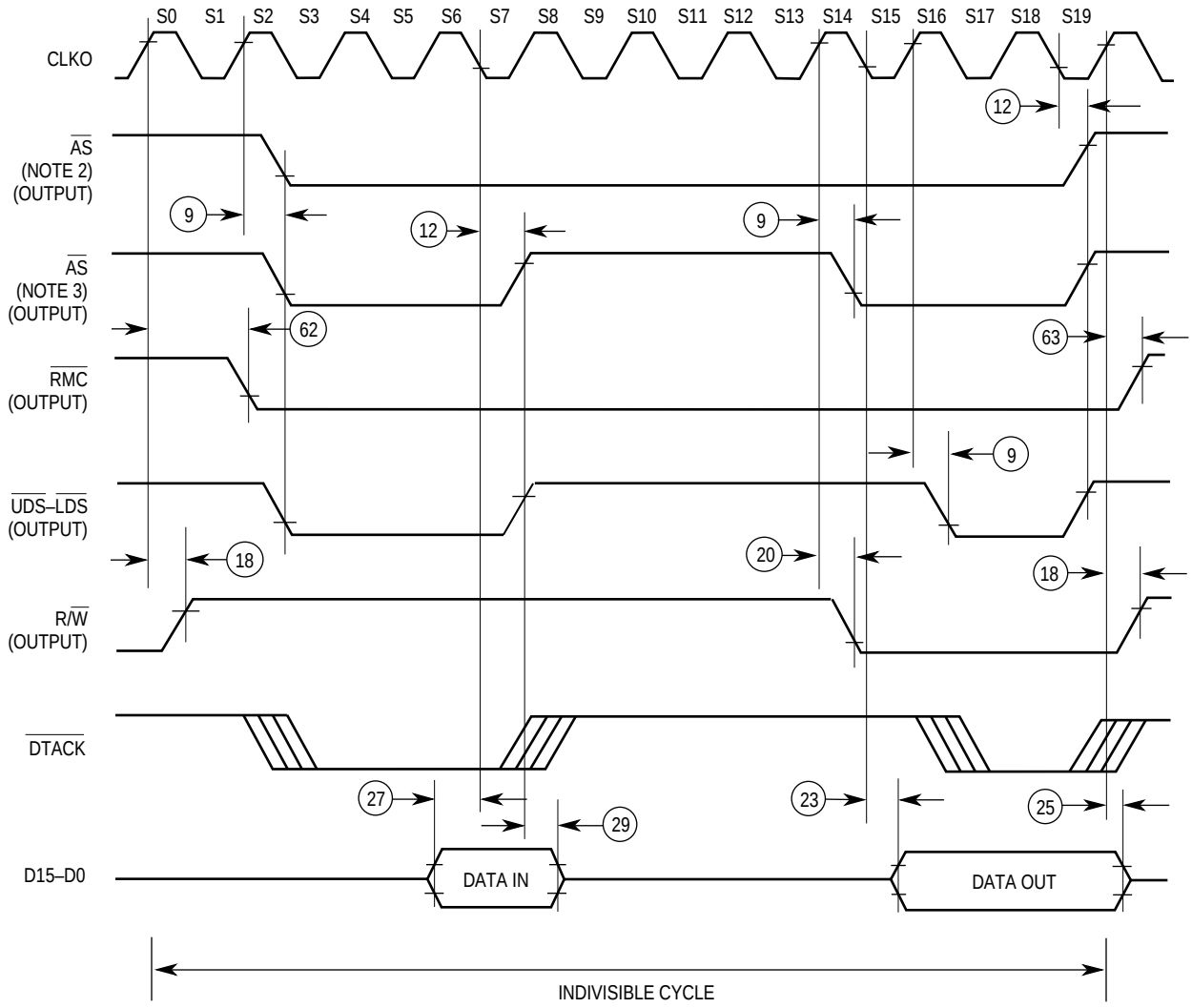
NOTES:
1. Setup time for the asynchronous inputs IPL2–IPL0 guarantees their recognition at the next falling edge of the clock.
2. BR need fall at this time only to insure being recognized at the end of the bus cycle.
3. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 volts and 2.0 volts.

Figure 6-2. Read Cycle Timing Diagram



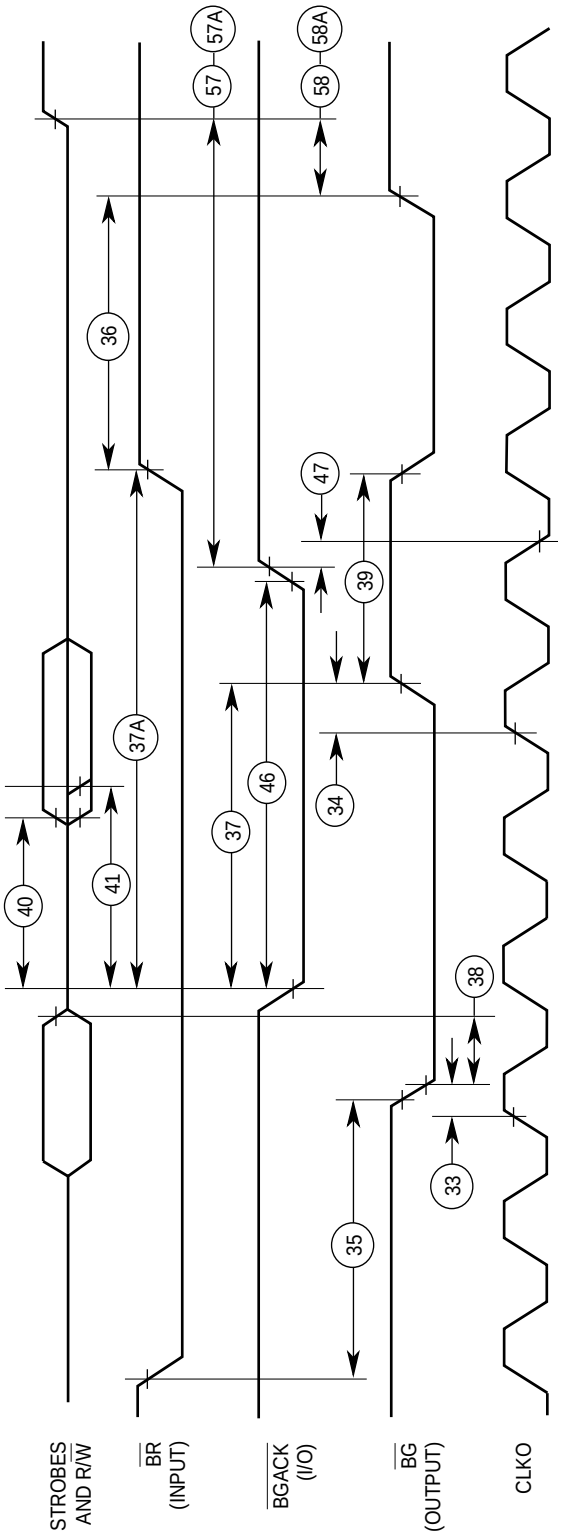
NOTES:
1. Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between between 0.8 volt and 2.0 volts.
2. Because of loading variations, R/W may be valid after AS even though both are initiated by the rising edge of S2 (specification #20A)
3. Each wait state is a full clock cycle inserted between S4 and S5.

Figure 6-3. Write Cycle Timing Diagram



NOTES:
1. For other timings than RMC, see Figures 6-2 and 6-3.
2. RMCST = 0 in the SCR.
3. RMCST = 1 in the SCR.
4. Wait states may be inserted between S4 and S5 during the write cycle and between S16 and S17 during the read cycle.
5. Read-modify-write cycle is generated only by the TAS instruction.

Figure 6-4. Read-Modify-Write Cycle Timing Diagram



NOTE: Setup time to the clock (#47) for the asynchronous inputs BERR, BGACK, BR, DTACK, AND IPL2–IPL0 guarantees their recognition at the next falling edge of the clock.

Figure 6-5. Bus Arbitration Timing Diagram

6.9 AC ELECTRICAL SPECIFICATIONS—DMA (see Figure 6-6 and Figure 6-7)

Num.	Characteristic	Symbol	16.67 MHz		20 MHz		25 MHz		Unit
			Min	Max	Min	Max	Min	Max	
80	$\overline{DREQ}$ Asynchronous Setup Time (see Note 1)	t_{REQASI}	15	—	15	—	10	—	ns
81	$\overline{DREQ}$ Width Low (see Note 2)	t_{REQL}	2	—	2	—	2	—	clks
82	$\overline{DREQ}$ Low to $\overline{BR}$ Low (see Notes 3 and 4)	$t_{REQLBRL}$	—	2	—	2	—	2	clks
83	Clock High to $\overline{BR}$ Low (see Notes 3 and 4)	t_{CHBRL}	—	30	—	25	—	20	ns
84	Clock High to $\overline{BR}$ High Impedance (see Notes 3 and 4)	t_{CHBRZ}	—	30	—	25	—	20	ns
85	$\overline{BGACK}$ Low to $\overline{BR}$ High Impedance (see Notes 3 and 4)	t_{BKLBRZ}	30	—	25	—	20	—	ns
86	Clock High to $\overline{BGACK}$ Low	t_{CHBKL}	—	30	—	25	—	20	ns
87	$\overline{AS}$ and $\overline{BGACK}$ High (the Latest One) to $\overline{BGACK}$ Low (when $\overline{BG}$ Is Asserted)	t_{ABHBKL}	1.5	2.5 +30	1.5	2.5 +25	1.5	2.5 +20	clks ns
88	$\overline{BG}$ Low to $\overline{BGACK}$ Low (No Other Bus Master) (see Notes 3 and 4)	t_{BGLBKL}	1.5	2.5 +30	1.5	2.5 +25	1.5	2.5 +20	clks ns
89	$\overline{BR}$ High Impedance to $\overline{BG}$ High (see Notes 3 and 4)	t_{BRHBGH}	0	—	0	—	0	—	ns
90	Clock on which $\overline{BGACK}$ Low to Clock on which $\overline{AS}$ Low	$t_{CLBKLAL}$	2	2	2	2	2	2	clks
91	Clock High to $\overline{BGACK}$ High	t_{CHBKH}	—	30	—	25	—	20	ns
92	Clock Low to $\overline{BGACK}$ High Impedance	t_{CLBKZ}	—	15	—	15	—	10	ns
93	Clock High to $\overline{DACK}$ Low	t_{CHACKL}	—	30	—	25	—	20	ns
94	Clock Low to $\overline{DACK}$ High	t_{CLACKH}	—	30	—	25	—	20	ns
95	Clock High to $\overline{DONE}$ Low (Output)	t_{CHDNL}	—	30	—	25	—	20	ns
96	Clock Low to $\overline{DONE}$ High Impedance	t_{CLDNZ}	—	30	—	25	—	20	ns
97	$\overline{DONE}$ Input Low to Clock Low (Asynchronous Setup)	t_{DNLTCH}	15	—	15	—	10	—	ns

NOTES:
1. $\overline{DREQ}$ is sampled on the falling edge of CLK in cycle steal and burst modes.
2. If #80 is satisfied for $\overline{DREQ}$, #81 may be ignored.
3. $\overline{BR}$ will not be asserted while $\overline{BG}$, $\overline{HALT}$, or $\overline{BERR}$ is asserted.
4. Specifications are for DISABLE CPU mode only.
5. $\overline{DREQ}$, $\overline{DACK}$, and $\overline{DONE}$ do not apply to the SDMA channels.
6. DMA and SDMA read and write cycle timing is the same as that for the M68000 core.