FEATURES

- 50Msps Update Rate
- 16-Bit Resolution
- High Spectral Purity: 87dB SFDR at 1MHz \( f_{\text{OUT}} \)
- Differential Current Outputs
- 30ns Settling Time
- 5pV-s Glitch Impulse
- Low Power: 180mW from ±5V Supplies
- TTL/CMOS (3.3V or 5V) Inputs
- Small Package: 28-Pin SSOP

DESCRIPTION

The LTC®-1668 is a 16-bit, 50Msps differential current output DAC implemented on a high performance BiCMOS process with laser trimmed, thin-film resistors. The combination of a novel current-steering architecture and a high performance process produces a DAC with exceptional AC and DC performance. This is the first 16-bit DAC in the marketplace to exhibit an SFDR (spurious free dynamic range) of 87dB for an output signal frequency of 1MHz.

Operating from ±5V supplies, the LTC1668 can be configured to provide full-scale output currents up to 10mA. The differential current outputs of the DAC allow single-ended or true differential operation. The –1V to 1V output compliance of the LTC1668 allows the outputs to be connected directly to external resistors to produce a differential output voltage without degrading the converter's linearity. Alternatively, the outputs can be connected to the summing junction of a high speed operational amplifier, or to a transformer.

The LTC1668 is available in a 28-pin SSOP and is fully specified over the industrial temperature range.

LTC and LT are registered trademarks of Linear Technology Corporation.
**LTC1668**

**ABSOLUTE MAXIMUM RATINGS**

(Note 1)
- Supply Voltage (V_{DD}): 6V
- Negative Supply Voltage (V_{SS}): –6V
- Total Supply Voltage (V_{DD} to V_{SS}): 12V
- Digital Input Voltage: –0.3V to (V_{DD} + 0.3V)
- Analog Output Voltage: (I_{OUTA} and I_{OUTB}) (V_{SS} – 0.3V) to (V_{DD} + 0.3V)
- Power Dissipation: 500mW

Operating Temperature Range
- LTC1668C: 0°C to 70°C
- LTC1668I: –40°C to 85°C
- Storage Temperature Range: –65°C to 150°C
- Lead Temperature (Soldering, 10 sec): 300°C

**ELECTRICAL CHARACTERISTICS**

The • denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 5V, V_{SS} = –5V, LADCOM = AGND = DGND = 0V, I_{OUTFS} = 10mA.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Accuracy (Measured at I_{OUTA}, Driving a Virtual Ground)</td>
<td>Resolution</td>
<td></td>
<td>16</td>
<td>Bits</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Monotonicity</td>
<td></td>
<td>14</td>
<td>Bits</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>INL</td>
<td>Integral Nonlinearity</td>
<td>±8</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>DNL</td>
<td>Differential Nonlinearity</td>
<td>±4</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Offset Error</td>
<td></td>
<td>0.1</td>
<td>±0.2</td>
<td>% FSR</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Offset Error Drift</td>
<td></td>
<td>5</td>
<td>ppm/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GE</td>
<td>Gain Error</td>
<td>Internal Reference, R_{IREFIN} = 2k</td>
<td>2</td>
<td>% FSR</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>External Reference, V_{REF} = 2.5V, R_{IREFIN} = 2k</td>
<td>1</td>
<td>% FSR</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Gain Error Drift</td>
<td>Internal Reference</td>
<td>75</td>
<td>ppm/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>External Reference</td>
<td>50</td>
<td>ppm/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>V_{DD} = 5V ±5%</td>
<td>±0.1</td>
<td>% FSR/V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{SS} = –5V ±5%</td>
<td>±0.1</td>
<td>% FSR/V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Analog Output</td>
<td>I_{OUTFS}</td>
<td>Full-Scale Output Current</td>
<td>•</td>
<td>1</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Output Compliance Range</td>
<td>R_IREF = 10mA</td>
<td>•</td>
<td>–1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Output Resistance; R_{IOUTA} R_{IOUTB}</td>
<td>I_{OUTA} B to LADCOM</td>
<td>•</td>
<td>0.7</td>
<td>1.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Output Capacitance</td>
<td></td>
<td>5</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Reference Output</td>
<td>Reference Voltage</td>
<td>REFOUT Tied to I_{REFIN} Through 2kΩ</td>
<td>2.475</td>
<td>2.5</td>
<td>2.525</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Reference Output Drift</td>
<td></td>
<td>25</td>
<td>ppm/°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Reference Output Load Regulation</td>
<td>I_{LOAD} = 0mA to 5mA</td>
<td>6</td>
<td>mV/mA</td>
<td></td>
</tr>
</tbody>
</table>

Consult factory for Military grade parts.
The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25^\circ C \). \( V_{DD} = 5V \), \( V_{SS} = -5V \), \( LADCOM = AGND = DGND = 0V \), \( I_{OUTFS} = 10mA \).

### SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS
--- | --- | --- | --- | --- | --- | ---
Reference Input | Reference Small-Signal Bandwidth | \( I_{FS} = 10mA, C_{COMP1} = 0.1\mu F \) | 20 | | | kHz

### Power Supply

<p>| | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
--- | --- | --- | --- | --- | --- | --- |
| \( V_{DD} \) | Positive Supply Voltage | | 4.75 | 5 | 5.25 | V |
| \( V_{SS} \) | Negative Supply Voltage | | -4.75 | -5 | -5.25 | V |
| \( I_{DD} \) | Positive Supply Current | \( I_{FS} = 10mA, f_{CLK} = 25\text{Msps}, f_{OUT} = 1\text{MHz} \) | 3 | 5 | | mA |
| \( I_{SS} \) | Negative Supply Current | \( I_{FS} = 10mA, f_{CLK} = 25\text{Msps}, f_{OUT} = 1\text{MHz} \) | 33 | 40 | | mA |
| \( P_{DIS} \) | Power Dissipation | \( I_{FS} = 10mA, f_{CLK} = 25\text{Msps}, f_{OUT} = 1\text{MHz} \) | 180 | | | mW |
| | | \( I_{FS} = 1\text{mA}, f_{CLK} = 25\text{Msps}, f_{OUT} = 1\text{MHz} \) | 85 | | | mW |

### Dynamic Performance (Differential Transformer Coupled Output, 50Ω Double Terminated, Unless Otherwise Noted)

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
--- | --- | --- | --- | --- | --- | --- |
| \( f_{CLOCK} \) | Maximum Update Rate | | 50 | 75 | | Msps |
| \( t_s \) | Output Settling Time | To 0.1% FSR | 30 | | | ns |
| \( t_{PD} \) | Output Propagation Delay | | 8 | | | ns |
| | | Glitch Impulse | Single Ended | 15 | 5 | | pV-s |
| | | | Differential | | | | pV-s |
| \( t_r \) | Output Rise Time | | 4 | | | ns |
| \( t_f \) | Output Fall Time | | 4 | | | ns |
| \( I_{NO} \) | Output Noise | \( I_{FS} = 10mA \) | 50 | | | pA/√Hz |
| | | \( I_{FS} = 1\text{mA} \) | 30 | | | pA/√Hz |

### AC Linearity

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
--- | --- | --- | --- | --- | --- | --- |
| SFDR | Spurious Free Dynamic Range to Nyquist | \( f_{CLK} = 25\text{Msps}, f_{OUT} = 1\text{MHz} \) | 78 | 87 | | dB |
| | | 0dB FS Output | | 87 | | dB |
| | | -6dB FS Output | | 86 | | dB |
| | | -12dB FS Output | | 80 | | dB |
| | | -18dB FS Output | | | | dB |
| | | \( f_{CLK} = 50\text{Msps}, f_{OUT} = 1\text{MHz} \) | 84 | | | dB |
| | | \( f_{CLK} = 50\text{Msps}, f_{OUT} = 2.5\text{MHz} \) | 80 | | | dB |
| | | \( f_{CLK} = 50\text{Msps}, f_{OUT} = 5\text{MHz} \) | 77 | | | dB |
| | | \( f_{CLK} = 50\text{Msps}, f_{OUT} = 20\text{MHz} \) | 65 | | | dB |
| | | Spurious Free Dynamic Range Within a Window | \( f_{CLK} = 25\text{Msps}, f_{OUT} = 1\text{MHz}, 2\text{MHz Span} \) | 86 | 96 | | dB |
| | | \( f_{CLK} = 50\text{Msps}, f_{OUT} = 5\text{MHz}, 4\text{MHz Span} \) | 88 | | | dB |
| THD | Total Harmonic Distortion | \( f_{CLK} = 25\text{Msps}, f_{OUT} = 1\text{MHz} \) | -84 | -77 | | dB |
| | | \( f_{CLK} = 50\text{Msps}, f_{OUT} = 5\text{MHz} \) | -76 | | | dB |

### Digital Inputs

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
--- | --- | --- | --- | --- | --- | --- |
| \( V_{IH} \) | Digital High Input Voltage | | 2.4 | | | V |
| \( V_{IL} \) | Digital Low Input Voltage | | 0.8 | | | V |
| \( I_{IN} \) | Digital Input Current | | ±10 | | | μA |
| \( C_{IN} \) | Digital Input Capacitance | | 5 | | | pF |
| \( t_{DS} \) | Input Setup Time | | 8 | | | ns |
| \( t_{DH} \) | Input Hold Time | | 4 | | | ns |
| \( t_{CLKH} \) | Clock High Time | | 5 | | | ns |
| \( t_{CLKL} \) | Clock Low Time | | 8 | | | ns |

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.
**TYPICAL PERFORMANCE CHARACTERISTICS**

**Single Tone SFDR**

- **fCLOCK** = 25Msps
- **fOUT** = 1.007MHz
- **AMPLITUDE** = 0dBFS
- **SFDR** = 86dBc

**2-Tone SFDR**

- **fCLOCK** = 50Msps
- **fOUT1** = 4.028MHz  
  **fOUT2** = 4.419MHz
- **AMPLITUDE 1, 2** = -6dBFS
  **= -14.5dBm**
- **SFDR > 77dBc**

**Integral Nonlinearity**

- **DIGITAL INPUT CODE**:
  - 16384
  - 32768
  - 49152
  - 65535

**Differential Nonlinearity**

- **DIGITAL INPUT CODE**:
  - 0
  - 16384
  - 32768
  - 49152
  - 65535

---

**PIN FUNCTIONS**

**REFOUT (Pin 15):** Internal Reference Voltage Output. Nominal value is 2.5V. Requires a 0.1μF bypass capacitor to AGND.

**IREFIN (Pin 16):** Reference Input Current. Nominal value is 1.25mA for **IFS** = 10mA. **IFS = IREFIN \* 8.**

**AGND (Pin 17):** Analog Ground.

**LADCOM (Pin 18):** Attenuator Ladder Common. Normally tied to GND.

**IOUT B (Pin 19):** Complementary DAC Output Current. Full-scale output current occurs when all data bits are 0s.

**IOUT A (Pin 20):** DAC Output Current. Full-scale output current occurs when all data bits are 1s.

**COMP1 (Pin 21):** Current Source Control Amplifier Compensation. Bypass to **VSS** with 0.1μF.

**COMP2 (Pin 22):** Internal Bypass Point. Bypass to **VSS** with 0.1μF.

**VSS (Pin 23):** Negative Supply Voltage. Nominal value is -5V.

**DGND (Pin 24):** Digital Ground.

**VDD (Pin 25):** Positive Supply Voltage. Nominal value is 5V.

**CLK (Pin 26):** Clock Input. Data is latched and the output is updated on positive edge of clock.

**DB15 to DB0 (Pins 27, 28, 1 to 14):** Digital Input Data Bits.
The LTC1668 is a high speed current steering 16-Bit DAC made on an advanced BiCMOS process. Precision thin film resistors and well matched bipolar transistors result in excellent DC linearity and stability. A low glitch current switching design gives excellent AC performance at sample rates up to 50Msps. The device is complete with a 2.5V internal bandgap reference and edge triggered latches, and sets a new standard for DAC applications requiring very high dynamic range at output frequencies up to several megahertz.

Referring to the Block Diagram, the DAC contains an array of current sources that are steered to IOUTA or IOUTB with NMOS differential current switches. The four most significant bits, DB15 to DB12 are made up of 15 current segments of equal weight. The lower bits, DB11 to DB0 are binary weighted, using a combination of current scaling and a differential resistive attenuator ladder. All bits and segments are precisely matched, both in current weight for DC linearity, and in switch timing for low glitch impulse and low spurious tone AC performance.

Setting the Full-Scale Current, IOUTFS

The full-scale DAC output current, IOUTFS, is nominally 10mA, and can be adjusted down to 1mA. Placing a resistor, RSET, between the REFOUT pin, and the IREFIN pin sets IOUTFS as follows.

The internal reference control loop amplifier maintains a virtual ground at IREFIN by servoing the internal current source, IINT, to sink the exact current flowing into IREFIN. IINT is a scaled replica of the DAC current sources and IOUTFS = 8 • (IREFIN), therefore:

IOUTFS = 8 • (IREFIN) = 8 • (VREF/RSET)  \( \text{(1)} \)

For example, if \( R_{\text{SET}} = 2k \) and is tied to \( V_{\text{REF}} = \text{REFOUT} = 2.5V \), IREFIN = 2.5/2k = 1.25mA and IOUTFS = 8 • (1.25mA) = 10mA.

The reference control loop requires a capacitor on the COMP1 pin for compensation. For optimal AC performance, \( C_{\text{COMP1}} \) should be connected to VSS and be placed very close to the package (less than 0.1µF).

For fixed reference voltage applications, \( C_{\text{COMP1}} \) should be 0.1µF or more. The reference control loop small-signal bandwidth is approximately \( 1/(2\pi) \cdot C_{\text{COMP1}} \cdot 80 \) or 20kHz for \( C_{\text{COMP1}} = 0.1\mu F \).

Internal Reference Output—REFOUT

The onboard 2.5V bandgap voltage reference drives the REFOUT pin. It is trimmed and specified to drive a 2k resistor tied from REFOUT to IREFIN, corresponding to a 1.25mA load (IOUTFS = 10mA). REFOUT has nominal output impedance of 6Ω, or 0.24% per mA, so it must be buffered to drive any additional external load. A 0.1µF capacitor is required on the REFOUT pin for compensation. Note that this capacitor is required for stability, even if the internal reference is not being used.

DAC Transfer Function

The LTC1668 uses straight binary digital coding. The complementary current outputs, IOUTA and IOUTB, sink current from 0 to IOUTFS. For IOUTFS = 10mA (nominal), IOUTA swings from 0mA when all bits are low (i.e., Code = 0) to 10mA when all bits are high (i.e., Code = 65535) (decimal representation). IOUTB is complementary to IOUTA. IOUTA and IOUTB are given by the following formulas:

\[ I_{\text{OUTA}} = I_{\text{OUTFS}} \cdot \frac{\text{DAC Code}}{65536} \]
\[ I_{\text{OUTB}} = I_{\text{OUTFS}} \cdot \frac{65535 - \text{DAC Code}}{65536} \]

In typical applications, the LTC1668 differential output currents either drive a resistive load directly or drive an equivalent resistive load through a transformer, or as the feedback resistor of an I-to-V converter. The voltage outputs generated by the IOUTA and IOUTB output currents are then:

\[ V_{\text{OUTA}} = I_{\text{OUTA}} \cdot R_{\text{LOAD}} \]
\[ V_{\text{OUTB}} = I_{\text{OUTB}} \cdot R_{\text{LOAD}} \]

The differential voltage is:

\[ V_{\text{DIFF}} = V_{\text{OUTA}} - V_{\text{OUTB}} = (I_{\text{OUTA}} - I_{\text{OUTB}}) \cdot (R_{\text{LOAD}}) \]
Substituting the values found earlier for $I_{OUT\ A}$, $I_{OUT\ B}$ and $I_{OUTFS}$:

$$V_{DIFF} = \left(\frac{2 \cdot DAC\ Code - 65535}{65536}\right) \cdot 8 \cdot \left(\frac{R_{LOAD}}{R_{SET}}\right) \cdot (V_{REF}) \tag{7}$$

From these equations some of the advantages of differential mode operation can be seen. First, any common mode noise or error on $I_{OUT\ A}$ and $I_{OUT\ B}$ is cancelled. Second, the signal power is twice as large as in the single-ended case. Third, any errors and noise that multiply times $I_{OUT\ A}$ and $I_{OUT\ B}$, such as reference or $I_{OUTFS}$ noise, cancel near mid-scale, where AC signal waveforms tend to spend the most time. Fourth, this transfer function is bipolar; e.g. the output swings positive and negative around a zero output at mid-scale input, which is more convenient for AC applications.

Note that the term $(R_{LOAD}/R_{SET})$ appears in both the differential and single-ended transfer functions. This means that the Gain Error of the DAC depends on the ratio of $R_{LOAD}$ to $R_{SET}$, and the Gain Error tempco is affected by the temperature tracking of $R_{LOAD}$ with $R_{SET}$. Note also that the absolute tempco of $R_{LOAD}$ is very critical for DC nonlinearity. As the DAC output changes from 0mA to 10mA the $R_{LOAD}$ resistor will heat up slightly, and even a very low tempco can produce enough INL bowing to be significant at the 16-bit level. This effect disappears with medium to high frequency AC signals due to the slow thermal time constant of the load resistor.

**Analog Outputs**

The LTC1668 has two complementary current outputs, $I_{OUT\ A}$ and $I_{OUT\ B}$ (see DAC Transfer Function). The output impedance of $I_{OUT\ A}$ and $I_{OUT\ B}$ ($R_{OUT\ A}$ and $R_{OUT\ B}$) is typically 1.1kΩ to LADCOM. (See the Equivalent Analog Output Circuit, Figure 1.) The LADCOM pin is the common connection for the internal DAC attenuator ladder. It usually is tied to analog ground, but more generally it should connect to the same potential as the lead resistors on $I_{OUT\ A}$ and $I_{OUT\ B}$. The LADCOM pin carries a constant current to $V_{SS}$ of approximately 0.32 • ($I_{OUTFS}$), plus any current that flows from $I_{OUT\ A}$ and $I_{OUT\ B}$ through the $R_{OUT\ A}$ and $R_{OUT\ B}$ resistors.

The specified output compliance voltage range is ±1V. The DC linearity specifications, INL and DNL, are trimmed and guaranteed on $I_{OUT\ A}$ into the virtual ground of an I-to-V converter, but are typically very good over the full output compliance range. Above 1V the output current will start to increase as the DAC current steering switch impedance decreases, degrading both DC and AC linearity. Below –1V, the DAC switches will start to approach the transition from saturation to linear region. This will degrade AC performance first, due to nonlinear capacitance and increased glitch impulse. AC distortion performance is optimal at amplitudes less than ±0.5Vp-p on $I_{OUT\ A}$ and $I_{OUT\ B}$ due to nonlinear capacitance and other large-signal effects. At first glance, it may seem counter-intuitive to decrease the signal amplitude when trying to optimize SFDR. However, the error sources that affect AC performance generally behave as additive currents, so decreasing the load impedance to reduce signal voltage amplitude will reduce most spurious signals by the same amount.

The LTC1668 is specified to operate with full-scale output current, $I_{OUTFS}$, from the nominal 10mA down to 1mA. This can be useful to reduce power dissipation or to adjust full-scale value. However, that the LTC1668 DC and AC accuracy is specified only at $I_{OUTFS} = 10$mA, and DC and AC accuracy will fall off significantly at lower $I_{OUTFS}$ values. At $I_{OUTFS} = 1$mA, INL and DNL typically degrade to the 14-bit to 13-bit level, compared to 16-bit to 15-bit typical accuracy at 10mA $I_{OUTFS}$. Increasing $I_{OUTFS}$ from 1mA, the
accuracy improves rapidly, roughly in proportion to $1/I_{OUTFS}$. The AC performance tends to be less affected by reducing $I_{OUTFS}$, except for the unavoidable affects on SFDR and THD due to increased INL and DNL.

**Output Configurations**

Based on the specific application requirements, the LTC1668 allows a choice of the best of several output configurations. Voltage outputs can be generated by external load resistors, transformer coupling or with an op amp I-to-V converter. Single-ended DAC output configurations use only one of the outputs, preferably $I_{OUT A}$, to produce a single-ended voltage output. Differential mode configurations use the difference between $I_{OUT A}$ and $I_{OUT B}$ to generate an output voltage, $V_{DIFF}$, as shown in equation 7. Differential mode gives much better accuracy in most AC applications. Because the DAC chip is the point of interface between the digital input signals and the analog output, some small amount of noise coupling to $I_{OUT A}$ and $I_{OUT B}$ is unavoidable. Most of that digital noise is common mode and is canceled by the differential mode circuit. Other significant digital noise components can be modeled as $V_{REF}$ or $I_{OUTFS}$ noise. In single-ended mode, $I_{OUTFS}$ noise is gone at zero scale and is fully present at full scale. In differential mode, $I_{OUTFS}$ noise is cancelled at midscale input, corresponding to zero analog output. Many AC signals, including broadband and multitone communications signals with high peak to average ratios, stay mostly near midscale.

Differential transformer-coupled output configurations usually give the best AC performance. An example is the AC Characterization Setup circuit, Figure 2. The advantages of transformer coupling include excellent rejection of common mode distortion and noise over a broad frequency range and convenient differential-to-single-ended conversion with isolation or level shifting. Also, as much as twice the power can be delivered to the load, and impedance matching can be accomplished by selecting the appropriate transformer turns ratio. The center tap on the primary side of the transformer is tied to ground to provide the DC current path for $I_{OUT A}$ and $I_{OUT B}$. For low distortion, the DC average of the $I_{OUT A}$ and $I_{OUT B}$ currents must be exactly equal to avoid biasing the core. This is especially important for compact RF transformers with small cores. The circuit in Figure 2 uses a Mini-Circuits T1-1T RF transformer with a 1:1 turns ratio. The load

![Figure 2. AC Characterization Setup](image-url)
APPLICATIONS INFORMATION

resistance on IOUTA and IOUTB is equivalent to a single
differential resistor of 50Ω, and the 1:1 turns ratio means
the output impedance from the transformer is 50Ω. Note
that the load resistors are optional, and they dissipate half
of the output power. However, in lab environments or
when driving long transmission lines it is very desirable to
have a 50Ω output impedance. This could also be done
with a 50Ω resistor at the transformer secondary, but
putting the load resistors on IOUTA and IOUTB is preferred
since it reduces the current through the transformer. At
signal frequencies lower than about 1MHz, the trans-
former core size required to maintain low distortion gets
larger, and at some lower frequencies this becomes
impractical.

A differential resistor loaded output configuration is shown
in the Block Diagram. It is simple and economical, but it
can drive only differential loads with impedance levels and
amplitudes appropriate for the DAC outputs.

The recommended single-ended resistor loaded configu-
ration is essentially the same circuit as the differential
resistor loaded, case—simply use the IOUTA output,
referred to ground. Rather than tying the unused IOUTB
output to ground, it is preferred to load it with the equiva-
 lent RLOAD of IOUTA. Then IOUTB will still swing with a
waveform complementary to IOUTA.

Adding an op amp differential to single-ended converter
circuit to the differential resistor loaded output gives the
circuit of Figure 10.

This circuit complements the capabilities of the trans-
former-coupled application at lower frequencies, since
available op amps can deliver good AC distortion perform-
ance at signal frequencies of a few MHz down to DC. The
optional capacitor adds a single real pole of filtering, and
helps reduce distortion by limiting the high frequency
signal amplitude at the op amp inputs. The circuit swings
±1V around ground.

Figure 3 shows a simplified circuit for a single-ended
output using I-to-V converter to produce a unipolar
buffered voltage output. This configuration typically has
the best DC linearity performance, but its AC distortion at
higher frequencies is limited by U1’s slewing capabilities.

Digital Interface

The LTC1668 has 16 parallel inputs that are latched on the
rising edge of the clock input. They accept CMOS levels
from either 5V or 3.3V logic and can accept clock rates of
up to 50MHz.

Referring to the Timing Diagram and Block Diagram, the
data inputs go to master-slave latches that update on the
rising edge of the clock. The input logic thresholds, VIH =
2.4V min, VIL = 0.8V max, work with 3.3V or 5V CMOS
levels over temperature. The guaranteed setup time, tDS,
is 8ns minimum and the hold time, tDH, is 4ns minimum.
The minimum clock high and low times are guaranteed at
6ns and 8ns, respectively. These specifications allow the
LTC1668 to be clocked at up to 50Msps minimum.

For best AC performance, the data and clock waveforms
need to be clean and free of undershoot and overshoot.
Clock and data interconnect lines should be twisted pair,
coax or microstrip, and proper line termination is impor-
tant. If the digital input signals to the DAC are considered
as analog AC voltage signals, they are rich in spectral
components over a broad frequency range, usually in-
cluding the output signal band of interest. Therefore, any
direct coupling of the digital signals to the analog output
will produce spurious tones that vary with the exact digital
input pattern.

Clock jitter should be minimized to avoid degrading the
noise floor of the device in AC applications, especially
where high output frequencies are being generated. Any
noise coupling from the digital inputs to the clock input will
APPLICATIONS INFORMATION

cause phase modulation of the clock signal and the DAC waveform, and can produce spurious tones. It is normally best to place the digital data transitions near the falling clock edge, well away from the active rising clock edge. Because the clock signal contains spectral components only at the sampling frequency and its multiples, it is usually not a source of in band spurious tones. Overall, it is better to treat the clock as you would an analog signal and route it separately from the digital data input signals. The clock trace should be routed either over the analog ground plane or over its own section of the ground plane. The clock line needs to have accurately controlled impedance and should be well terminated near the LTC1668.

Printed Circuit Board Layout Considerations—Grounding, Bypassing and Output Signal Routing

The close proximity of high frequency digital data lines and high dynamic range, wide-band analog signals makes clean printed circuit board design and layout an absolute necessity. Figures 5 to 9 are the printed circuit board layers for an AC evaluation circuit for the LTC1668. Ground planes should be split between digital and analog sections as shown. All bypass capacitors should have minimum trace length and be ceramic 0.1μF or larger with low ESR. Bypass capacitors are required on VSS, VDD and REFOUT, and all connected to the AGND plane. The COMP2 pin ties to a node in the output current switching circuitry, and it requires a 0.1μF bypass capacitor. It should be bypassed to VSS along with COMP1. The AGND and DGND pins should both tie directly to the AGND plane, and the tie point between the AGND and DGND planes should nominally be near the DGND pin. LADCOM should either be tied directly to the AGND plane or be bypassed to AGND. The IOUT A and IOUT B traces should be close together, short, and well matched for good AC CMRR. The transformer output ground should be capable of optionally being isolated or being tied to the AGND plane, depending on which gives better performance in the system.

Suggested Evaluation Circuit

Figure 4 is the schematic and Figures 5 to 9 are the circuit board layouts for a suggested evaluation circuit, DC245A. The circuit can be programmed with component selection and jumpers for a variety of differentially coupled transformer output and differential and single-ended resistor loaded output configurations.
Figure 4. Suggested Evaluation Circuit
Figure 5. Suggested Evaluation Circuit Board—Silkscreen

Figure 6. Suggested Evaluation Circuit Board—Component Side
APPLICATIONS INFORMATION

Figure 7. Suggested Evaluation Circuit Board—GND Plane

Figure 8. Suggested Evaluation Circuit Board—Power Plane
Figure 9. Suggested Evaluation Circuit Board—Solder Side
Dimensions in millimeters (inches) unless otherwise noted.

G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)

NOTE: DIMENSIONS ARE IN MILLIMETERS
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH
SHALL NOT EXCEED 0.152mm (0.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD
FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE
**TYPICAL APPLICATION**

Figure 10. High Speed Buffered $V_{OUT}$ DAC

**RELATED PARTS**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC1406</td>
<td>8-Bit, 20Msps ADC</td>
<td>Undersampling Capability Up to 70MHz Input</td>
</tr>
<tr>
<td>LTC1414</td>
<td>14-Bit, 2.2Msps ADC</td>
<td>84dB SFDR at 1.1MHz $f_{IN}$</td>
</tr>
<tr>
<td>LTC1420</td>
<td>12-Bit, 10Msps ADC</td>
<td>72dB SINAD at 5MHz $f_{IN}$</td>
</tr>
<tr>
<td>LTC1604</td>
<td>16-Bit, 333ksps ADC</td>
<td>16-Bit, No Missing Codes, 90dB SINAD, –100dB THD</td>
</tr>
</tbody>
</table>