**FEATURES**

- Instrumentation Front End with 120dB CMRR
- Precise, Charge-Balanced Switching
- Operates from 3V to 18V
- Internal or External Clock
- Operates up to 5MHz Clock Rate
- Low Power
- Two Independent Sections with One Clock

**APPLICATIONS**

- Precision Instrumentation Amplifiers
- Ultra Precision Voltage Inverters, Multipliers and Dividers
- V–F and F–V Converters
- Sample-and-Hold
- Switched Capacitor Filters

**DESCRIPTION**

The LTC®-1043 is a monolithic, charge-balanced, dual switched capacitor instrumentation building block. A pair of switches alternately connects an external capacitor to an input voltage and then connects the charged capacitor across an output port. The internal switches have a break-before-make action. An internal clock is provided and its frequency can be adjusted with an external capacitor. The LTC1043 can also be driven with an external CMOS clock.

The LTC1043, when used with low clock frequencies, provides ultra precision DC functions without requiring precise external components. Such functions are differential voltage to single-ended conversion, voltage inversion, voltage multiplication and division by 2, 3, 4, 5, etc. The LTC1043 can also be used for precise V–F and F–V circuits without trimming, and it is also a building block for switched capacitor filters, oscillators and modulators.

The LTC1043 is manufactured using Linear Technology’s enhanced LTCMOS™ silicon gate process.

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**TYPICAL APPLICATION**

Instrumentation Amplifier

**CMRR vs Frequency**

COMMON MODE INPUT VOLTAGE INCLUDES THE SUPPLIES
LTC1043

**ABSOLUTE MAXIMUM RATINGS**

(Note 1)

Supply Voltage ........................................................ 18V

Input Voltage at Any Pin ........ –0.3V ≤ VIN ≤ V+ + 0.3V

Operating Temperature Range

LTC1043C ................................... –40°C ≤ TA ≤ 85°C

LTC1043M (OBSOLETE) .............–55°C ≤ TA ≤ 125°C

Storage Temperature Range .......... –65°C to 150°C

Lead Temperature (Soldering, 10 sec)............. 300°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

**ELECTRICAL CHARACTERISTICS**

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at TA = 25°C. V+ = 10V, V– = 0V, LTC1043M operates from –55°C ≤ TA ≤ 125°C; LTC1043C operates from –40°C ≤ TA ≤ 85°C, unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1043M</th>
<th>LTC1043C</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td>MIN</td>
</tr>
<tr>
<td>I5</td>
<td>Power Supply Current</td>
<td>Pin 16 Connected High or Low</td>
<td>0.25</td>
<td>0.4</td>
<td>0.7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>●</td>
<td></td>
<td></td>
<td>●</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C0SC</td>
<td>(Pin 16 to V–) = 100pF</td>
<td>0.4</td>
<td>0.65</td>
<td>1</td>
<td>0.4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>●</td>
<td></td>
<td></td>
<td>●</td>
</tr>
<tr>
<td>I1</td>
<td>OFF Leakage Current</td>
<td>Any Switch, Test Circuit 1 (Note 2)</td>
<td>6</td>
<td>100</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>●</td>
<td></td>
<td></td>
<td>●</td>
</tr>
<tr>
<td>RON</td>
<td>ON Resistance</td>
<td>Test Circuit 2, VIN = 7V, I = ±0.5mA</td>
<td>240</td>
<td>400</td>
<td>700</td>
</tr>
<tr>
<td></td>
<td></td>
<td>●</td>
<td></td>
<td></td>
<td>●</td>
</tr>
<tr>
<td>RON</td>
<td>ON Resistance</td>
<td>Test Circuit 2, VIN = 3.1V, I = ±0.5mA</td>
<td>400</td>
<td>700</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>●</td>
<td></td>
<td></td>
<td>●</td>
</tr>
<tr>
<td>fOSC</td>
<td>Internal Oscillator Frequency</td>
<td>C0SC (Pin 16 to V–) = 0pF</td>
<td>185</td>
<td>20</td>
<td>34</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C0SC (Pin 16 to V–) = 100pF</td>
<td>20</td>
<td>34</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>●</td>
<td></td>
<td></td>
<td>●</td>
</tr>
<tr>
<td>fOSC</td>
<td>Pin Source or Sink Current</td>
<td>Pin 16 at V+ or V–</td>
<td>40</td>
<td>70</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>●</td>
<td></td>
<td></td>
<td>●</td>
</tr>
<tr>
<td>I5</td>
<td>Break-Before-Make Time</td>
<td>25</td>
<td></td>
<td></td>
<td>25</td>
</tr>
<tr>
<td>I5</td>
<td>Clock to Switching Delay</td>
<td>C0SC Pin Externally Driven</td>
<td>75</td>
<td></td>
<td></td>
</tr>
<tr>
<td>fM</td>
<td>Max External CLK Frequency</td>
<td>C0SC Pin Externally Driven with CMOS Levels</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>V+ = 5V, V– = –5V, –5V &lt; VCM &lt; 5V</td>
<td>120</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(Note 1): Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

(Note 2): OFF leakage current is guaranteed but not tested at 25°C.
**TYPICAL PERFORMANCE CHARACTERISTICS**

(Tests Circuits 2 through 4)

*Power Supply Current vs Power Supply Voltage*

*Ron vs Vin*

*Ron (Peak) vs Power Supply Voltage and Temperature*

*Oscillator Frequency, fosc vs Cosc*

*Oscillator Frequency, fosc vs Supply Voltage*

*Normalized Oscillator Frequency, fosc vs Supply Voltage*
**TYPICAL PERFORMANCE CHARACTERISTICS** (Test Circuits 2 through 4)

**Oscillator Frequency, \( f_{OSC} \) vs Ambient Temperature, \( T_A \)**

- \( f_{OSC} \) vs \( T_A \) for different supply voltages:
  - \( V^+ = 10V, V^- = 0V \)
  - \( V^+ = 5V, V^- = 0V \)
  - \( V^+ = 15V, V^- = 0V \)

**C\( \text{OSC} \) Pin ISINK, ISOURCE vs Supply Voltage**

- \( I_{SINK} \) and \( I_{SOURCE} \) for different temperature limits:
  - \( I_{SINK}, T_A = -55^\circ C \)
  - \( I_{SOURCE}, T_A = 25^\circ C \)
  - \( I_{SOURCE}, T_A = 125^\circ C \)

**Break-Before-Make Time, \( t_{NOV} \), vs Supply Voltage**

- \( t_{NOV} \) for different supply voltages:
  - \( T_A = 25^\circ C \)

**BLOCK DIAGRAM**

THE SWITCHES ARE TIMED AS SHOWN WITH PIN 16 HIGH.

THE CHARGE BALANCING CIRCUITRY SAMPLES THE VOLTAGE AT S3 WITH RESPECT TO S4 (PIN 16 HIGH) AND INJECTS A SMALL CHARGE AT THE C\(^+ \) PIN (PIN 16 LOW). THIS BOOSTS THE CMRR WHEN THE LTC1043 IS USED AS AN INSTRUMENTATION AMPLIFIER FRONT END.

FOR MINIMUM CHARGE INJECTION IN OTHER TYPES OF APPLICATIONS, S3A AND S3B SHOULD BE GROUNDED.
TEST CIRCUITS

Test Circuit 1. Leakage Current Test

Test Circuit 2. RON Test

Test Circuit 3. Oscillator Frequency, f_{OSC}

Test Circuit 4. CMRR Test

APPLICATIONS INFORMATION

Common Mode Rejection Ratio (CMRR)

The LTC1043, when used as a differential to single-ended converter rejects common mode signals and preserves differential voltages (Figure 1). Unlike other techniques, the LTC1043’s CMRR does not degrade with increasing common mode voltage frequency. During the sampling mode, the impedance of Pins 2, 3 (and 11, 12) should be reasonably balanced, otherwise, common mode signals will appear differentially. The value of the CMRR depends on the value of the sampling and holding capacitors (C_S, C_H) and on the sampling frequency. Since the common mode voltages are not sampled, the common mode signal frequency can well exceed the sampling frequency without experiencing aliasing phenomena. The CMRR of Figure 1 is measured by...
shorting Pins 7 and 13 and by observing, with a precision DVM, the change of the voltage across CH with respect to an input CM voltage variation. During the sampling and holding mode, charges are being transferred and minute voltage transients will appear across the holding capacitor. Although the RON on the switches is low enough to allow fast settling, as the sampling frequency increases, the rate of charge transfer increases and the average voltage measured with a DVM across it will increase proportionally; this causes the CMRR of the sampled data system, as seen by a “continuous” instrument (DVM), to decrease (Figure 2).

**Switch Charge Injection**

Figure 3 shows one out of the eight switches of the LTC1043, configured as a basic sample-and-hold circuit. When the switch opens, a “hold step” is observed and its magnitude depends on the value of the input voltage. Figure 4 shows charge injected into the hold capacitor. For instance, a 2pCb of charge injected into a 0.01μF capacitor causes a 200μV hold step. As shown in Figure 4, there is a predictable and repeatable charge injection cancellation when the input voltage is close to half the supply voltage of the LTC1043. This is a unique feature of this product, containing charge-balanced switches fabricated with a self-aligning gate CMOS process. Any switch of the LTC1043, when powered with symmetrical dual supplies, will sample-and-hold small signals around ground without any significant error.

**Shielding the Sampling Capacitor for Very High CMRR**

Internal or external parasitic capacitors from the C+ pin(s) to ground affect the CMRR of the LTC1043 (Figure 1). The common mode error due to the internal junction capacitances of the C+Pin(s) 2 and 11 is cancelled through internal circuitry. The C+ pin, therefore, should be used as the top plate of the sampling capacitor. The interpin capacitance between pin 2 and dummy Pin 1 (11 and 10) appears in parallel with the sampling capacitor so it does not degrade the CMRR. A shield placed underneath the sampling capacitor and connected to either Pin 1 or 3 helps to boost the CMRR in excess of 120dB (Figure 5).

Excessive external parasitic capacitance between the C– pins and ground indirectly degrades CMRR; this becomes visible especially when the LTC1043 is used with clock frequencies above 2kHz. Because of this, if a shield is used, the parasitic capacitance between the shield and circuit ground should be minimized.

It is recommended that the outer plate of the sampling capacitor be connected to the C– pin(s).

**Input Pins, SCR Sensitivity**

An internal 60Ω resistor is connected in series with the input of the switches (Pins 5, 6, 7, 8, 13, 14, 15, 18) and it is included in the RON specification. When the input voltage exceeds the power supply by a diode drop, current will flow into the input pin(s). The LTC1043 will not latch until the input current reaches 2mA–3mA. The device will...
recover from the latch mode when the input drops 3V to 4V below the voltage value which caused the latch. For instance, if an external resistor of 200Ω is connected in series with an input pin, the input can be taken 1.3V above the supply without latching the IC. The same applies for the C+ and C− pins.

C_{Osc} Pin (16), Figure 6
The C_{Osc} pin can be used with an external capacitor, C_{Osc}, connected from Pin 16 to Pin 17, to modify the internal oscillator frequency. If Pin 16 is floating, the internal 24pF capacitor, plus any external interpin capacitance, set the oscillator frequency around 190kHz with ±5V supply. The typical performance characteristics curves provide the necessary information to set the oscillator frequency for various power supply ranges. Pin 16 can also be driven with an external clock to override the internal oscillator. Although standard 7400 series CMOS gates do not guarantee CMOS levels with the current source and sink requirements of Pin 16, they will in reality drive the C_{Osc} pin. CMOS gates conforming to standard B series output drive have the appropriate voltage levels and more than enough output current to simultaneously drive several LTC1043 C_{Osc} pins. The typical trip levels of the Schmitt trigger (Figure 6) are given below.

<table>
<thead>
<tr>
<th>SUPPLY</th>
<th>TRIP LEVELS</th>
</tr>
</thead>
<tbody>
<tr>
<td>V^+ = 5V, V^- = 0V</td>
<td>V_H = 3.4V, V_L = 1.35V</td>
</tr>
<tr>
<td>V^+ = 10V, V^- = 0V</td>
<td>V_H = 6.5V, V_L = 2.8V</td>
</tr>
<tr>
<td>V^+ = 15V, V^- = 0V</td>
<td>V_H = 9.5V, V_L = 4.1V</td>
</tr>
</tbody>
</table>

Figure 4. Individual Switch Charge Injection vs Input Voltage

Figure 5. Printed Circuit Board Layout Showing Shielding the Sampling Capacitor

Figure 6. Internal Oscillator
Divide by 2

\[ V_{OUT} = V_{IN}/2 \pm 1\text{ppm} \]

\[ 0 \leq V_{IN} = V^+ \]

\[ 3 \leq V^+ = 18V \]

Multiply by 2

\[ V_{OUT} = 2V_{IN} \pm 5\text{ppm} \]

\[ 0 \leq V_{IN} = V^+/2 \]

\[ 3 \leq V^+ = 18V \]

Ultra Precision Voltage Inverter

\[ V_{OUT} = -V_{IN} \pm 20\text{ppm} \]

\[ V^+ = +5V, V^- = -5V \]

Precision Multiply by 3

\[ V_{OUT} = 3V_{IN} \pm 10\text{ppm} \]

\[ 0 < V_{IN} < V^+/3 \]

\[ 3V < V^+ < 18V \]

Precision Multiply by 4

\[ V_{OUT} = 4V_{IN} \pm 40\text{ppm} \]

\[ 0 < V_{IN} < V^+/4 \]

\[ 3V < V^+ < 18V \]

Divide by 3

\[ V_{OUT} = V_{IN}/3 \pm 3\text{ppm} \]

\[ 0 \leq V_{IN} = V^+ \]

\[ 3V < V^+ < 18V \]
TYPICAL APPLICATIONS

Divide by 4

0 = \( V_{IN} = V' \)

\( V_{OUT} = V_{IN}/4 \pm 5ppm \)

0.005% V/F Converter

0.01% Analog Multiplier

0.01 \( \mu F \)

0 \( \leq \) \( V_{IN} \) \( \leq \) \( V^+ \)

\( V_{OUT} = V_{IN}/4 \pm 0.01\% \)

1k

0.01 \( \mu F \)

22k

330k

5V

5V

–5V

–5V

–5V

–5V

0.01 \( \mu F \)

20k

80.6k*

20k

80.6k*

0.001 \( \mu F \)

XINPUT

OPERATE LTC1043 FROM ±5V

† POLYSTYRENE, MOUNT CLOSE

†† 1% FILM RESISTOR

ADJUST OUTPUT TRIM

SO X • Y = OUTPUT ± 0.01%

††† TYPICAL APPLICATIONS
**LTC1043**

**TYPICAL APPLICATIONS**

**Single 5V Supply, Ultra Precision Instrumentation Amplifier**

![Circuit Diagram]

- **Input Voltage:** ±5V
- **Output Voltage:** ±5V
- **Bias Current:** 1nA
- **Open Loop Gain:** > 10^8
- **CMRR:** 140dB
- **Drift:** 0.1µV/°C
- **Input Offset:** 10µV

**Voltage Controlled Current Source with Ground Referred Input and Output**

![Circuit Diagram]

- **Input Voltage:** 0V to 2V
- **Output Voltage:** 0V to 2V
- **Bias Current:** 1nA
- **Gain:** \( \frac{R_2}{R_1} + 1 \)

**Precision Instrumentation Amplifier**

![Circuit Diagram]

- **Input Voltage:** ±5V
- **Output Voltage:** ±5V
- **Gain:** \( \frac{R_2}{R_1} + 1 \)
- **Bias Current:** 1nA
- **CMRR:** 140dB
- **Drift:** 0.1µV/°C
- **Input Offset:** 10µV

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**1043fa**
Lock-In Amplifier (= Extremely Narrow-Band Amplifier)

THERMISTOR BRIDGE IS THE SIGNAL SOURCE

SYNONOMOUS DEMODULATOR

5V

10k*

10k*

5V

100k

47µF

0.01µF

50Hz SINE DRIVE

T1 = TFSSX17ZZ, TOROTEL
R_T = Y30 THERMISTOR 44006
≈ 6.19k AT 37.5°C

MATCH 0.05%

6.19k = VISHAY S-102

OPERATE LTC1043 WITH ±5V SUPPLIES

LOCK-IN AMPLIFIER TECHNIQUE USED TO EXTRACT VERY SMALL SIGNALS BURIED INTO NOISE

ZERO CROSSING DETECTOR

50MHz Termal RMS/DC Converter

300mV

10VRMS INPUT

2% ACCURACY DC 50MHz

100:1 CREST FACTOR CAPABILITY

T1 TO T2 = YELLOW SPRINGS INST. CO.

THERMISITOR COMPOSITE

ENCLOSE T1 AND T2 IN STYROFOAM

*1% RESISTOR

TYPICAL APPLICATIONS
Quad Single 5V Supply, Low Hold Step, Sample-and-Hold

Single Supply Precision Linearized Platinum RTD Signal Conditioner

LTC1043
TYPICAL APPLICATIONS

1/4 LT1014
V_{IN}
NC

1/4 LT1014
V_{IN}
NC

1/4 LT1014
V_{IN}
NC

1/4 LT1014
V_{IN}
NC

LTC1043

Vin
Cl
0.01 \mu F

Vin
Cl
0.01 \mu F

Vin
Cl
0.01 \mu F

Vin
Cl
0.01 \mu F

HOLD

SAMPLE

0V TO 4V = 0°C TO 400°C

±0.05°C

R_p = ROSEMOUNT 118MFRTD

*1% FILM RESISTOR

TRIM SEQUENCE:
SET SENSOR TO 0°C VALUE. ADJUST ZERO FOR 0V OUT
SET SENSOR TO 100°C VALUE. ADJUST GAIN FOR 1,000V OUT
SET SENSOR TO 400°C VALUE. ADJUST LINEARITY FOR 4,000V OUT
REPEAT AS REQUIRED

LT1014
2.5V
2.74k*

10k*

2.4k

50k

250k*

(LINEARITY CORRECTION LOOP)
**TYPICAL APPLICATIONS**

### 0.005% F/V Converter

![Diagram of 0.005% F/V Converter]

### High Frequency Clock Tunable Bandpass Filter

![Diagram of High Frequency Clock Tunable Bandpass Filter]

**BANDPASS CENTER FREQUENCY** $f_0 = \frac{f_{CLK}}{3\pi \sqrt{\frac{R2}{RT}}}$

- $f_0$ MAX = 100kHz
- $Q_{MAX}$ AT 100kHz $f_0$ IS x10
- $(f_0 \cdot Q)_{MAX} = 1$MHz
- $f_{CLK} MAX = 3$MHz, $Q < 2$
TYPICAL APPLICATIONS

Frequency-Controlled Gain Amplifier

Relative Humidity Sensor Signal Conditioner

* = 1% FILM RESISTOR

SENSOR = PANAMETRICS # RHS
= 500pF AT RH = 76%
1.7 pF/%RH

1/4 LTC1043

GAIN CONTROL
0kHz TO 10kHz = GAIN 0 TO 1000

FOR DIFFERENTIAL INPUT, GROUND PIN 8A AND USE PINS 13A AND 7A FOR INPUTS
GAIN = \( f_{\text{in}} \times 0.01 \mu F \); GAIN IS NEGATIVE AS SHOWN

FOR SINGLE-ENDED INPUT AND POSITIVE GAIN, GROUND PIN 8A AND USE PIN 7A FOR INPUT
USE ±5V SUPPLIES FOR LTC1043
TYPICAL APPLICATIONS

Linear Variable Differential Transformer (LVDT), Signal Conditioner

Precision Current Sensing in Supply Rails
**PACKAGE DESCRIPTION**

**D Package**
18-Lead Side Brazed (Hermetic)
(Reference LTC DWG # 05-08-1210)

**N Package**
18-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)

**SW Package**
18-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)

**OBSOLETE PACKAGE**

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**NOTE:**
1. DIMENSIONS ARE IN INCHES

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**NOTE:**
1. DIMENSIONS ARE IN MILLIMETERS

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**Lin**

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