Ordering number: EN 5551

CMOS LSI

LC864164B/56B/48B/40B

8-bit Single Chip Microcontroller

Overview

The LC864164B/56B/48B/40B microcontrollers are 8-bit single chip microcontrollers with the following on-chip functional blocks:

- CPU : Operable at a minimum bus cycle time of 0.5 µs
- On-chip ROM maximum capacity : 64 K bytes
- On-chip RAM capacity : 384 bytes
- CRT display RAM : 640 × 9 bits
- Closed-caption TV controller and the on-screen display controller
- 16-bit timer/counter
- 4 channel × 4-bit A/D Converter
- 8-bit synchronous serial-interface circuit
- Closed-caption data slicer
- 12-source 10-vectored interrupt system

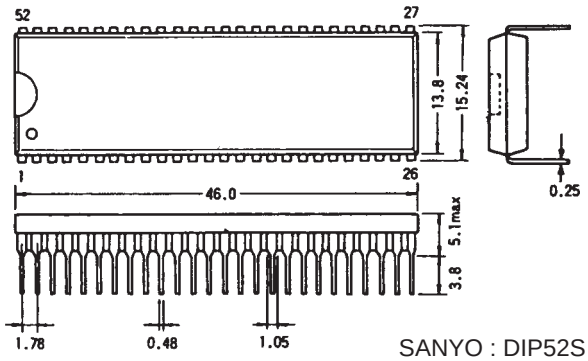
All of the above functions are fabricated on a single chip.

Package Dimensions

unit : mm

3128-DIP52S

[LC864164B/56B/48B/40B]



SANYO : DIP52S

Features

(1) Read-only memory (ROM) :

LC864164B	65280 × 8 bits
LC864156B	57344 × 8 bits
LC864148B	49152 × 8 bits
LC864140B	40960 × 8 bits

(2) Random access memory (RAM) : 384 × 8 bits
640 × 9 bits (for CRT display)

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

(3) OSD functions
- Screen for display : 34 columns × 16 rows (at standard character size)
- Display for RAM : 640 × 9 bits (6 columns for control + 34 columns for display) × 16 rows × 9 bits
- 252 kinds of user specified characters
  125 kinds 9 × 9 dots
  127 kinds 12 × 18 dots
- Various character attributes
  Character colors : 16 colors
  Character background colors : 16 colors
  Fringe / shadow colors : 16 colors
  Full screen colors : 16 colors
  Fringe / shadow
  Rounding
  Underline
  Italic character (slanting)
- Close-character attribute data changing available
- Vertical display start line setting available (Row overlapping available)
- Horizontal display start position setting available
- Display mode specification by row (Display mode mixable)
  captio mode / text mode / OSD mode
- Eight kinds of characters size
  Horiz × Vert. = (1 × 1), (1 × 2), (2 × 2), (2 × 4)
  (1.5 × 1), (1.5 × 2), (3 × 2), (3 × 4)
- Shuttering and scrolling in row unit available
- Horizontal character pitch selectable : 9 to 16 dots
- Polarity of $\overline{R}$, $\overline{G}$, $\overline{B}$, I, BL output programmable
- Polarity of $\overline{HS}$, $\overline{VS}$ input programmable

(4) Bus cycle time / Instruction-cycle time
The LC864164A/56A/48A/40A microcontrollers are designed to read the ROM twice within one instruction cycle. It has about 1.7 times performance capability within the same instruction-cycle compared to our 4-bit microcontrollers (LC66000 series).
The bus cycle time indicates the speed to read ROM.

Bus cycle time	Instruction cycle time	System clock oscillation	Oscillation frequency	Voltage
0.5 μs	1.0 μs	Ceramic (CR)	12 MHz	4.5 V to 5.5 V
7.5 μs	15.0 μs	Internal RC	800 kHz	4.5 V to 5.5 V

(5) Ports
- Input/output port : 2 ports (16 lines)
  Input/output port programmable in nibble unit : 1 port (8 lines)
(When the N-channel open drain output is selected, the data in a bit can be inputted.)
Input/output port programmable in a bit : 1 port (8 lines)
- Input port : 2 ports (8 lines)

(6) A/D converter
- 4-channel × 4-bit A/D converter (converted with program)

(7) PWM output
- 10-channel × 7-bit PWM

(8) Timer
- Timer 0 : 16-bit timer / counter
  2-bit prescaler + 8-bit built-in programmable prescaler
  - Mode 0 : Two 8-bit timers with a programmable prescaler
  - Mode 1 : 8-bit timer with a programmable prescaler + 8-bit counter
  - Mode 2 : 16-bit timer with a programmable prescaler
  - Mode 3 : 16-bit counter

  The resolution of timer is 1 tCYC.
- Timer 1 : 16-bit timer / PWM
  - Mode 0 : Two 8-bit timers
  - Mode 1 : 8-bit timer + 8-bit PWM
  - Mode 2 : 16-bit timer
  - Mode 3 : Variable-bit PWM (9 to 16 bits)

  In Mode 0 and Mode 1, the resolution of Timer and PWM is tCYC.
  In Mode 2 and Mode 3, the resolution of Timer and PWM selectable : tCYC or 1/2tCYC by program.

(9) Remote control receiver circuit (shares with the P73/INT3/T0IN terminal)
- Noise rejection function
- Polarity switching

(10) Watchdog timer
External RC circuit is required
Interrupt or system reset is selectable

(11) Interrupts
- 12-source 10-vectored interrupts
  1. External interrupt INT0
  2. External interrupt INT1
  3. External interrupt INT2, Timer/counter T0L (Lower 8 bits)
  4. External interrupt INT3
  5. Timer/counter T0H (Upper 8 bits)
  6. Timer T1H, T1L
  7. Serial interface 0 (SIO0)
  8. Data slicer
  9. Vertical synchronous signal interrupt ($\overline{VS}$)
  10. Port 0

- Interrupt priority control available

  Three interrupt priorities are supported (low, high and the highest) and multilevel nesting is possible. Low or high priority can be assigned to the interrupt from 3 to 10 listed above. For the external interrupt INT0 and INT1, high or the highest priority can be set.

(12) Sub-routine stack level
- A maximum of 128 levels (Sets the stack inside a RAM.)

(13) Multiplication/division instruction
- 16 bits × 8 bits (7 instruction cycle times)
- 16 bits / 8 bits (7 instruction cycle times)

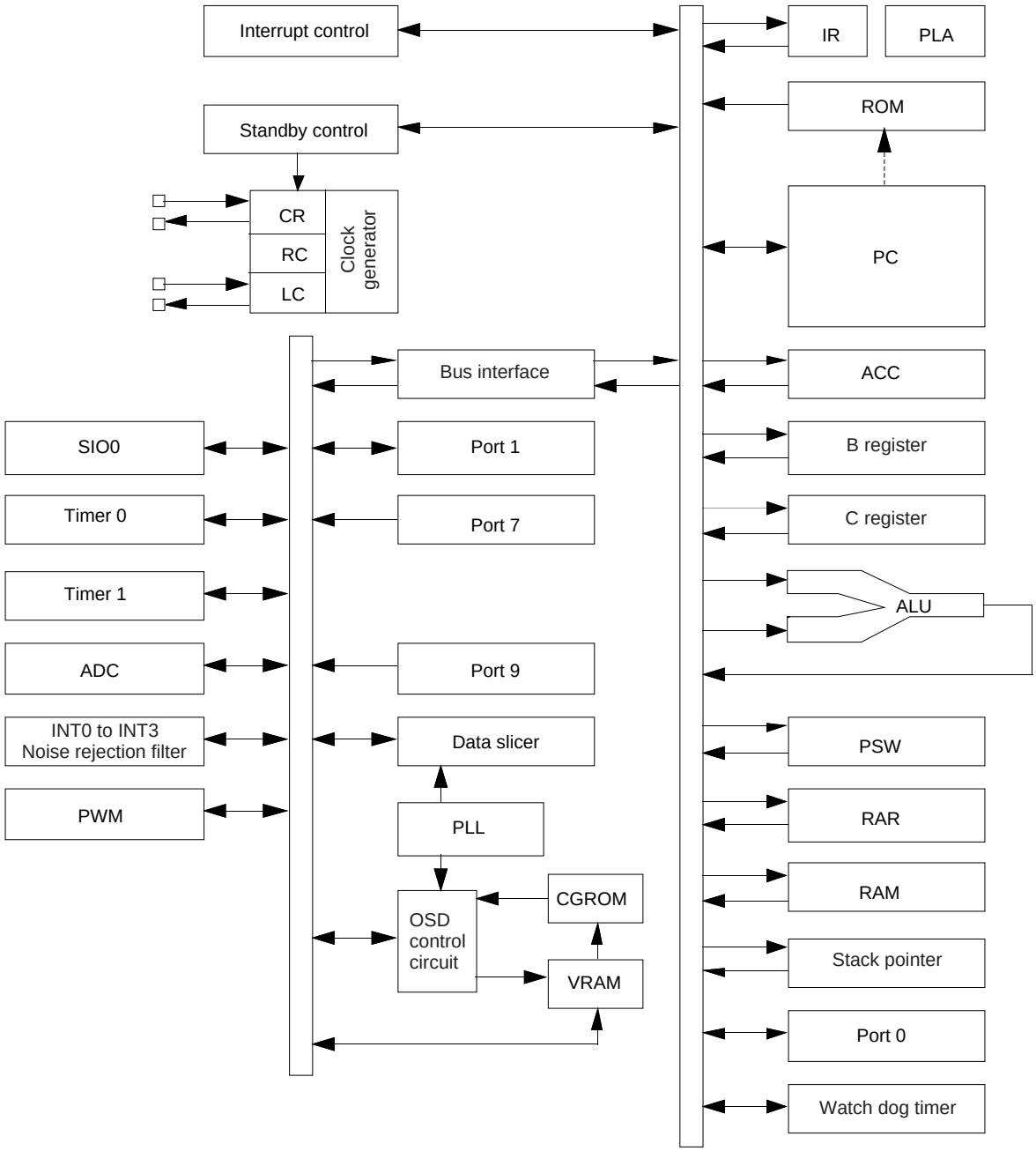
(14) 3 oscillation circuits
- On-chip RC oscillation circuit for the system clock
- On-chip CP oscillation circuit for the system clock
- On-chip LC oscillation circuit for the CRT synchronization

(15) Standby function
- HALT mode function
  The HALT mode is used to reduce the power dissipation. In this operation mode, the program execution is stopped. This mode can be released by the interrupt request signals or the system reset.
- HOLD mode
  The HOLD mode is used to stop oscillations ; the RC (internal) and the ceramic oscillations. This mode can be released by the following conditions.
  • Pull the reset terminal ($\overline{\text{RES}}$) to low level.
  • Feed the selected level to either P70/INT0 or P71/INT1.
  • Feed the Port 0 interrupt condition.

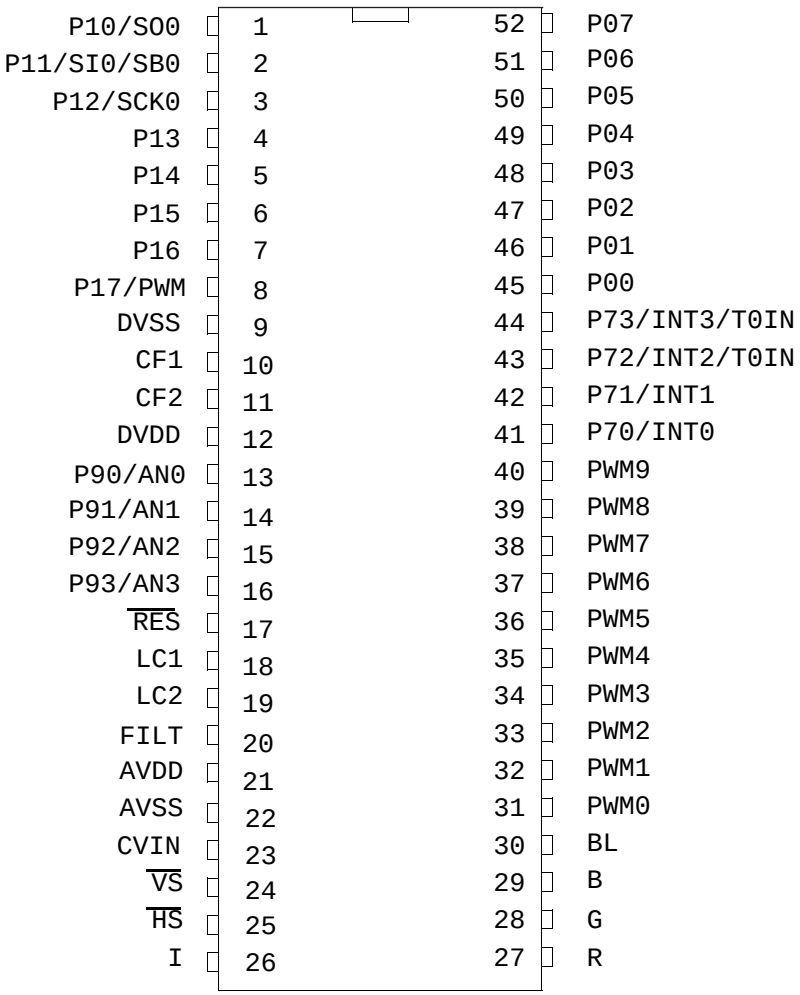
(16) Factory shipment
DIP52S

(17) Development Tool
- Evaluation chip : LC866098
- EPROM with a window : LC86E4164
- One time : LC86P4164
- Emulator : EVA86000 (Main) + ECB864100 (Evaluation board) + POD864100 (Pod)

System Block Diagram



Pin Assignment



Top view

Pin Description

• Port option can be specified in bit units except the pull-up resistor selection of port 0.

<table>
<tr><th>Pin name</th><th>Pin No.</th><th>I/O</th><th>Function description</th><th>Option</th></tr>
<tr><td>DVSS</td><td>9</td><td>—</td><td>Negative power supply for digital circuit</td><td></td></tr>
<tr><td>CF1</td><td>10</td><td>Input</td><td>Input terminal for ceramic resonator</td><td></td></tr>
<tr><td>CF2</td><td>11</td><td>Output</td><td>Output terminal for ceramic resonator</td><td></td></tr>
<tr><td>DVDD</td><td>12</td><td>—</td><td>Positive power supply for digital circuit</td><td></td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>17</td><td>Input</td><td>Reset terminal</td><td></td></tr>
<tr><td>LC1</td><td>18</td><td>Input</td><td>LC oscillation circuit input terminal</td><td></td></tr>
<tr><td>LC2</td><td>19</td><td>Output</td><td>LC oscillation circuit output terminal</td><td></td></tr>
<tr><td>FILT</td><td>20</td><td>Output</td><td>Filter terminal for PLL</td><td></td></tr>
<tr><td>AVDD</td><td>21</td><td>—</td><td>Positive power supply for analog circuit</td><td></td></tr>
<tr><td>AVSS</td><td>22</td><td>—</td><td>Negative power supply for analog circuit</td><td></td></tr>
<tr><td>CVIN</td><td>23</td><td>Input</td><td>Video signal input terminal</td><td></td></tr>
<tr><td>$\overline{\text{VS}}$</td><td>24</td><td>Input</td><td>Vertical synchronization signal input terminal</td><td></td></tr>
<tr><td>$\overline{\text{HS}}$</td><td>25</td><td>Input</td><td>Horizontal synchronization signal input terminal</td><td></td></tr>
<tr><td>I</td><td>26</td><td>Output</td><td>Image intensity output</td><td></td></tr>
<tr><td>R</td><td>27</td><td>Output</td><td>Red (R) output terminal of RGB image output</td><td></td></tr>
<tr><td>G</td><td>28</td><td>Output</td><td>Green (G) output terminal of RGB image output</td><td></td></tr>
<tr><td>B</td><td>29</td><td>Output</td><td>Blue (B) output terminal of RGB image output</td><td></td></tr>
<tr><td>BL</td><td>30</td><td>Ouptut</td><td>Fast blanking control signal
Switch TV image signal and caption/OSD image signal</td><td></td></tr>
<tr><td>PWM0
to PWM9</td><td>31 to 40</td><td>Output</td><td>PWM0 to 9 output terminals
15 V withstand</td><td></td></tr>
<tr><td>Port 0
P00 to P07</td><td>45 to 52</td><td>I/O</td><td>8-bit Input/output port
Input/output can be specified in nibble units
HOLD release input
Interrupt input</td><td>Pull-up resistor
Provided/not provided
(in bit units)
Output Format
CMOS/Nch-OD
(in bit units)</td></tr>
<tr><td>Port 1
P10 to P17</td><td>1to 8</td><td>I/O</td><td>8-bit Input/output port
Input/output can be specified in bit units
Other function
<table>
<tr><td>P10</td><td>SIO0 data output</td></tr>
<tr><td>P11</td><td>SIO0 data input / bus input/output</td></tr>
<tr><td>P12</td><td>SIO0 clock input/output</td></tr>
<tr><td>P17</td><td>Timer 1 (PWM) output</td></tr>
</table></td><td>Output Format
CMOS/Nch-OD
(in bit units)</td></tr>
<tr><td>Port 7
P70
P71 to P73</td><td>41
42 to 44</td><td>I/O
Input</td><td>4-bit input port
Other function
<table>
<tr><td>P70</td><td>INT0 input/HOLD release input/
Nch-transistor output for watchdog timer</td></tr>
<tr><td>P71</td><td>INT1 input/HOLD release input</td></tr>
<tr><td>P72</td><td>INT2 input/timer 0 event input</td></tr>
<tr><td>P73</td><td>INT3 input (noise rejection filter attached input/
timer 0 event input)</td></tr>
</table>
Interrupt receiver format vector address
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/Falling</th><th>H level</th><th>L level</th><th>Vector</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr>
</table></td><td>Pull-up resistor
provided/ not provided
(in bit units)</td></tr>
</table>

Continued on next page.

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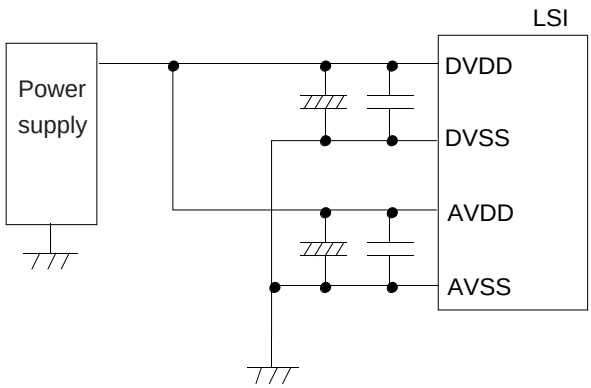
Pin name	Pin No.	I/O	Function description	Option
Port 9 P90 to P93	13 to 16	Input	4-bit input port Other functions A/D converter input port (4 lines)	

- Any port option can be selected in bit units.
- Port 0 portion : Pull-up resistor is provided when CMOS output is selected.
  The pull-up resister is not provided when N-ch Open Drain is selected.
- Port 1 option: Programmable pull-up resister is provided when any output form is selected.

- Port status during reset

Terminal	I/O	Pull-up resistor status at selecting pull-up option
Port 0	Input	Pull-up resistor OFF, ON after reset release
Port 1	Input	Programmable pull-up resistor OFF
Port 7	Input	Fixed pull-up resistor provided

* AVDD and AVSS are the power supply terminals for built-in analog circuit while DVDD and DVSS are the power supply terminals for built-in digital circuit. Connect them like the following figure to reduce the mutual noise influence.



Specifications

1. Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter		Symbol	Pins	Conditions		Ratings			Unit
					V_{DD} [V]	min	typ	max	
Supply voltage		V_{DD}max	DVDD, AVDD	DVDD = AVDD		–0.3		7.0	V
Input voltage		V_I(1)	• P71, 72, 73 • Port 9 • $\overline{RES}$, HS, $\overline{VS}$, CVIN			–0.3		V_{DD}+0.3	
Output voltage		V_O(1)	R, G, B, BL, I, FILT			–0.3		V_{DD}+0.3	
		V_O(2)	PWM0 to PWM9			–0.3		15	
Input/output voltage		V_{IO}(1)	Ports 0, 1, P70			–0.3		V_{DD}+0.3	
High-level output current	Peak output current	I_{OPH}(1)	Ports 0, 1	• Pull-up MOS Transistor output • At each pin		–2			mA
		I_{OPH}(2)	Ports 0, 1	• CMOS output • At each pin		–4			
		I_{OPH}(3)	R, G, B, BL, I	• CMOS output • At each pin		–5			
	Total output current	$\sum I_{OAH}$(1)	Port 1	The total of all pins		–10			
		$\sum I_{OAH}$(2)	Port 0	The total of all pins		–10			
		$\sum I_{OAH}$(3)	R, G, B, BL, I	The total of all pins		–15			
Low-level output current	Peak output current	I_{OPL}(1)	Ports 0, 1	At each pin				20	
		I_{OPL}(2)	P70	At each pin				30	
		I_{OPL}(3)	• R, G, B, BL, I • PWM0 to PWM9	At each pin				5	
	Total output current	$\sum I_{OAL}$(1)	Port 0	The total of all pins				40	
		$\sum I_{OAL}$(2)	Port 1, P70	The total of all pins				40	
		$\sum I_{OAL}$(3)	R, G, B, BL, I	The total of all pins				15	
		$\sum I_{OAL}$(4)	PWM0 to PWM9	The total of all pins				30	
Maximum power dissipation		Pd max	DIP52S	Ta = –30 to +70°C				430	mW
Operating temperature range		Topr				–30		+70	°C
Storage temperature range		Tstg				–55		+150	

*DVSS and AVSS must be supplied the same voltage, V_{SS}. V_{SS} = DVSS = AVSS
DVDD and AVDD must be supplied the same voltage, V_{DD}. V_{DD} = DVDD = AVDD

2. Recommended Operating Range at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions		Ratings			Unit
				V_{DD} [V]	min	typ	max	
Operating supply voltage range	V_{DD}	DVDD, AVDD	0.98 µs ≤ tCYC tCYC ≤ 1.02 µs		4.5		5.5	V
Hold voltage	V_{HD}	DVDD, AVDD	RAMs and the registers hold data at HOLD mode.		2.0		5.5	
Input high-level voltage	V_{IH}(1)	Port 0 (Schmitt)	Output disable	4.5 to 5.5	0.6V_{DD}		V_{DD}	
	V_{IH}(2)	• Port 1 (Schmitt) • P72,73 • $\overline{HS}$,$\overline{VS}$	Output disable	4.5 to 5.5	0.75V_{DD}		V_{DD}	
	V_{IH}(3)	• P70 port input / interrupt • P71 • $\overline{RES}$ (Schmitt)	Output N-channel transistor OFF	4.5 to 5.5	0.75V_{DD}		V_{DD}	
	V_{IH}(4)	P70 Watchdog timer input	Output N-channel transistor OFF	4.5 to 5.5	V_{DD}-0.5		V_{DD}	
	V_{IH}(5)	Port 9 port input		4.5 to 5.5	0.7V_{DD}		V_{DD}	
Input low-level voltage	V_{IL}(1)	Port 0 (Schmitt)	Output disable	4.5 to 5.5	V_{SS}		0.2V_{DD}	
	V_{IL}(2)	• Port 1 (Schmitt) • P72,73 • $\overline{HS}$,$\overline{VS}$ • Port 9	Output disable	4.5 to 5.5	V_{SS}		0.25V_{DD}	
	V_{IL}(3)	• P70 port input / interrupt • P71 • $\overline{RES}$ (Schmitt)	N-channel transistor OFF	4.5 to 5.5	V_{SS}		0.25V_{DD}	
	V_{IL}(4)	P70 Watchdog timer input	N-channel transistor OFF	4.5 to 5.5	V_{SS}		0.6V_{DD}	
	V_{IL}(5)	Port 9 port input		4.5 to 5.5	V_{SS}		0.3V_{DD}	
CVIN input amplitude	V_{CVIN}	CVIN		5.0	1Vp-p –3dB	1Vp-p	1Vp-p +3dB	Vp-p *
Operation cycle time	tCYC(1)		OSD function	4.5 to 5.5	0.98	1	1.02	µs
	tCYC(2)		Except OSD function	4.5 to 5.5	0.98		30	

* Vp-p : Peak-to-peak voltage

Parameter	Symbol	Pins	Conditions		Ratings			Unit
				V_{DD} [V]	min	typ	max	
Oscillation frequency range (Note 1)	FmCF	CF1, CF2	12 MHz (ceramic resonator oscillation) Refer to Figure 1.	4.5 to 5.5	11.76	12	12.24	MHz
	FmLC	LC1, LC2	14.11 MHz (LC oscillation) Refer to Figure 2.	4.5 to 5.5		14.11		
	FmRC		RC oscillation	4.5 to 5.5	0.4	1.5	3.0	
Oscillation stable time period (Note 2)	tmsCF	CF1, CF2	12 MHz (ceramic resonator oscillation) Refer to Figure 3.	4.5 to 5.5		0.02	0.2	ms

(Note 1) The oscillation constant is shown on Table 1 and Table 2.

(Note 2) The oscillation stable time period is the time necessary for the oscillation to become stable after the following conditions.

1. Supplying voltage.
2. Release the HOLD mode.
3. Release stopping the main-clock oscillation.

Refer to Page 3 for details.

3. Electrical Characteristics at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions		Ratings			Unit
				V_{DD} [V]	min	typ	max	
Input high-level current	I_{IH}(1)	• Port 1 • Port 0 without pull-up MOS transistor	• Output disable • Pull-up MOS transistor OFF • $V_{IN} = V_{DD}$ (including the off-leak current of the output transistor)	4.5 to 5.5			1	µA
	I_{IH}(2)	• Port 7 without pull-up MOS transistor • Port 9 • $\overline{RES}$ • HS, VS	$V_{IN} = V_{DD}$	4.5 to 5.5			1	
Input low-level current	I_{IL}(1)	• Port 1 • Port 0 without pull-up MOS transistor	• Output disable • Pull-up MOS transistor OFF • $V_{IN} = V_{SS}$ (including the off-leak current of the output transistor)	4.5 to 5.5	–1			
	I_{IL}(2)	• Port 7 without pull-up MOS transistor • Port 9	$V_{IN} = V_{SS}$	4.5 to 5.5	–1			
	I_{IL}(3)	• $\overline{RES}$ • HS, VS	$V_{IN} = V_{SS}$	4.5 to 5.5	–1			
Output high-level voltage	V_{OH}(1)	CMOS output of ports 0, 1	I_{OH} = –1.0 mA	4.5 to 5.5	V_{DD}–1			V
	V_{OH}(2)	R, G, B, BL, I	I_{OH} = –0.1 mA	4.5 to 5.5	V_{DD}–0.5			
Output low-level voltage	V_{OL}(1)	Ports 0, 1	I_{OL} = 10 mA	4.5 to 5.5			1.5	
	V_{OL}(2)	Ports 0, 1	• I_{OL} = 1.6 mA • The total current of the ports 0,1 is not over 40 mA.	4.5 to 5.5			0.4	
	V_{OL}(3)	• R, G, B, BL, I • PWM0 to PWM9	• I_{OL} = 3.0 mA • The current of any unmeasured pin is not over 3 mA.	4.5 to 5.5			0.4	
	V_{OL}(4)	P70	I_{OL} = 1 mA	4.5 to 5.5			0.4	
Pull-up MOS transistor resistance	Rpu	• Ports 0, 1 • Port 7	$V_{OH} = 0.9V_{DD}$	4.5 to 5.5	13	38	80	kΩ
Output off-leakage current	I_{OFF}	PWM0 to PWM9	V_{OUT} = 13.5V	4.5 to 5.5			5	µA
Hysteresis voltage	V_{HIS}	• Ports 0, 1 • Port 7 • $\overline{RES}$ • HS, VS	Output disable	4.5 to 5.5		$0.1V_{DD}$		V

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD} [V]	min	typ	max	
Input clamp voltage	V_{CLMP}	CVIN		5.0	2.3	2.5	2.7	V
Pin capacitance	CP	All pins	• f = 1 MHz • Unmeasured terminals for the input are set to V_{SS} level. • Ta = 25°C	4.5 to 5.5		10		pF

4. Serial Input/Output Characteristics at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter			Symbol	Pins	Conditions	Ratings				Unit
						V_{DD} [V]	min	typ	max	
Serial clock	Input clock	Cycle	tCKCY(1)	• SCK0 • SCLK0	Refer to Figure 5	4.5 to 5.5	2			tCYC
		Low-level pulse width	tCKL(1)			4.5 to 5.5	1			
		High-level pulse width	tCKH(1)			4.5 to 5.5	1			
	Output clock	Cycle	tCKCY(2)	• SCK0 • SCLK0	• Use a pull-up resistor (1 kΩ) during open drain output • Refer to Figure 5.	4.5 to 5.5	2			
		Low-level pulse width	tCKL(2)			4.5 to 5.5		1/2tCKCY		
		High-level pulse width	tCKH(2)			4.5 to 5.5		1/2tCKCY		
Serial input	Data set-up time		tICK	SI0	• Data set-up to SCK0 rising • Data hold from SCK0 rising • Refer to Figure 5.	4.5 to 5.5	0.1			µs
	Data hold time		tCKI			4.5 to 5.5	0.1			
Serial output	Output delay time (External serial clock)		tCKO(1)	SO0	• Use a pull-up resistor (1 kΩ) during open drain output. • Data set-up to SCK0 falling • Data hold from SCK0 falling • Refer to Figure 5.	4.5 to 5.5			7/12tCYC +0.2	µs
	Output delay time (Internal serial clock)		tCKO(2)			4.5 to 5.5			1/3tCYC +0.2	

5. Pulse Input Conditions at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit
			V_{DD} [V]	min	typ	max	
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	•Interrupt acceptable •Timer0-countable	4.5 to 5.5	1		tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection filter time constant is 1/1)	•Interrupt accept able •Timer0-countable	4.5 to 5.5	2		
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection filter time constant is 1/16)	•Interrupt acceptable •Timer0-countable	4.5 to 5.5	32		
	tPIL(4)	$\overline{RES}$	Reset acceptable	4.5 to 5.5	200		µs
	tPIH(5) tPIL(5)	$\overline{HS}$, $\overline{VS}$	Display position controllable Each active edge of $\overline{HS}$, $\overline{VS}$ must be more than 1tCYC. Refer to Figure 7.	4.5 to 5.5	10		tCYC
Rising/falling time	tTHL tTLH	$\overline{HS}$	Refer to Figure 7.	4.5 to 5.5		500	ns
Horizontal pull-in range	FH	$\overline{HS}$	The monitor point in figure 10 is 1/2 V_{DD}.	4.5 to 5.5	15.23	15.73	16.23	kHz

6. A/D Converter Characteristics at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit
			V_{DD} [V]	min	typ	max	
Resolution	N			4.5 to 5.5		4		bit
Absolute precision	ET		(Note 3)	4.5 to 5.5		±1/4	±1/2	LSB
Conversion time	tCAD	From selecting Vref to resulting	1 bit conversion time = 2tCYC	4.5 to 5.5			1.96	µs
Reference current	I_{REF}		(Regulate the ladder resistor)	4.5 to 5.5		1.0	2.0	mA
Analog input voltage range	V_{AIN}	AN0 to AN3		4.5 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	I_{AINH}		V_{AIN} = V_{DD}	4.5 to 5.5			1	µA
	I_{AINL}		V_{AIN} = V_{SS}	4.5 to 5.5	–1		

(Note 3) Absolute precision excepts quantizing error (±1/2 LSB).

7. Current Drain Characteristics at Ta = –30°C to +70°C , V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD} [V]	min	typ	max	
Current drain during basic operation (Note 4)	I_{DDOP}(1)	DVDD, AVDD	• FmCF = 12 MHz Ceramic resonator oscillation • FmLC = 14.11 MHz LC oscillation • System clock : CF oscillation • Internal RC oscillation stops.	4.5 to 5.5		16	28	mA
Current drain in HALT mode (Note 4)	I_{DDHALT}(1)	DVDD, AVDD	• HALT mode • FmCF = 12 MHz Ceramic resonator oscillation • FmLC = 0 Hz (oscillation stops) • System clock : CF oscillation • Internal RC oscillation stops.	4.5 to 5.5		5	10	mA
	I_{DDHALT}(2)	DVDD, AVDD	• HALT mode • FmCF = 0 MHz (oscillation stops) • FmLC = 0 Hz (oscillation stops) • System clock : Internal RC	4.5 to 5.5		600	1200	µA
Current drain in HOLD mode (Note 4)	I_{DDHOLD}	DVDD, AVDD	• HOLD mode • All oscillation stops.	4.5 to 5.5		0.05	20	µA

(Note 4) The currents of the output transistors and the pull-up MOS transistors are ignored.

Oscillation type	Manufacturer	Oscillator	C1	C2
12 MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33 pF	33 pF
		CST12.0MTW	on chip	
	Kyocera	KBR-12.0M	47 pF	47 pF

* Both C1 and C2 must use an K rank (±10%) and an SL characteristics.

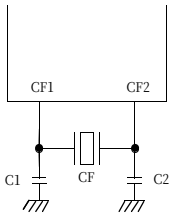
Table 1. Ceramic Resonator Oscillation Guaranteed Constant (main-clock)

Oscillation type	L	C3	C4
14.11MHz LC oscillation	4.7 µH	33 pF	45 pF (Trimmer)
	4.7 µH±10% (Variable)	33 pH	33 pH

* See Figure 11,12.

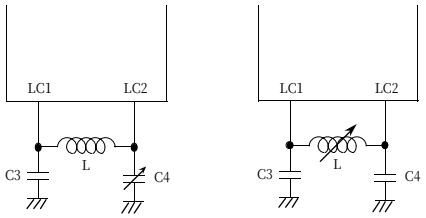
Table 2. LC Oscillation Guaranteed Constant (OSD clock)

(Notes) • Since the circuit pattern may affect the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest pattern length.
• If you use other oscillators than those shown above, we provide no guarantee for the characteristics.
• Adjust the voltage of monitor point in figure 10 to 1/2V_{DD}±10% by the LC oscillation constant 'L' or 'C' to lock the PLL circuit.



Main clock

Figure 1 Ceramic Resonator Oscillation



OSD clock

Figure 2 LC Resonator Oscillation

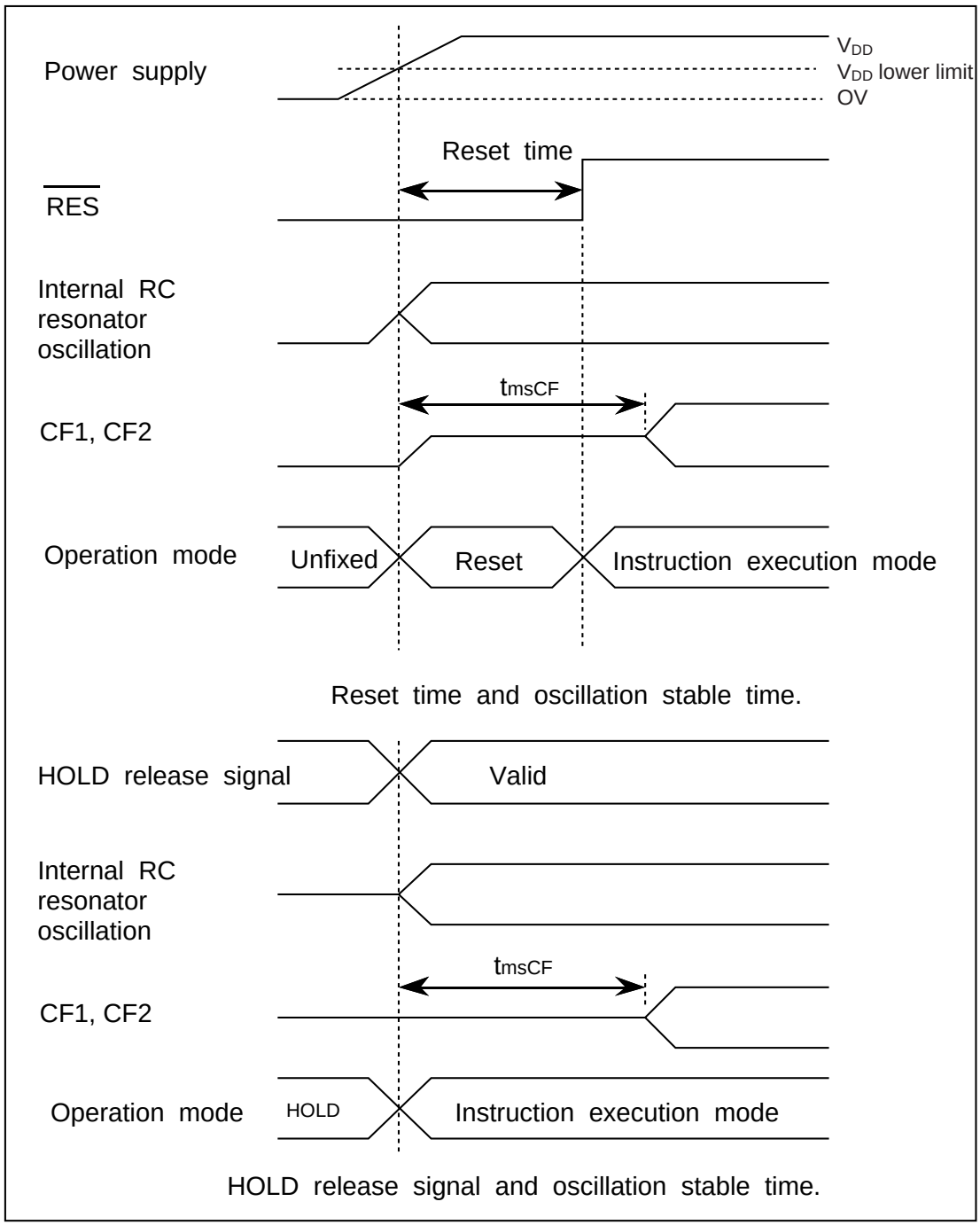
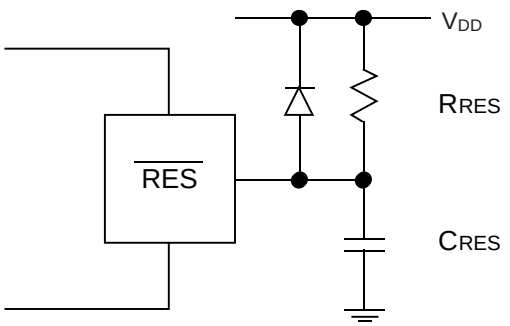
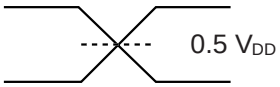


Figure 3 Oscillation Stable Time



(Note) Set the values of C_{RES}, R_{RES} so that the reset time is 200 µs or longer.

Figure 4 Reset Circuit



< AC timing point >

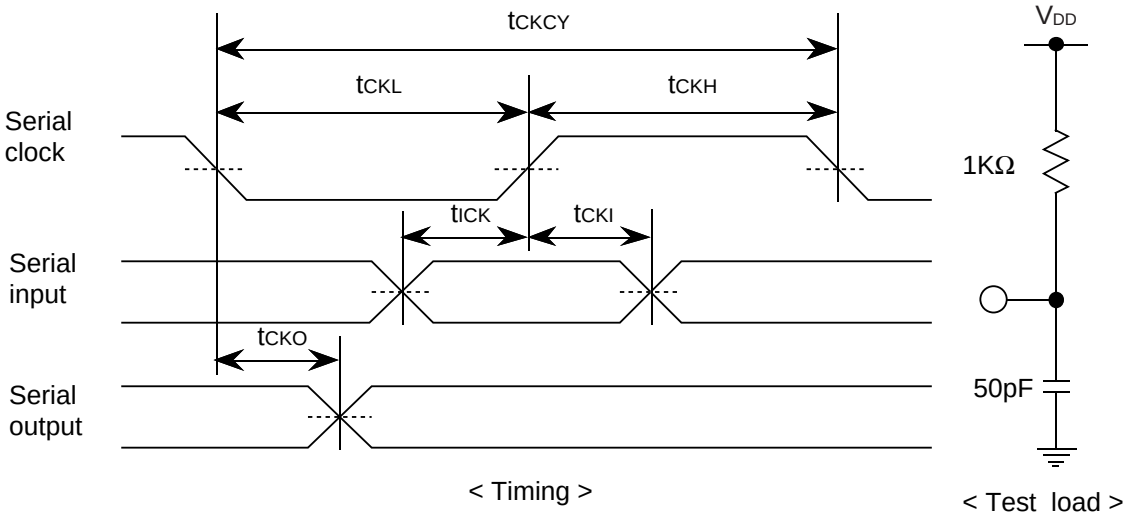


Figure 5 Serial Input/output Test Condition

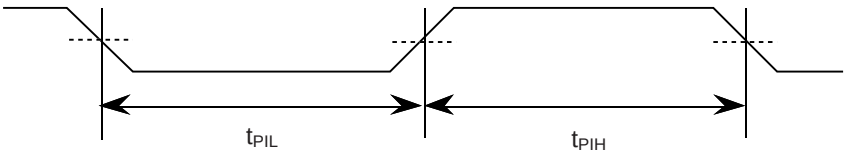
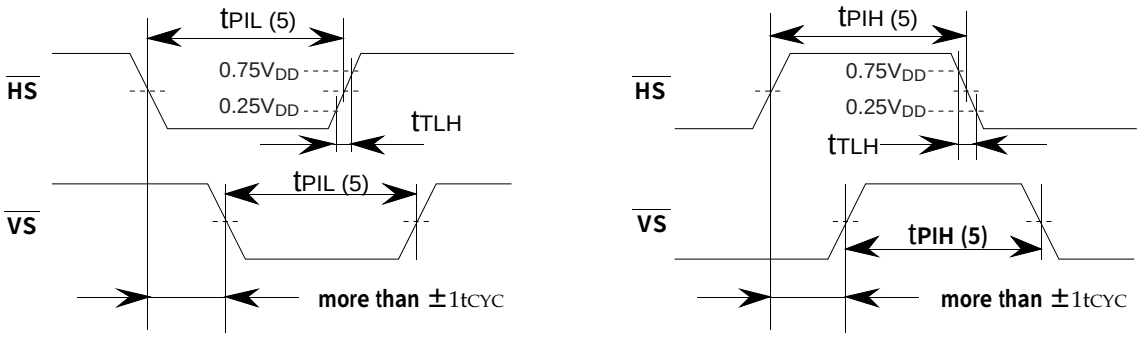


Figure 6 Pulse Input Timing Condition - 1



(a) In case of active low (b) In case of active high

Figure 7 Pulse Input Timing Condition - 2

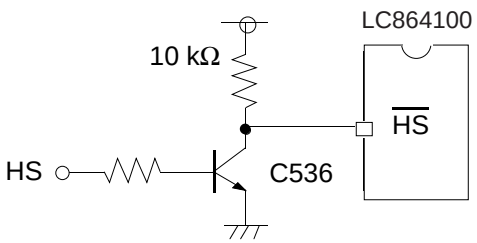


Figure 8 Recommended Interface Circuit

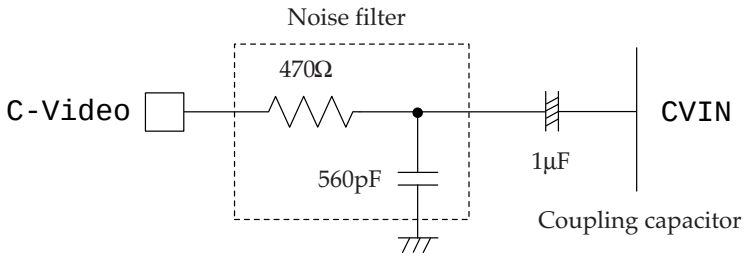


Figure 9 CVIN Recommended Circuit

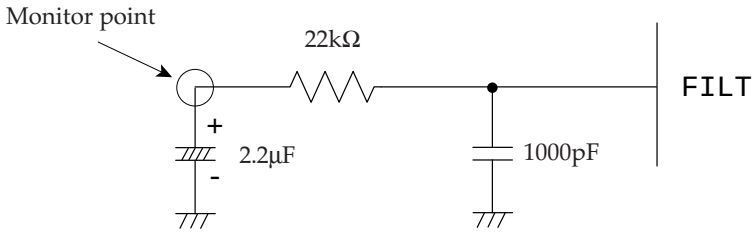


Figure 10 FILT Recommended Circuit

(Note) • Place the parts connected to the FILT terminal as close to the FILT as possible with the shortest pattern length on the board.

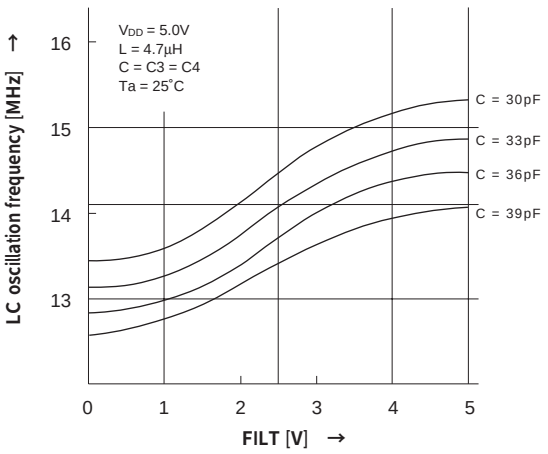


Figure 11 FILT-LC Oscillation Frequency (1)

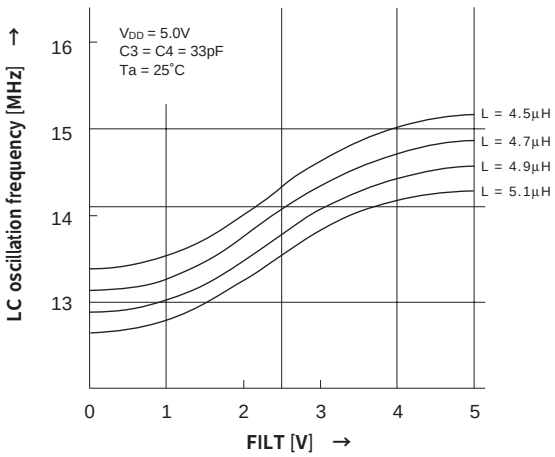


Figure 12 FILT-LC Oscillation Frequency (2)