# LC7537N, 7537AN

SANYO SEMICONDUCTOR CORP

3025B 3052A

CMOS LSI

# Electronic Volume Control System for Audio Equipment



**Functions**

The LC7537N is an electronic control LSI capable of electronically controlling the volume, balance, loudness, fader, bass, and treble functions individually with fewer externally connected component parts.

**Features**

. Enables controlling the below-listed functions with 3-line serial data, including CE, DI, and CLK. Also, due to 0V to 5V swing of the serial data input voltage, permits the use of a general purpose microcomputer.

(1) Volume : Separately controls the Lch and Rch volume levels across 81 positions over the 0dB to -79dB (in 1dB steps) range and -∞, and consequently also serves balance control purposes.

(2) Loudness : By virtue of a center tap provided at the -20dB position of the volume controlling ladder resistors, permits loudness to be controlled with externally connected CR components.

(3) Fader : By varying only the rear or front output level across 16 positions, provides fader functions (in 2dB steps over the 0dB to -20dB range, and 5dB steps over the -20dB to -45dB range, and at -∞, for a total of 16 positions).

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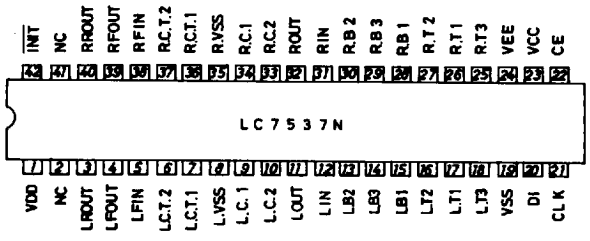
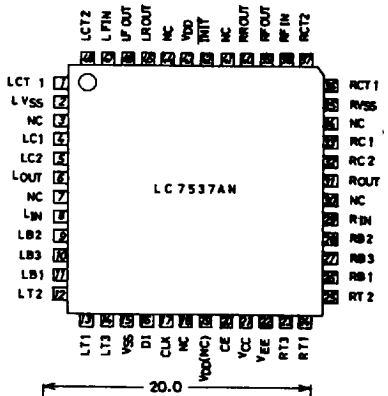
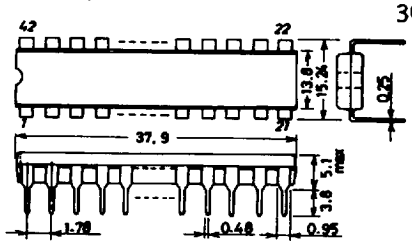
**Pin Assignment**



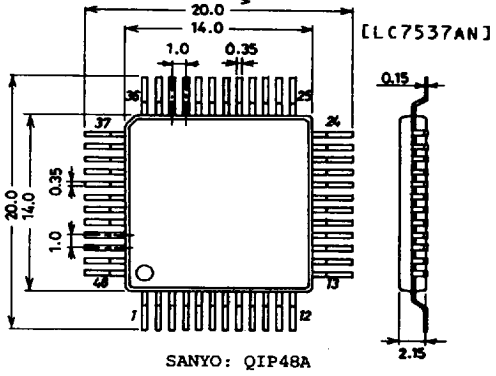




**Case Outline** 3025B (unit:mm) [LC7537N]




SANYO: DIP42S

**Case Outline** (unit:mm) 3052A [LC7537AN]




SANYO: QIP48A

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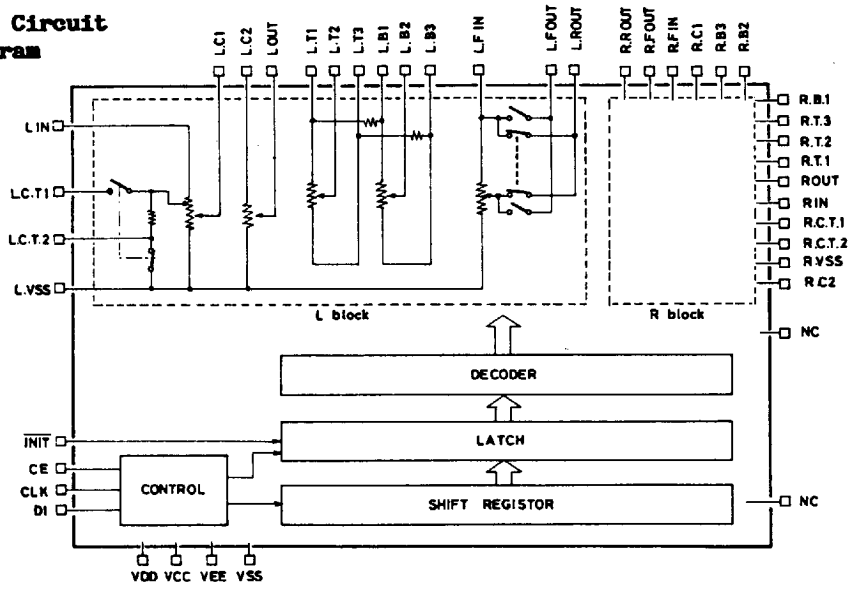
(4) Bass/Treble: With CR components externally connected, forms an NF type tone control circuit (Baxandall type) to exercise control across 15 positions over both the bass and treble functions in 2dB steps.

. By virtue of its CMOS structure, the LSI operates under a broad power supply voltage range from +4.5V to +15V, permitting the use of either a single or a dual ± power supply, whichever is preferred.

**Equivalent Circuit Block Diagram**




**Absolute Maximum Ratings** at Ta=25°C, $V_{SS}$=0V, $V_{DD} \geqq V_{CC} > V_{SS} \geqq V_{EE}$

| | | | | unit |
|---|---|---|---|---|
| Maximum Supply Voltage | $V_{DD}-V_{EE}$ max | $V_{DD}$, $V_{EE}$: $V_{EE} \leqq -8V$ | 16 | V |
| | $V_{CC}$ max | $V_{CC}$: $V_{DD} \geqq V_{CC}$ | $V_{SS}$-0.3 to $V_{SS}$+7 | V |
| Input Supply Voltage | Vi 1 | DI, CLK, CE | $V_{SS}$-0.3 to $V_{DD}$+0.3 | V |
| | Vi 2 | INIT | $V_{EE}$-0.3 to $V_{DD}$+0.3 | V |
| Allowble Power Dissipation | Pdmax | Ta≦85°C | 200 | mW |
| Operating Temperature | Topg | | -40 to +85 | °C |
| Storage Temperature | Tstg*3 | | -50 to +125 | °C |

**Allowable Operating Conditions** at Ta=25°C, $V_{SS}$=0V, $V_{DD} \geqq V_{CC} > V_{SS} \geqq V_{EE}$

| | | | | unit |
|---|---|---|---|---|
| Supply Voltage *1 | $V_{DD}-V_{EE}$ | $V_{EE} \geqq -7.5V$ | 4.5 to 15 | V |
| | $V_{CC}$ | | 4.5 to 5.5 | V |
| Input "H"-Level Voltage | $V_{IH1}$ *2 | DI, CLK, CE | 0.8$V_{CC}$ to $V_{DD}$ | V |
| | $V_{IH2}$ | INIT | 0.8($V_{DD}-V_{EE}$)+$V_{EE}$ to $V_{DD}$ | V |
| Input "L"-Level Voltage | $V_{IL1}$ *2 | DI, CLK, CE | $V_{SS}$ to 0.2$V_{CC}$ | V |
| | $V_{IL2}$ | INIT | $V_{EE}$ to 0.2($V_{DD}-V_{EE}$)+$V_{EE}$ | V |
| Input Signal Amplitude | $V_{IN}$ | | $V_{EE}$ to $V_{DD}$ | Vp-p |
| Input Pulse Width | $t_{\phi w}$ | | 1 min. | us |
| Setup Time | $t_{set\ up}$ | | 1 min. | us |
| Hold Time | $t_{hold}$ | | 1 min. | us |
| Operating Frequency | $f_{opg}$ | | up to 330 | kHz |

*1 : A 1,000pF or larger capacitor should be added on between each individul power supply terminal and $V_{SS}$.

*2 : When the microcomputer side control signals rise faster than $V_{DD}$ for the LC7537N, a 2kohm or higher resistor should be inserted midway on each of the DI, CLK, and CE lines.

*3 : When mounting the QIP package on the board, do not dip the entire package in solder.

**Electrical Characteristics** at Ta=25°C, $V_{DD}$=+7.5V, $V_{EE}$=-7.5V, $V_{CC}$=+5V

| | | | min | typ | max | unit |
|---|---|---|---|---|---|---|
| Total Harmonic Distortion | THD(1) | $V_{IN}$=1V, f=1kHz, all flat overall | | 0.005 | 0.01 | % |
| | THD(2) | $V_{IN}$=1V, f=20kHz, all flat overall | | 0.006 | 0.02 | % |
| Crosstalk | CT | $V_{IN}$=1V, f=1kHz, all flat, Rg=1kohm | 60 | 95 | | dB |
| Maximum Attenuation Output | Vomin(1) | $V_{IN}$=1V, f=1kHz, MAIN, VR=∞, FADER VR=∞ | 80 | 90 | | dB |
| | Vomin(2) | $V_{IN}$=1V, f=1kHz, MAIN VR=∞, $V_{DD}$=8V, FADER VR=∞, $V_{EE}$=$V_{SS}$=0V, C between $V_{SS}$ and GND of L/R=1000uF | 70 | 80 | | dB |
| VR Resistance Value | $R_{VOL(1)}$ | 5dB-step | 12 | 20 | 28 | kohm |
| | $R_{VOL(2)}$ | 1dB-step | 12 | 20 | 28 | kohm |
| | $R_{BASS}$ | | 12 | 20 | 28 | kohm |
| | $R_{TREBLE}$ | | 12 | 20 | 28 | kohm |
| | $R_{FADER}$ | | 12 | 20 | 28 | kohm |
| Output Noise Voltage | $V_{N(1)}$ | All flat overall($I_{HFA}$) Rg=1kohm | | 2 | 10 | uV |
| | $V_{N(2)}$ | 0dB position ($I_{HFA}$) Rg=1kohm, $V_{DD}$=8V, $V_{EE}$=$V_{SS}$=0V | | 2 | 10 | uV |
| Current Dissipation | $I_{DD}$ | $V_{DD}$-$V_{EE}$=15V | | | 1 | mA |
| | $I_{CC}$ | $V_{CC}$=5V | | | 1 | mA |

**Pin Description** ( ):LC7537AN

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| Pin No. | Symbol | Description of Functions | Remarks |
|---|---|---|---|
| 12(8) | L.IN | Main Volume Control Block 5dB-Step Attenuator Input Terminals. These pins should be driven at a low impedance. | |
| 31(29) | R.IN | | |
| 9(4) | L.C1 | Main Volume Control Block 5dB-Step Attenuator Output Terminals. Having been designed to be open, the step positions will develop errors if at low acceptor impedances, so that as high load impedances as possible should be provided. | VR Resistance : 20kohms |
| 34(33) | R.C1 | | |
| 10(5) | L.C2 | Main Volume Control Block 1dB-Step Attenuator Input Terminals. These pins should be driven at a low impedance. | |
| 33(32) | R.C2 | | |
| 11(6) | L.OUT | Main Volume Control Block 1dB-Step Attenuator Output Terminals. Due to the step positions designed to be open, load impedances as high as possible should be provided to them, similar to those for the LC1 and RC1. | VR Resistance : 20kohms |
| 32(31) | R.OUT | | |
| 5(47) | L.FIN | Fader Functions Employing Mode Input Terminals. These pins should be driven at a low impedance. | |
| 38(38) | R.FIN | | |
| 4(46) | L.FOUT | Fader Block Output Terminals. These pins permit the front and rear sides to be faded out independently of each other. Attenuations exercised on Lch will be the same as on Rch. Due to the step positions designed to be open, acceptor impedances as high as possible should be provided to them. | VR Resistance : 20kohms |
| 3(45) | L.ROUT | | |
| 39(39) | R.FOUT | | |
| 40(40) | R.ROUT | | |

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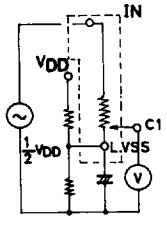
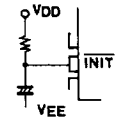
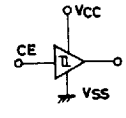
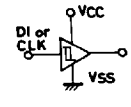
| Pin No. | Symbol | Description of Functions | Remarks |
|---|---|---|---|
| 15(11)<br>16(9)<br>14(10)<br>28(26)<br>27(28)<br>29(27) | L.B1<br>L.B2<br>L.B3<br>R.B1<br>R.B2<br>R.B3 | Bass Tone Control Block Terminals. A total of 15 positions have been provided in 2dB steps. | VR Resistance : 20kohms |
| 17(13)<br>16(12)<br>18(14)<br>26(24)<br>27(25)<br>25(23) | L.T1<br>L.T2<br>L.T3<br>R.T1<br>R.T2<br>R.T3 | Treble Tone Control Block Terminals. A total of 15 positions have been provided in 2dB steps. The VR resistance value is 20kohm. | VR Resistance : 20kohms |
| 7(1)<br>6(48)<br>36(36)<br>37(37) | LCT1<br>LCT2<br>RCT1<br>RCT2 | Loudness Dedicated Terminals. A high-frequency-range correcting C should be put between CT1 and IN, and low-frequency-range-correcting C between CT2 and L.$V_{SS}$ (R.$V_{SS}$). | |
| 8(2)<br><br>35(35) | L.$V_{SS}$<br><br>R.$V_{SS}$ | Main Volume Control Block Fader Control Common Terminals. The impedance of pattern connected to these pins should be as low as possible. Since L.$V_{SS}$, R.$V_{SS}$, and $V_{SS}$ have not been connected inside the LSI, they should be connected together on the outside in conformance with their individual specifications. Particular attenuation should be paid to the capacitance assigned to the capacitors put between L.$V_{SS}$ (R.$V_{SS}$) and $V_{SS}$, which will emerge as a residual resistive component when control is turned down for maximum attenuation. |  |
| 42(42) | $\overline{INIT}$ | Intra-IC Latch Resetting Terminal<br>  <br>Control-setting data at the internal latch will be indeterminate when power has just been switched on, so that by engaging the "L" level of this pin at power-on, the fader control may be set at its -∞ position and muting behavior is engaged (Note: $V_{DD}$-$V_{EE}$ Level). |  |
| 22(20) | CE | Chip Enable Terminal. When this pin is made "H"→"L", data is written in the internal latch, activating the various analog switches. When the "H" level is then restored, transfer of the data will be enabled. |  |
| 20(16)<br><br>21(17) | DI<br><br>CLK | Input Terminals for Serial Data and Clock that serve control purposes. |  |

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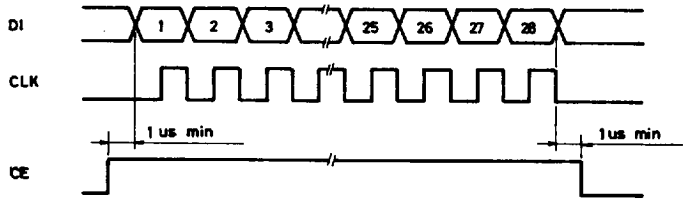
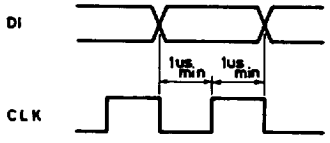
| Pin No. | Symbol | Description of Functions | Remarks |
|---|---|---|---|
| 1(43)<br>23(21)<br>19(15)<br>24(22) | $V_{DD}$<br>$V_{CC}$<br>$V_{SS}$<br>$V_{EE}$ | These pins are connected to the relevant power supplies. Exercise caution against $V_{CC}$ rising earlier than $V_{DD}$. | |
| 2(3,7)<br>41(18,<br>30,34,<br>41,44) | NC | No Connect Pins. Absolutely nothing should be connected here. | |
| (19) | $V_{DD}$(NC) | $V_{DD}$ subterminal. Connected to $V_{DD}$ or left open. | LC7537AN only |

**Control Timing**




**Data Format**

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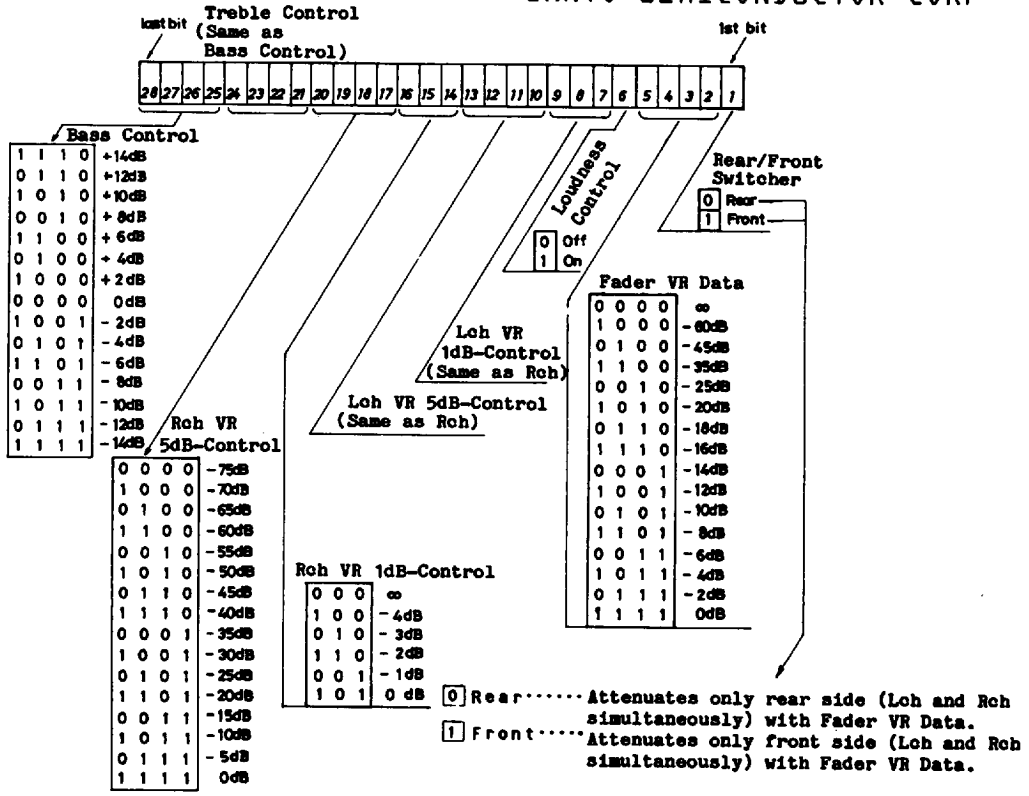
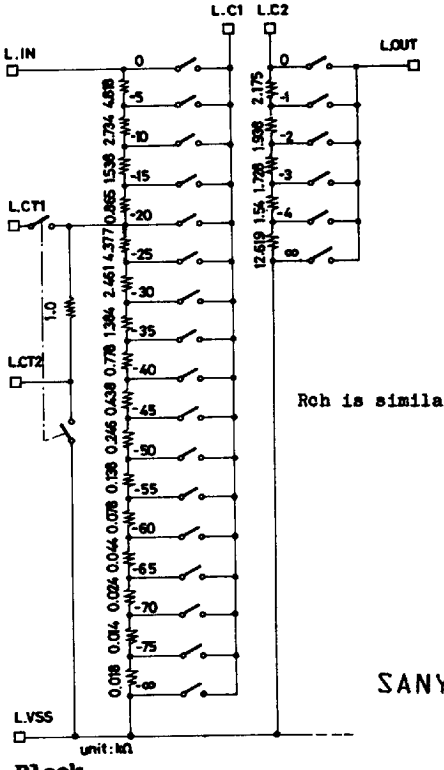


## Main Volume Control Block Equivalent Circuit

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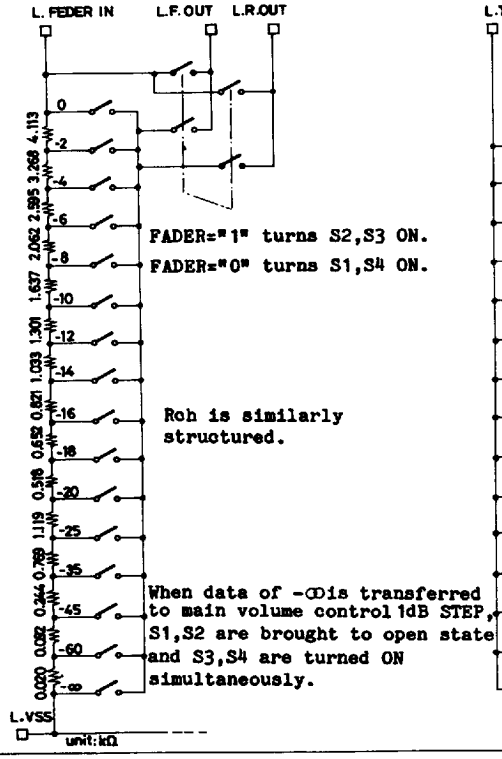
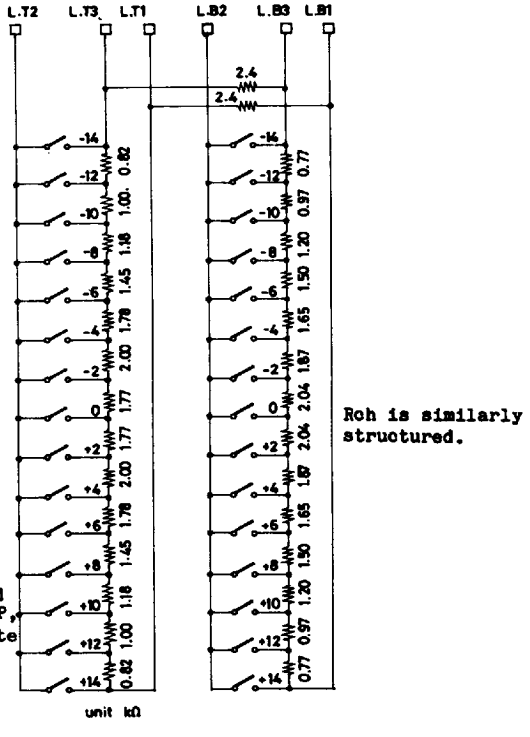
## Fader Volume Control Block Equivalent Circuit




## Tone Control Block Equivalent Circuit



**Sample Application Circuits**
(1) Single Power Supply

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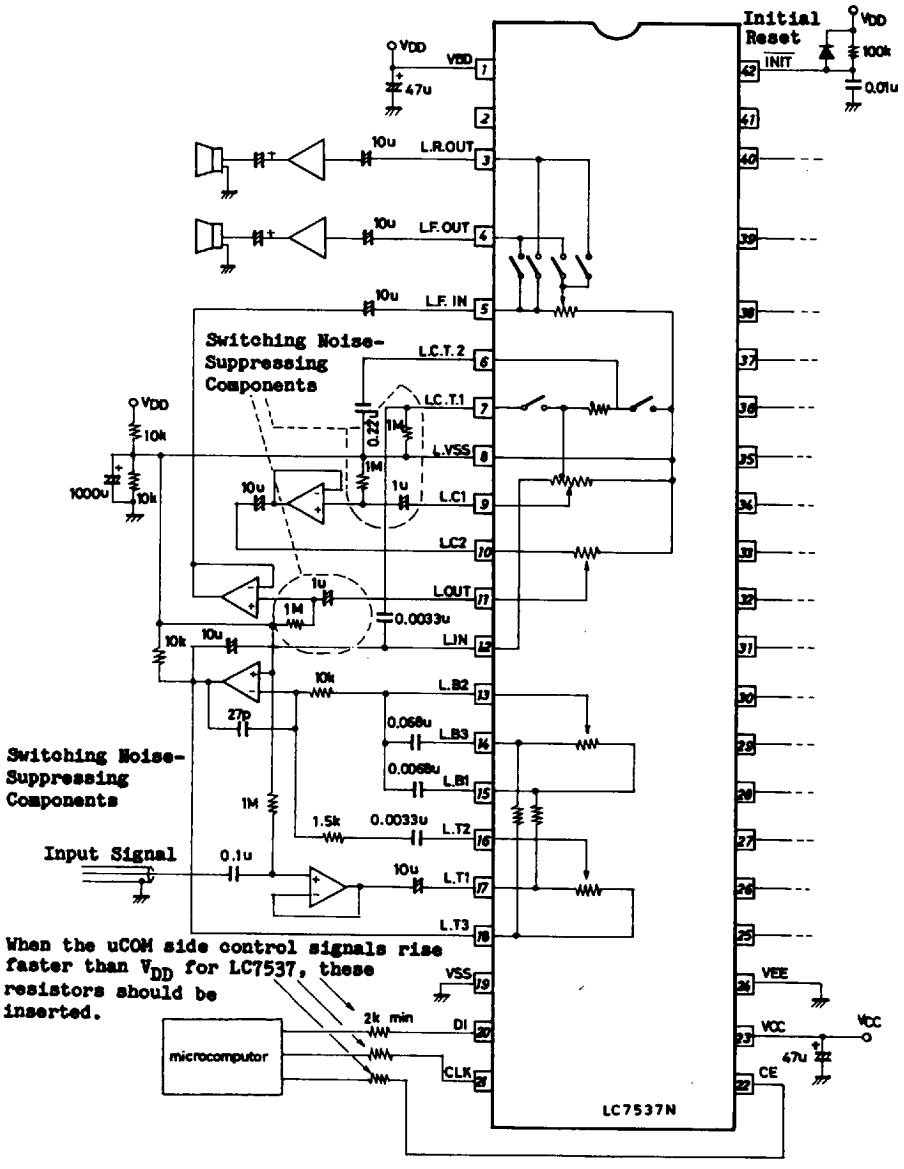


Note: Bipolar electrolytic capacitors should preferably be employed where no polarity has been indicated.

**(2) Dual ± Power Supply**

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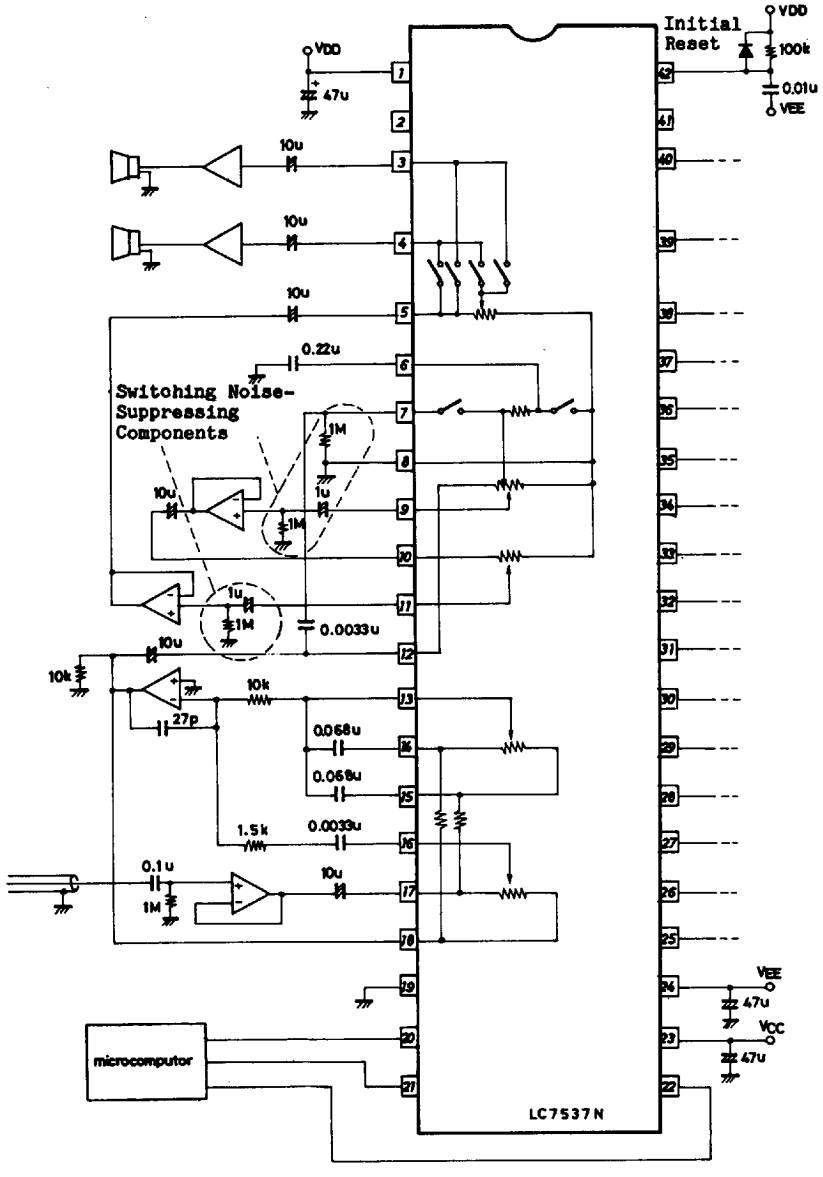


**Note: Bipolar electrolytic capacitors should preferably be employed where no polarity has been indicated.**

**(3) Single Power Supply**

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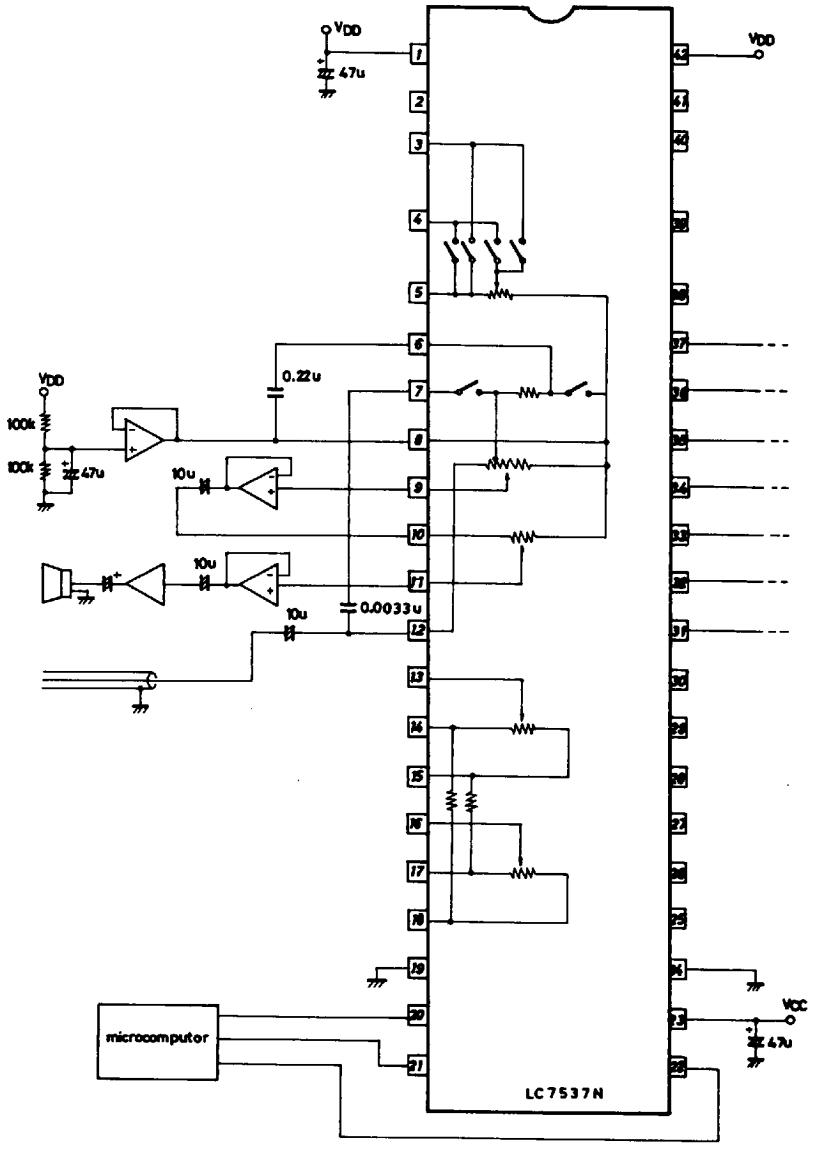


Note: Bipolar electrolytic capacitors should preferably be employed where no polarity has been indicated.

Caution for Pattern Designing

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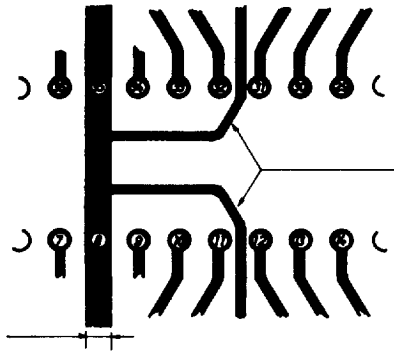
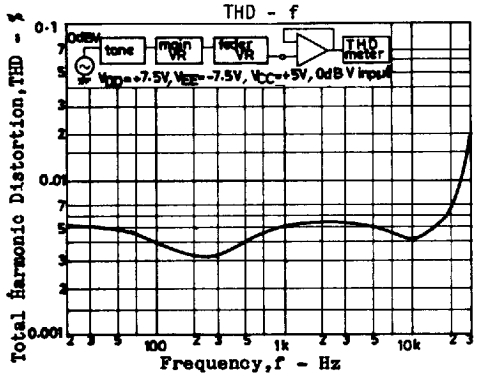
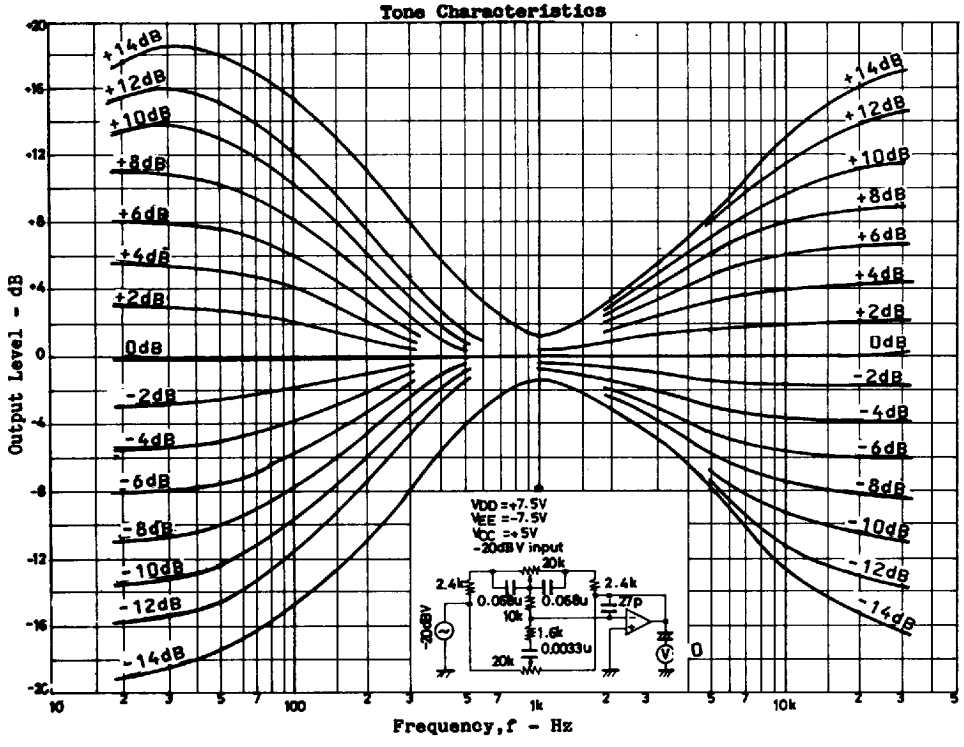



- Space the patterns between L.IN and L.OUT and those between R.IN and R.OUT as far apart as possible. When forced to design them close together, provide shielding patterns between as illustrated. They will be effective at the maximum attenuated level (with 10kHz and higher frequencies).(DIP42S)
- Make the L.$V_{SS}$ and R.$V_{SS}$ as broad as possible.



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