1. General description

The 74HC137 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). The 74HC137 is specified in compliance with JEDEC standard no. 7A.

The 74HC137 is a 3-to-8 line decoder, demultiplexer with latches at the three address inputs (An). The 74HC137 essentially combines the 3-to-8 decoder function with a 3-bit storage latch. When the latch is enabled (LE = LOW), the 74HC137 acts as a 3-to-8 active LOW decoder. When the latch enable (LE) goes from LOW-to-HIGH, the last data present at the inputs before this transition, is stored in the latches. Further address changes are ignored as long as LE remains HIGH.

The output enable input (E1 and E2) controls the state of the outputs independent of the address inputs or latch operation. All outputs are HIGH unless E1 is LOW and E2 is HIGH.

The 74HC137 is ideally suited for implementing non-overlapping decoders in 3-state systems and strobed (stored address) applications in bus oriented systems.

2. Features

- Combines 3-to-8 decoder with 3-bit latch
- Multiple input enable for easy expansion or independent controls
- Active LOW mutually exclusive outputs
- Low-power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from −40 °C to +80 °C and from −40 °C to +125 °C.
3. Quick reference data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PHL}$, $t_{PLH}$</td>
<td>propagation delay</td>
<td>$C_L = 15 \text{ pF} \quad V_{CC} = 5 \text{ V}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>An to $Y_n$</td>
<td></td>
<td>-</td>
<td>18</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$\overline{LE}$ to $Y_n$</td>
<td></td>
<td>-</td>
<td>17</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>E1 to $Y_n$</td>
<td></td>
<td>-</td>
<td>15</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>E2 to $Y_n$</td>
<td></td>
<td>-</td>
<td>15</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

$C_I$ is input capacitance, $C_{PD}$ is power dissipation capacitance.

$P_D = C_{PD} \times V_{CC}^2 \times \frac{1}{2} \times N \times \sum(C_L \times V_{CC}^2) \times f_0$ where:

$\frac{1}{2} \times N$ is number of inputs switching;

$\sum(C_L \times V_{CC}^2) \times f_0$ = sum of outputs.

4. Ordering information

Table 2: Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Temperature range</th>
<th>Name</th>
<th>Description</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>74HC137N</td>
<td>DIP16</td>
<td>$-40 \degree \text{C to } +125 \degree \text{C}$</td>
<td>塑料双排封装；16脚 (300 mil)</td>
<td>SOT38-4</td>
<td></td>
</tr>
<tr>
<td>74HC137D</td>
<td>SO16</td>
<td>$-40 \degree \text{C to } +125 \degree \text{C}$</td>
<td>塑料小外形封装；16脚；宽度3.9 mm</td>
<td>SOT109-1</td>
<td></td>
</tr>
<tr>
<td>74HC137DB</td>
<td>SSOP16</td>
<td>$-40 \degree \text{C to } +125 \degree \text{C}$</td>
<td>塑料小外形封装；16脚；宽度5.3 mm</td>
<td>SOT338-1</td>
<td></td>
</tr>
</tbody>
</table>
5. Functional diagram

**Fig 1. Functional diagram**

**Fig 2. Logic symbol**

**Fig 3. IEC logic symbol**
6. Pinning information

6.1 Pinning

![Logic diagram]

Fig 4. Logic diagram

![Pin configuration]

Fig 5. Pin configuration
6.2 Pin description

Table 3: Pin description

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>1</td>
<td>data input 0</td>
</tr>
<tr>
<td>A1</td>
<td>2</td>
<td>data input 1</td>
</tr>
<tr>
<td>A2</td>
<td>3</td>
<td>data input 2</td>
</tr>
<tr>
<td>LE</td>
<td>4</td>
<td>latch enable input (active LOW)</td>
</tr>
<tr>
<td>E1</td>
<td>5</td>
<td>data enable input 1 (active LOW)</td>
</tr>
<tr>
<td>E2</td>
<td>6</td>
<td>data enable input 2 (active HIGH)</td>
</tr>
<tr>
<td>Y7</td>
<td>7</td>
<td>multiplexer output 7</td>
</tr>
<tr>
<td>GND</td>
<td>8</td>
<td>ground (0 V)</td>
</tr>
<tr>
<td>Y6</td>
<td>9</td>
<td>multiplexer output 6</td>
</tr>
<tr>
<td>Y5</td>
<td>10</td>
<td>multiplexer output 5</td>
</tr>
<tr>
<td>Y4</td>
<td>11</td>
<td>multiplexer output 4</td>
</tr>
<tr>
<td>Y3</td>
<td>12</td>
<td>multiplexer output 3</td>
</tr>
<tr>
<td>Y2</td>
<td>13</td>
<td>multiplexer output 2</td>
</tr>
<tr>
<td>Y1</td>
<td>14</td>
<td>multiplexer output 1</td>
</tr>
<tr>
<td>Y0</td>
<td>15</td>
<td>multiplexer output 0</td>
</tr>
<tr>
<td>VCC</td>
<td>16</td>
<td>positive supply voltage</td>
</tr>
</tbody>
</table>

7. Functional description

7.1 Function table

Table 4: Function table [1]

<table>
<thead>
<tr>
<th>Enable</th>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>LE</td>
<td>E1</td>
<td>Y0</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>H</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
</tbody>
</table>

[1] H = HIGH voltage level;  
L = LOW voltage level;  
X = don’t care.
8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>supply voltage</td>
<td>$-0.5$ to $+7$ V</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IK}$</td>
<td>input diode current</td>
<td>$V_I &lt; -0.5$ V or $V_I &gt; V_{CC} + 0.5$ V</td>
<td>-</td>
<td>±20</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{OK}$</td>
<td>output diode current</td>
<td>$V_O &lt; -0.5$ V or $V_O &gt; V_{CC} + 0.5$ V</td>
<td>-</td>
<td>±25</td>
<td>mA</td>
</tr>
<tr>
<td>$I_O$</td>
<td>output source or sink current</td>
<td>$V_O = -0.5$ V to $V_{CC} + 0.5$ V</td>
<td>-</td>
<td>±25</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CC}$, $I_{GND}$</td>
<td>$V_{CC}$ or GND current</td>
<td>-</td>
<td>±50</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>storage temperature</td>
<td>$-65$ to $+150$ °C</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>$P_{tot}$</td>
<td>power dissipation</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>DIP16 package</td>
<td>$[1]$ - $750$ mW</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SO16 and SSOP16</td>
<td>packages</td>
<td>$[2]$ - $500$ mW</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[1] Above 70 °C: $P_{tot}$ derates linearly with 12 mW/K.
[2] Above 70 °C: $P_{tot}$ derates linearly with 8 mW/K.

9. Recommended operating conditions

Table 6: Recommended operating conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>supply voltage</td>
<td>$2.0$ to $6.0$ V</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_I$</td>
<td>input voltage</td>
<td>$0$ to $V_{CC}$</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_O$</td>
<td>output voltage</td>
<td>$0$ to $V_{CC}$</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$t_r$, $t_f$</td>
<td>input rise and fall times</td>
<td>$V_{CC} = 2.0$ V</td>
<td>-</td>
<td>-</td>
<td>1000</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 4.5$ V</td>
<td>-</td>
<td>6.0</td>
<td>500</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 6.0$ V</td>
<td>-</td>
<td>-</td>
<td>400</td>
<td>ns</td>
</tr>
<tr>
<td>$T_{amb}$</td>
<td>ambient temperature</td>
<td>$-40$ to $+125$ °C</td>
<td></td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>
## 10. Static characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>( T_{\text{amb}} = 25 ^\circ \text{C} )</th>
<th>( T_{\text{amb}} = -40 ^\circ \text{C to } +85 ^\circ \text{C} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{IH}} )</td>
<td>HIGH-level input voltage</td>
<td>( V_{\text{CC}} = 2.0 ) ( \text{V} )</td>
<td>1.5</td>
<td>1.2 ( \text{- V} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{\text{CC}} = 4.5 ) ( \text{V} )</td>
<td>3.15</td>
<td>2.4 ( \text{- V} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{\text{CC}} = 6.0 ) ( \text{V} )</td>
<td>4.2</td>
<td>3.2 ( \text{- V} )</td>
</tr>
<tr>
<td>( V_{\text{IL}} )</td>
<td>LOW-level input voltage</td>
<td>( V_{\text{CC}} = 2.0 ) ( \text{V} )</td>
<td>-</td>
<td>0.8 ( \text{0.5 \text{V}} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{\text{CC}} = 4.5 ) ( \text{V} )</td>
<td>-</td>
<td>2.1 ( \text{1.35 \text{V}} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{\text{CC}} = 6.0 ) ( \text{V} )</td>
<td>-</td>
<td>2.8 ( \text{1.8 \text{V}} )</td>
</tr>
<tr>
<td>( V_{\text{OH}} )</td>
<td>HIGH-level output voltage</td>
<td>( V_{\text{I}} = V_{\text{IH}} ) or ( V_{\text{IL}} )</td>
<td>( I_{\text{O}} = -20 ) ( \mu \text{A} ); ( V_{\text{CC}} = 2.0 ) ( \text{V} )</td>
<td>1.9 ( \text{2.0 \text{- V}} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( I_{\text{O}} = -20 ) ( \mu \text{A} ); ( V_{\text{CC}} = 4.5 ) ( \text{V} )</td>
<td>4.4 ( \text{4.5 \text{- V}} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( I_{\text{O}} = -20 ) ( \mu \text{A} ); ( V_{\text{CC}} = 6.0 ) ( \text{V} )</td>
<td>5.9 ( \text{6.0 \text{- V}} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( I_{\text{O}} = -4 ) ( \text{mA} ); ( V_{\text{CC}} = 4.5 ) ( \text{V} )</td>
<td>3.98 ( \text{4.32 \text{- V}} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( I_{\text{O}} = -5.2 ) ( \text{mA} ); ( V_{\text{CC}} = 6.0 ) ( \text{V} )</td>
<td>5.48 ( \text{5.81 \text{- V}} )</td>
</tr>
<tr>
<td>( V_{\text{OL}} )</td>
<td>LOW-level output voltage</td>
<td>( V_{\text{I}} = V_{\text{IH}} ) or ( V_{\text{IL}} )</td>
<td>( I_{\text{O}} = 20 ) ( \mu \text{A} ); ( V_{\text{CC}} = 2.0 ) ( \text{V} )</td>
<td>- ( \text{0 \text{0.1 \text{V}} \text{- V}} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( I_{\text{O}} = 20 ) ( \mu \text{A} ); ( V_{\text{CC}} = 4.5 ) ( \text{V} )</td>
<td>- ( \text{0 \text{0.1 \text{V}} \text{- V}} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( I_{\text{O}} = 20 ) ( \mu \text{A} ); ( V_{\text{CC}} = 6.0 ) ( \text{V} )</td>
<td>- ( \text{0 \text{0.1 \text{V}} \text{- V}} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( I_{\text{O}} = 4 \text{mA} ); ( V_{\text{CC}} = 4.5 ) ( \text{V} )</td>
<td>- ( \text{0.15 \text{0.26 \text{V}} \text{- V}} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( I_{\text{O}} = 5.2 \text{mA} ); ( V_{\text{CC}} = 6.0 ) ( \text{V} )</td>
<td>- ( \text{0.16 \text{0.26 \text{V}} \text{- V}} )</td>
</tr>
<tr>
<td>( I_{\text{IL}} )</td>
<td>input leakage current</td>
<td>( V_{\text{I}} = V_{\text{CC}} ) or ( \text{GND} ); ( V_{\text{CC}} = 6.0 ) ( \text{V} )</td>
<td>-</td>
<td>- ( \text{±0.1 \text{\muA}} )</td>
</tr>
<tr>
<td>( I_{\text{CC}} )</td>
<td>quiescent supply current</td>
<td>( V_{\text{I}} = V_{\text{CC}} ) or ( \text{GND} ); ( I_{\text{O}} = 0 ) ( \text{A} ); ( V_{\text{CC}} = 6.0 ) ( \text{V} )</td>
<td>-</td>
<td>- ( \text{8.0 \text{\muA}} )</td>
</tr>
<tr>
<td>( C_{\text{I}} )</td>
<td>input capacitance</td>
<td>-</td>
<td>3.5</td>
<td>- ( \text{pF} )</td>
</tr>
</tbody>
</table>

At recommended operating conditions; voltages are referenced to \( \text{GND} \) (ground = 0 \text{V}).
Table 7: Static characteristics…continued
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OL}$</td>
<td>LOW-level output voltage</td>
<td>$V_I = V_{IH}$ or $V_{IL}$</td>
<td>$I_O = 20 \mu A$; $V_{CC} = 2.0$ V</td>
<td>-</td>
<td>-</td>
<td>0.1 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$I_O = 20 \mu A$; $V_{CC} = 4.5$ V</td>
<td>-</td>
<td>-</td>
<td>0.1 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$I_O = 20 \mu A$; $V_{CC} = 6.0$ V</td>
<td>-</td>
<td>-</td>
<td>0.1 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$I_O = 4$ mA; $V_{CC} = 4.5$ V</td>
<td>-</td>
<td>-</td>
<td>0.33 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$I_O = 5.2$ mA; $V_{CC} = 6.0$ V</td>
<td>-</td>
<td>-</td>
<td>0.33 V</td>
</tr>
<tr>
<td>$I_{LI}$</td>
<td>input leakage current</td>
<td>$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V</td>
<td>-</td>
<td>-</td>
<td>±1.0 \mu A</td>
<td></td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>quiescent supply current</td>
<td>$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V</td>
<td>-</td>
<td>-</td>
<td>80 \mu A</td>
<td></td>
</tr>
</tbody>
</table>

$T_{amb} = -40$ °C to $+125$ °C

$V_{IH}$ HIGH-level input voltage

| $V_{IH}$ | HIGH-level input voltage | | $V_{CC} = 2.0$ V | 1.5 | - | - | V |
| | | | $V_{CC} = 4.5$ V | 3.15 | - | - | V |
| | | | $V_{CC} = 6.0$ V | 4.2 | - | - | V |

$V_{IL}$ LOW-level input voltage

| $V_{IL}$ | LOW-level input voltage | | $V_{CC} = 2.0$ V | - | - | 0.5 V |
| | | | $V_{CC} = 4.5$ V | - | - | 1.35 V |
| | | | $V_{CC} = 6.0$ V | - | - | 1.8 V |

$V_{OH}$ HIGH-level output voltage

| $V_{OH}$ | HIGH-level output voltage | | $V_I = V_{IH}$ or $V_{IL}$ | - | - | - | V |
| | | | $I_O = -20 \mu A$; $V_{CC} = 2.0$ V | 1.9 | - | - | V |
| | | | $I_O = -20 \mu A$; $V_{CC} = 4.5$ V | 4.4 | - | - | V |
| | | | $I_O = -20 \mu A$; $V_{CC} = 6.0$ V | 5.9 | - | - | V |
| | | | $I_O = -4$ mA; $V_{CC} = 4.5$ V | 3.7 | - | - | V |
| | | | $I_O = -5.2$ mA; $V_{CC} = 6.0$ V | 5.2 | - | - | V |

$V_{OL}$ LOW-level output voltage

| $V_{OL}$ | LOW-level output voltage | | $V_I = V_{IH}$ or $V_{IL}$ | - | - | - | V |
| | | | $I_O = 20 \mu A$; $V_{CC} = 2.0$ V | - | - | 0.1 V |
| | | | $I_O = 20 \mu A$; $V_{CC} = 4.5$ V | - | - | 0.1 V |
| | | | $I_O = 20 \mu A$; $V_{CC} = 6.0$ V | - | - | 0.1 V |
| | | | $I_O = 4$ mA; $V_{CC} = 4.5$ V | - | - | 0.4 V |
| | | | $I_O = 5.2$ mA; $V_{CC} = 6.0$ V | - | - | 0.4 V |

$I_{LI}$ input leakage current

| $I_{LI}$ | input leakage current | | $V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V | - | - | ±1.0 \mu A |

$I_{CC}$ quiescent supply current

| $I_{CC}$ | quiescent supply current | | $V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V | - | - | 160 \mu A |
11. Dynamic characteristics

Table 8: Dynamic characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
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Table 8: Dynamic characteristics...continued

\( GND = 0 \text{ V}; t_r = t_f = 6 \text{ ns}; C_L = 50 \text{ pF} \)

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Table 8: Dynamic characteristics (continued)

GND = 0 V; \( t_r = t_f = 6 \text{ ns} \); \( C_L = 50 \text{ pF} \).

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<td>ns</td>
</tr>
<tr>
<td>( t_{H} )</td>
<td>hold time An to ( \bar{I} )</td>
<td>see Figure 8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_{CC} = 2.0 \text{ V} )</td>
<td></td>
<td></td>
<td></td>
<td>45</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>( V_{CC} = 4.5 \text{ V} )</td>
<td></td>
<td></td>
<td></td>
<td>9</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>( V_{CC} = 6.0 \text{ V} )</td>
<td></td>
<td></td>
<td></td>
<td>8</td>
<td>ns</td>
</tr>
</tbody>
</table>

[1] \( C_{PD} \) is used to determine the dynamic power dissipation (\( P_D \) in \( \mu \text{W} \)).
\[
P_D = C_{PD} \times V_{CC}^2 \times t_i \times N + \sum(C_L \times V_{CC}^2 \times t_o)
\]
where:
- \( t_i \) = input frequency in MHz;
- \( t_o \) = output frequency in MHz;
- \( C_L \) = output load capacitance in pF;
- \( V_{CC} \) = supply voltage in V;
- \( N \) = number of inputs switching;
- \( \sum(C_L \times V_{CC}^2 \times t_o) \) = sum of outputs.

Table 8: Dynamic characteristics (continued)
12. Waveforms

Fig 6. Waveforms showing the address input (An) and enable input (E2) to output ($\overline{Y}_n$) propagation delays and the output transition times.

$V_M = 0.5 \times V_i.$

Fig 7. Waveforms showing the enable input (E1, LE) to output ($\overline{Y}_n$) propagation delays and the output transition times.

$V_M = 0.5 \times V_i.$

Fig 8. Waveforms showing the data set-up, hold times for An input to LE input and the latch enable pulse width.

The shaded areas indicate when the input is permitted to change for predictable output performance.

$V_M = 0.5 \times V_i.$
13. Application information

Test data is given in Table 9.
Definitions for test circuit:
- $R_T =$ Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.
- $C_L =$ Load capacitance including jig and probe capacitance.

Fig 9. Load circuitry for switching times

<table>
<thead>
<tr>
<th>Supply $V_{CC}$</th>
<th>Input $V_I$</th>
<th>$t_r$, $t_f$ (ns)</th>
<th>Load $C_L$ (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0 V</td>
<td>$V_{CC}$</td>
<td>6</td>
<td>50</td>
</tr>
<tr>
<td>4.5 V</td>
<td>$V_{CC}$</td>
<td>6</td>
<td>50</td>
</tr>
<tr>
<td>6.0 V</td>
<td>$V_{CC}$</td>
<td>6</td>
<td>50</td>
</tr>
<tr>
<td>5.0 V</td>
<td>$V_{CC}$</td>
<td>6</td>
<td>15</td>
</tr>
</tbody>
</table>

Fig 10. 6-to-64 line decoder with input address storage
14. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)  

**Fig 11. Package outline SOT38-4**

**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

<table>
<thead>
<tr>
<th>UNIT</th>
<th>A</th>
<th>A1 min.</th>
<th>A2 max.</th>
<th>b</th>
<th>b1</th>
<th>b2</th>
<th>c</th>
<th>D(1)</th>
<th>E(1)</th>
<th>e</th>
<th>e1</th>
<th>L</th>
<th>M0</th>
<th>M1</th>
<th>W</th>
<th>Z(1) max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>mm</td>
<td>4.2</td>
<td>0.51</td>
<td>3.2</td>
<td>1.73</td>
<td>0.53</td>
<td>1.25</td>
<td>0.36</td>
<td>19.50</td>
<td>6.48</td>
<td>2.54</td>
<td>7.62</td>
<td>3.60</td>
<td>8.25</td>
<td>10.0</td>
<td>0.254</td>
<td>0.76</td>
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<tr>
<td>inches</td>
<td>0.17</td>
<td>0.02</td>
<td>0.13</td>
<td>0.068</td>
<td>0.051</td>
<td>0.049</td>
<td>0.009</td>
<td>0.77</td>
<td>0.26</td>
<td>0.1</td>
<td>0.3</td>
<td>0.14</td>
<td>0.32</td>
<td>0.39</td>
<td>0.01</td>
<td>0.03</td>
</tr>
</tbody>
</table>

**Note**  
1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

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**Fig 11. Package outline SOT38-4 (DIP16)**
Philips Semiconductors

74HC137

3-to-8 line decoder, demultiplexer with address latches; inverting

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

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<th>UNIT</th>
<th>A max.</th>
<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>b_p</th>
<th>c</th>
<th>D(1)</th>
<th>E(1)</th>
<th>e</th>
<th>H_E</th>
<th>L</th>
<th>L_p</th>
<th>Q</th>
<th>V</th>
<th>w</th>
<th>y</th>
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<tr>
<td>mm</td>
<td>1.75</td>
<td>0.25</td>
<td>1.25</td>
<td>0.25</td>
<td>0.49</td>
<td>0.25</td>
<td>10.0</td>
<td>4.0</td>
<td>1.27</td>
<td>6.2</td>
<td>1.05</td>
<td>1.0</td>
<td>0.7</td>
<td>0.25</td>
<td>0.7</td>
<td>0.1</td>
<td>0.7</td>
<td>0.3</td>
</tr>
<tr>
<td>inches</td>
<td>0.069</td>
<td>0.010</td>
<td>0.004</td>
<td>0.057</td>
<td>0.049</td>
<td>0.01</td>
<td>0.019</td>
<td>0.014</td>
<td>0.00075</td>
<td>0.39</td>
<td>0.16</td>
<td>0.15</td>
<td>0.05</td>
<td>0.244</td>
<td>0.011</td>
<td>0.228</td>
<td>0.041</td>
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Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION

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Fig 12. Package outline SOT109-1 (SO16)
Philips Semiconductors

74HC137

3-to-8 line decoder, demultiplexer with address latches; inverting

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

DIMENSIONS (mm are the original dimensions)

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<thead>
<tr>
<th>UNIT</th>
<th>A max</th>
<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>bD</th>
<th>c</th>
<th>D(1)</th>
<th>E(1)</th>
<th>e</th>
<th>HE</th>
<th>L</th>
<th>LP</th>
<th>Q</th>
<th>v</th>
<th>w</th>
<th>y</th>
<th>Z(1)</th>
<th>ø</th>
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<tbody>
<tr>
<td>mm</td>
<td>2</td>
<td>0.21</td>
<td>1.80</td>
<td>0.25</td>
<td>0.38</td>
<td>0.20</td>
<td>6.4</td>
<td>6.0</td>
<td>0.65</td>
<td>1.9</td>
<td>7.9</td>
<td>7.6</td>
<td>1.25</td>
<td>1.03</td>
<td>0.9</td>
<td>0.2</td>
<td>0.13</td>
<td>0.1</td>
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</table>

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION

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<tr>
<td>IEC</td>
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Fig 13. Package outline SOT338-1 (SSOP16)
## 15. Revision history

**Table 10: Revision history**

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<th>Data sheet status</th>
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16. Data sheet status

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<td>This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.</td>
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<td>This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).</td>
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[1] Please consult the most recently issued data sheet before initiating or completing a design.
[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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For sales office addresses, send an email to: sales.addresses@www.semiconductors.philips.com
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